Summary of Events

Sunday, 5/17
Registration
Tutorial on System – 1st part
Lunch Break (provided)
Tutorial on 3D-Memory – 2nd part

Monday, 5/18
Registration
Opening remarks
Session #1
Committee Luncheon
Lunch (on your own)
Session #2
Panel discussion
Poster Session
Reception

Tuesday, 5/19
Registration
Session #3
Session #4
Lunch Break (on your own)
Session #5
Session #6
Banquet (provided)

Wednesday, 5/20
Registration
Session #7
Session #8
Lunch (provided)
Session #9
Closing Remarks

Poster Session
Monday May 18th, 2015  6:00 PM – 8:30 PM  POSTER PAPERS

1) L. Crespi, Politecnico di Milano, “Modeling of Atomic Migration Phenomena in Phase Change Memory Devices”
2) Z. Jiang, Stanford University, “Performance Prediction of Large-Scale 1T1R Resistive Memory Array Using Machine Learning”
3) N. D. Lu, Chinese Academy of Sciences, “A Novel Approach to Identify the Carrier Transport Path and its Correlation to the Current Variation in RRAM”
4) J. Bartoli, Aix-Marseille Université /STMicroelectronics, “Optimization of the ATW non-volatile memory for connected smart objects”
5) Roger Lo, Macronix InternationalCo., Ltd / National Chiao Tung University, “A Study of Blocking and Tunnel Oxide Engineering on Double-Trap (DT) BE-SONOS Performance”
6) B. L. Ji, SUNY Polytechnic Institute/SEMTECH, “In-Line-Test of Variability and Bit-Error-Rate of HfOx-Based Resistive Memory”
7) Nhan Do, Silicon Storage Technology (Micron), “A 55 nm Logic-Process-Compliant, Split-Gate Flash Memory Array Fully Demonstrated at Automotive Temperature with High Access Speed and Reliability”
10) Hao Wang, RPI, “Efficiently Realizing Weak Cell Aware DRAM Error Tolerance for Sub-20nm Technology Nodes”
11) F. Memrik-Bayat, UCSB, “Memory Technologies for Neural Networks”
Monday May 18, 2015
Registration 7:00 AM - 6:00 PM

Session #1 8:00 AM - 12:00 PM Invited Talk
Chairs: Sung-Chong Jung, SK-Hynix, Korea
Jing Li, UW-Madison, USA

8:00 AM Sung-Chong Jung, Opening Remarks
8:20 AM Sung-Yi Park, SK-Hynix, “Technology scaling challenges and Future prospects of DRAM and NAND Flash memory”
8:50 AM Will Akin, Micron, “Understanding NAND’s intrinsic characteristics critical role in Solid State Drive (SSD) design: A key enabler for Enterprise Data Center applications”
9:20 AM Dale Juennemann and Prasad Allur, Intel, “Accelerating NVM adoption in PCs: A system study to identify the enablers”

9:50 AM Break (Refreshments Provided)
10:20 AM Barbara desaleo, CEA-LETI, “From memory in our brain to future Silicon-based memory technologies”
11:20 AM Shinobu Fujita, Toshiba, “Technology trends and near-future applications of embedded STT/RAM”
11:50 PM Lunch Break (on your own)
12:00 PM Committee Luncheon

Session #2 2:00 PM – 3:40 PM RRAM-1
Chair: Knobloch Klaus, Infineon, Germany
Steve Heinrich-Barna, Texas Instrument, USA

2:00 PM B. Gorceaux, IMEC, “Thin-Silicon Injector (TSI): an All-Silicon Engineered Barrier, Highly Nonlinear Select for High Density Resistive RAM Applications”
2:25 PM A. Schönhals, RWTH-Aachen University, “Critical ReRAM Stack Parameters Controlling Complementary versus Bipolar Resistive Switching”
2:50 PM S. Lee, POSTECH, “Comprehensive Methodology for ReRAM and Selecteur Design Guideline of Cross-point Array”
3:15 PM X. Huang, Tsinghua University, “Optimization of TiN/TaOx/HfO2/Ti NRAM Arrays for Improved Switching and Data Retention”
3:40 PM Break (Refreshments Provided)

Panel Discussion: 4:00 PM – 5:30 PM
Future of Memory: Application-driven or Technology-driven, which will dominate in the new era of computing?
Panelists: Will Akin, Micron
Thomas Coughlin, Coughlin Associates
Barbara De Salvo, CEA-LETI
Dale Juennemann, Intel
Ming Liu, IMECAS
Joseph Wang, Qualcomm

Moderator: Jing Li, UW-Madison, USA

Poster Session: 6:00 PM – 8:30 PM
Chair: Gill Lee, Applied Materials, USA
6:00 PM Poster Introduction
(See the front page for the list of poster papers)

Reception 6:00 PM – 8:30 PM
Sponsor: Applied Materials, Inc., USA

Tuesday May 19, 2015
Registration 7:00 AM – 5:00 PM

Session #3 8:00 AM – 9:40 AM RRAM-2
Chairs: Steve Heinrich-Barna, Texas Instrument, USA

8:00 AM M. Kudo, Hokkaido University, “Visualization of Conductive Filament during Write and Erase Cycles on Nanometer-scale ReRAM Achieved by In-situ TEM”
8:25 AM J. Baek, SKH, “A Reliable Cross-Point MLC ReRAM with Slew Current Compensation”
8:50 AM A. Grossi, Universita’ di Ferrara, “Relationship among current fluctuations during forming, cell-to-cell variability and reliability in RRAM arrays”
9:15 AM J. Tranchant, Universite de Nantes, “From resistive switching mechanisms in AM4Q Mott insulators to Mott memories”

9:40 AM Break (Refreshments Provided)

Session #4 10:05 AM – 12:10 AM NAND
Chairs: Ken Takeuchi, Chuo University, Japan
Geert Van den bosch, imec, Belgium

10:05 AM L. Breuil, imec, “Optimization of Ru based Hybrid Floating Gate For Planar NAND Flash”
10:30 AM W. Kuwer, Micron, “A Highly Reliable and Cost Effective 19nm Planar NAND Cell Technology”
10:55 AM E. Capogreco, imec, “Integration and electrical evaluation of epitaxialy grown Si and SiGe channels for vertical NAND Memory applications”
11:20 AM D. Oh, SK-Hynix, “TCAD Simulation of Data Retention Characteristics of Charge Trap Devia for 3-D NAND Flash Memory”
11:45 AM P. Khayat, Micron, “Performance Characterization of LDPC Codes for Large-Volume NAND Flash Drive”
12:10 PM Lunch Break (on your own)

Session #5 2:00 PM – 3:40 PM DRAM/Oxide RAM/2RAM/SRAM
Chairs: Fukuzumi Yoshiaki, Toshiba, Japan

2:00 PM K. Min, SK Hynix, “Study on the Sub-threshold Margin Characteristics of the Extremely Scaled 3-D DRAM Cell Transistors”
2:25 PM T. Matsui, Semiconductor Energy Laboratory Co., Ltd., “A 16-Level-Cell Nonvolatile Memory with Crystalline-In-Ga-Zn Oxide FET”
2:50 PM S. Dutta, IIT Bombay, “A Bulk Planar SiGe Quantum-Well based 2RAM with Low VT Variability”
3:40 PM Break (Refreshments Provided)

Session #6 4:10 PM – 5:00 PM MRAM/FRAM
Chairs: Scott Sumnerfelt, Texas Instrument, USA
Knobloch Klaus, Infineon, Germany

4:10 PM H. Saito, Fujitsu, “A Triple Protection Structured COB FRAM with 1.2-V Operation and 10x17 Endurance”
4:35 PM H. Kolke, Tokyo University, “ITMTJ STT-MRAM Cell Array Design with an Adaptive Reference Voltage Generator for Improving Device Variation Tolerance”
5:00 PM W. Kang, Baechang University, “Dynamic Reference Sensing Scheme for Deeply Scaled IT-MRAM”

Banquet 7:00 PM – 9:00 PM (provided)
Special Event: IEEE Reynold B. Johnson Information Storage Systems Award

Wednesday May 20, 2015
Registration 7:00 AM – 2:00 PM

Session #7 8:00 AM – 9:40 AM Solid State Disk
Chairs: Akira Goda, Micron, USA
Craig Swift, Freescale, USA

8:00 AM T. Iwasaki, Chuo University, “Machine Learning Prediction for 13+ Endurance Enhancement in ReRAM SSD System”
8:25 AM C. Matsui, Chuo University, “3x Faster Speed Solid-State Drive with a Write Order based Garbage Collection Scheme”
8:50 AM S. Okamoto, Chuo University, “Application Driven SCM/NAND Flash Hybrid SSD Design for Data-Centric Computing System”
9:15 AM Lorenzo Zusto, Università degli Studi di Ferrara, “LDPC Soft Decoding with Reduced Power and Latency in 1X-2X NAND Flash-Based Solid State Drives”
9:40 AM Break (Refreshments Provided)

Session #8 10:05 AM – 12:15 PM eNVM/New App
Chairs: Akira Goda, Micron, USA
Craig Swift, Freescale, USA

10:05 AM L. Luo, GLOBALFOUNDRIES, “Functionality Demonstration of a High-Density 1.1V Self-Aligned Split-Gate NMN Cell Embedded Into LP 40 nm CMOS for Automotive and Smart Card Applications”
10:30 AM S. Park, SK-Hynix, “Single-Poly Embedded NVM Solution For Analog Trimming And Code Storage Applications”
10:55 AM A. Baiano, NXP, “Junction optimization for embedded 40nm FinFET flash memory”
11:20 AM P. Amato, Micron, “An Analytical Model of eMMC Key Performance Indicators”
11:45 AM Lunch Break (on your own)

Session #9 2:00 PM – 3:40 PM CBRAM/PCM
Chairs: Takashi Kobayashi, Hitachi, Japan

2:00 PM W.S.Ko, Macrom “A Procedure to Reduce Cell Variation in Phase Change Memory for Improving Multi-Level-Cell Performances”
2:25 PM N. Ciochin, Politecnico di Milano, Universal thermoelectric characteristic in phase change memories
2:50 PM M. Barci, CEA-LETI, “Bilayer Metal-Oxide CBRAM technology for improved window margin and reliability”
3:15 PM A. Belmonte, IMEC, “Fast and Stable sub-10μA Pulse Operation in W/SiO2/ Ta/Cu 90nm 1T1R CBRAM devices”
3:40 PM Break (Refreshments Provided)

4:05 PM – 4:45 PM Closing Remarks & Adjourn