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Special Issue for

IEEE Transactions on Electromagnetic Compatibility

on 'PCB Level Signal Integrity, Power Integrity, and EMC'

Printed circuit boards (PCBs) are becoming the most fundamental interconnect element in computers, wireless mobile phones, high-definition displays, and high-density packages. However, the steadily increasing clock speeds and data transmission rates of these systems have resulted in inevitable challenges to PCB designers due to issues of PCB level signal integrity, power integrity, and EMC.

High frequency channel loss, reflection, and crosstalk are causing degradation of the receiver eye opening, jitter performance, and bit-error-rate. In addition, improper PCB design can lead to non compliance with EMC regulations. The growing popularity of mixed integration on the same PCB of noise sensitive RF and sensor chips with noisy digital chips has created significant PCB design challenges to suppress high frequency electromagnetic interference. High frequency electromagnetic interference can yield lower receiver sensitivity and performance degradation. In order to overcome these difficulties and achieve compatibility, there have been major advances in areas of PCB level modeling, design, and measurement with respect to signal integrity, power integrity, and EMC.

This special issue aims to highlight the recent progress on PCB Si/PI and EMC related issues. In particular, this issue is directed toward identifying areas of creative innovations and significant advancements related to not only fundamental improvements in modeling and measurement, but also novel design methodologies and new materials. Prospective authors are invited to submit original papers on their latest research results in the following fields:

- PCB level signal integrity
- High-speed channel modeling, design, and measurement
- Channel loss, ISI, and equalizer
- Jitter and eye estimation
- Crosstalk
- Carbon nanotube interconnects
- PCB level power integrity
- PDN modeling, design, and measurement
- Embedded passives and EBG structures
- PCB level EMC
- Electromagnetic emission modeling, design, and measurement
- Electromagnetic susceptibility modeling, design, and measurement
- Fast and efficient numerical approaches

Paper submission deadline: September 30, 2009

Planned publication date: May 2010

Authors are requested to submit papers up to 8 pages in length, including title, author's affiliation, abstract, figures and references. Please submit your manuscript on-line to the IEEE 'TEMC Manuscript Central' making it clear that it is for this Special Issue, by September 30, 2009. The website is http://mc.manuscriptcentral.com/temc-ieee/temc-ieee. All manuscripts are to conform to the *IEEE Transactions on EMC* Guidelines, see "Information for Authors". Due to page limitations a maximum number of about 20 papers will be published in this Special Issue, scheduled for May 2010.

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