



# Practical Papers, Articles and Application Notes

*Flavio Canavero, Technical Editor*

**A** new year. A new Technical Editor. During 2006, Professor Robert Olsen decided to leave this column and the EMC Society kindly asked me to take over in this position. I would like first to thank Professor Olsen for the meritorious work he has done during his many years of running this technical section and for having introduced me to this new job. Over the years, he passionately hunted for contributions of interest for the *Newsletter* readership, and he made this column very successful and appreciated by the Society members. I can only hope to be able to achieve the same results.

I will follow the footsteps of my predecessor, since I totally agree with the approach he adopted for the papers selection. Here, I repeat the policy statement that used to appear in the introduction of this column: "The purpose of this section is to disseminate practical information to the EMC community. In some cases, the material is entirely original. In others, the material is not new but has been made either more understandable or accessible to the community. In others, the material has been previously presented at a conference but has been deemed especially worthy of wider dissemination. While all material will be reviewed prior to acceptance, it is not necessary that the paper be original or archival; it is only necessary that the paper be useful and of interest to readers of the *Newsletter*."

While I will personally solicit contributions, I encourage all readers to actively participate to this column, either submitting manuscripts they deem appropriate or suggesting other authors who have something exciting to share with the EMC community. I will follow up on all suggestions, and

with the help of independent reviewers, I sincerely hope to publish enjoyable and instructive papers. Please communicate with me, preferably by e-mail at [canavero@ieee.org](mailto:canavero@ieee.org).

The articles of the current and next issues still represent the legacy of Professor Olsen; he invited the authors to contribute, and conducted the review process. I gladly endorse his decision since these papers have different characteristics and specific merits that make reading them worthwhile.

The first paper is entitled "PDN Design Strategies: IV. Sources of PDN Noise" by James L. Knighten, Bruce Archambeault, Jun Fan, Giuseppe Selli, Abhilash Rajagopal, Samuel Connor, and James L. Drewniak. This is the fourth in a series of papers they wrote on a very significant problem designers are facing in recent digital devices, where the border between Signal Integrity and EMC issues (that we used to consider separately) becomes blurred. The second paper is entitled "Electrocardiogram (ECG) Susceptibility to Interference from Popular Electronic Devices" by Matthew Pinchuk Meland and Anthony Dedes. The authors, at the time of writing, were Secondary II (Grade 8) students at West Island College in Montréal, Quebec, Canada, and this paper represents the report of research undertaken under the supervision of their teacher, Mr. Martin Bailly, as a Science Fair Project for which they were awarded the Gold Medal. The merit of this paper is to increase the awareness of EMI in the healthcare environment. Finally, the decision of publishing this contribution is not only to reward these students for their nice work, but also to stimulate the interest in and participation of youngsters to our electromagnetic compatibility discipline.

## PDN Design Strategies: IV. Sources of PDN Noise

*James L. Knighten<sup>1</sup>, Bruce Archambeault<sup>2</sup>, Jun Fan<sup>1</sup>, Giuseppe Selli<sup>3</sup>, Abhilash Rajagopal<sup>3</sup>, Samuel Connor<sup>2</sup>, and James L. Drewniak<sup>3</sup>*

### I. INTRODUCTION

This is the fourth in a series of articles on strategies for power distribution network (PDN) design for high-speed printed circuit boards (PCB). Previous articles addressed: (a) the importance of the specific capacitance values of decoupling capacitors to the overall effectiveness of decoupling of the PDN [1]; (b) the importance of the location of the decoupling capacitor to its decoupling effectiveness, i.e., global vs. local decoupling [2]; and (c) the importance of power/ground layer spacing, relative per-

mittivity, and dielectric loss to effective decoupling [3]. This article addresses sources of noise on the PDN; hence it departs somewhat from the overall discussion of noise suppression by effective decoupling. Nevertheless, knowledge of the characteristics of noise sources is important in achieving effective decoupling designs for PDN structures and in diagnosing PDN noise problems.

Noise induced on a PDN containing active digital devices, such as an integrated circuit (IC) is created by either (1) current being drawn from, or supplied to, the PDN as the IC switches between on and off states, or (2) by signals (or clocks) that are routed on a PCB in such a manner so as to change layers in the stack-up and in doing so, completely penetrate a plane pair (a power/ground power bus or some other pair of planes) and thereby excite the plane pair by causing the return current to jump

<sup>1</sup>NCR Corporation, San Diego, CA: [jim.knighten@ncr.com](mailto:jim.knighten@ncr.com) and [jun.fan@ncr.com](mailto:jun.fan@ncr.com)

<sup>2</sup>IBM Co., Research Triangle Park, NC: [barch@us.ibm.com](mailto:barch@us.ibm.com) and [sconnor@us.ibm.com](mailto:sconnor@us.ibm.com)

<sup>3</sup>University of Missouri-Rolla, Rolla, MO: [gs5xd@umr.edu](mailto:gs5xd@umr.edu), [arrh3@umr.edu](mailto:arrh3@umr.edu), and [drewniak@umr.edu](mailto:drewniak@umr.edu)

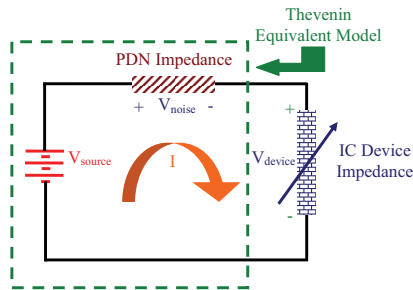


Figure 1: A digital IC is powered by a PDN. Changes between low and high states cause a changing current demand from the IC which causes the dc voltage across the IC to fluctuate. This voltage fluctuation is inevitable and represents an ac voltage ripple on the dc voltage level which is a source of ac noise on the PDN.

between planes. While these noise mechanisms are different, studies have shown that the relative levels of noise for either mechanism can be similar [4, 5, 6]. Therefore, both mechanisms should be included when estimating the noise on the PDN. The convention of referring to a pair of power and ground planes as a power bus and referring to an ensemble of power buses as a PDN is maintained.

## II. DECOUPLING NOISE DUE TO CURRENT DRAWN FROM THE POWER BUS

Between its power and ground pins, a digital IC and its load circuitry represents an impedance load to the PDN (and power bus) that varies with time as the IC switches states. This impedance is either high when the device is in the off-state, or low when the device is in the on-state. The resulting current drawn from the PDN is either low or high, respectively. As we have seen in previous articles, a goal of good decoupling is to lower the impedance of the PDN, but this impedance is always greater than zero. The voltage drop across the PDN impedance is either higher or lower, depending on the impedance state of the IC. If the IC changes states periodically, such as is the case with a clock, or periodic signal, the voltage drop across the PDN impedance,  $V_{noise}$  is also periodic and reduces the voltage across the IC power/ground pins pair,  $V_{device}$ , as seen in Figure 1. The voltage,  $V_{source}$  is the PDN source dc voltage that is used to power active devices on the PCB. DC voltage values are typically 3.3V, 5V, 1.8V, etc. The voltage across the power/ground pins of the IC device is

$$V_{device} = V_{source} - V_{noise} \quad (1)$$

$V_{noise}$  is sometimes referred to as an ac ripple voltage that is superimposed on the dc rail voltage that powers the power/ground plane pair. (In real cases, dc resistance can also reduce the dc voltage level at the IC device, but since our discussion focuses on ac noise voltages, this is ignored in this discussion.) This ac ripple voltage is switching noise. The ac ripple on the power bus, or PDN, which is due to digital IC switching, is inevitable. It cannot be avoided unless the impedance of the PDN is reduced to zero, which is unrealistic. For the same amount of current drawn from the PDN, the lower the impedance of the PDN, as seen in Figure 1, the lower the resulting ac noise voltage,  $V_{noise}$  that is generated.

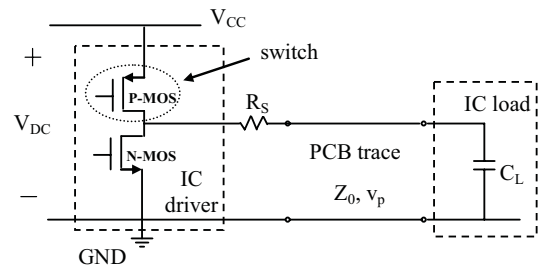


Figure 2: A typical totem pole CMOS IC output driver contains two complimentary field effect transistors (FET) between power ( $V_{CC}$ ) and ground. The IC load represents PCB traces and devices external to the IC or other circuitry within the IC.

The previous paragraph demonstrates that the PDN or power bus exhibits switching noise if it contains operating digital devices, regardless of the type and number of these devices. Power bus noise is inherent in the flow of current to and from the digital IC and cannot be avoided. This power bus noise may be reduced by designing the power bus/PDN in such a way as to lower the complex impedance (transfer- or self-) of the PDN through using thin power bus structures, effective decoupling, and specialized materials between power and ground planes [2, 3]. In general, as implied in Figure 1,  $V_{noise}$  is proportional to PDN impedance.

There are other mechanisms that can contribute power bus noise. The IC itself contains its own PDN that can suffer noise generation internally. Also, it is well-known that complex ICs can demand current more rapidly than some PCB PDNs are able to supply it. Neither of these two possible sources of additional noise is explicitly addressed in this work.

The IC has its own internal PDN that likely exhibits its own internal switching noise. This noise may escape the IC in the traditional ways that PCB switching noise escapes the PCB, i.e., direct radiation, crosstalk, PDN asymmetries that produce common-mode noise sources, etc. In cases where the IC is an aggressive producer of switching noise, often through unfortunate design choices, the presence of a low PDN impedance on the PCB may minimize the consequences of this noise being introduced on the PCB [3]. Isolation of the noise on an IC and prevention of its transfer to the PCB PDN requires careful design. Design techniques that may be appropriate to achieve effective isolation are not discussed in this work.

The analyses of previous paragraphs presuppose that the PDN has the ability to meet the timely current demands of the IC. A legitimate concern of circuit designers dealing with fast switching ICs is the ability of the power bus to supply sufficient current in a timely manner. It is generally accepted that failure to deliver enough current quickly enough is an undesirable condition. If the power bus cannot meet the IC's needs for sufficient current during the time of need, the IC may fail to function properly. Functional failure may produce altered signal and clock waveforms. The noise voltage generated by the device may be enhanced. During the time when current demands cannot be met, the impedance of the IC on the power bus may attain some value that is neither the on- nor the off-state value. Analysis of IC behavior in the state of current starvation is complex and beyond the scope of this article. All analyses presented in this

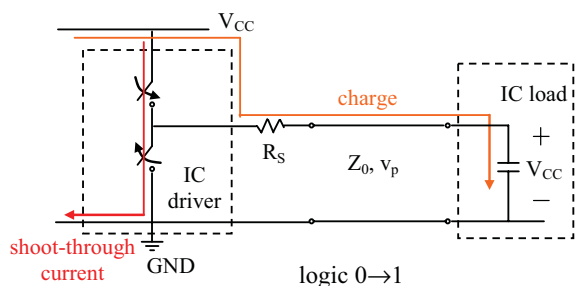


Figure 3: When the IC driver switches from low (Logic 0) to high (Logic 1), the upper transistor closes and the lower transistor opens. Current flows from  $V_{CC}$  to the IC load through the upper transistor. In addition, for a brief moment when both transistors are in transitioning states, they are simultaneously in low impedance states and shoot-through current flows from  $V_{CC}$  through the transistor pair to ground.

article are based on the assumption that sufficient charge is available when needed from the power bus.

## Decoupling Noise from ASIC/IC power pins

While it is common knowledge that some ASIC/ICs (application specific integrated circuit/integrated circuit) cause more noise problems than others, it has been traditionally difficult to predict the amount of noise created by the ASIC/IC.

Since current drawn from the power bus is a primary source of power bus switching noise, it is useful to focus on the current demands of the ASIC/IC when predicting the amount of noise on a power bus generated by that device. The resulting noise voltage depends on the power bus impedance at the point where the ASIC/IC power/ground pins are located. (Note that some design approaches for PDN design focus on targeting a maximum PDN impedance [1]).

When examining current drawn from the power bus by a digital ASIC/IC, it is useful to consider the configuration of common IC output drivers and the manner in which they make demands for current from the power bus. Figure 2 shows a typical “totem pole” output driver configuration for an I/O driver for a CMOS IC. (This paper is focused on I/O current.) When the output driver changes state from logic state 0 to logic state 1, the upper P-MOS transistor exhibits a low impedance and the lower N-MOS transistor exhibits a high impedance. Therefore, current flows from the IC’s power supply through the upper transistor out onto the load, shown as an external trace transmission line on the PCB in Figure 3. As the two transistors switch states, there is a moment when both transistors are in relatively low impedance states, which allows current to flow from the IC power supply directly to the ground-reference. This is usually referred to as “shoot-through current” and occurs during both the logic state 0-to-logic state 1 and also 1-to-0 transitions. As shown in Figure 4, there is no current required from the supply during the logic state 1-to-logic state 0 transition except the shoot-through current. Therefore, there are two important categories of current demanded from the power bus during switching: a load current demand, which occurs once during each clock cycle; and shoot-through current, which occurs twice during each clock cycle.

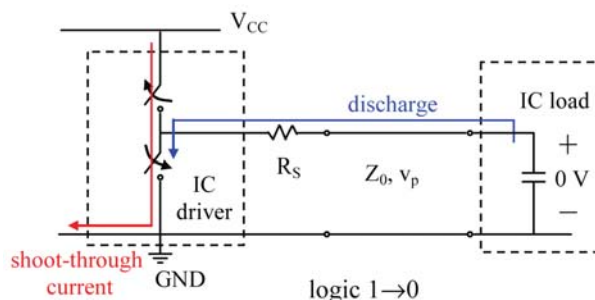


Figure 4: When the IC driver switches from high (Logic 1) to low (Logic 0), the upper transistor opens and the lower transistor closes. Current flows from the IC load through the lower transistor to ground. No load current flows from  $V_{CC}$ . Shoot-through current flows from  $V_{CC}$  through the transistor pair to ground in the same manner as in the opposite state transition in Figure 3.

The I/O current can often be found conveniently by using commercial signal integrity analysis software programs. Normally, signal integrity analysis software packages can be used to simulate voltage waveforms on various transmission lines. Many of these can also be used to find the current on the I/O trace. If complex analysis tools are not available, estimates of I/O current can be made for certain ASIC/IC types.

There are two general categories of ASIC/ICs to be considered when designing PDNs. Each produces its own frequency spectrum of noise generated at the IC’s power pins. First, some ASIC/ICs produce I/O currents that are repetitive, such as a clock signal. An example is the clock buffer, which typically produces a discrete frequency spectrum that includes a number of harmonics, with each harmonic frequency clearly defined. Second, large ASIC/ICs typically have many different I/O lines, both for data and address busses. The resulting signal on any single I/O line is not a regular bit pattern, like a clock, but is a bit pattern that will vary with time. Depending on the ASIC/IC, the I/O bit patterns are more akin to a pseudo-random bit pattern than a repetitive bit pattern. The current spectra of the typical large ASIC/IC are complex and may change from cycle-to-cycle.

For completeness, it must be noted that current demands by an ASIC/IC can come from different types of circuits in the device, not just the I/O circuits. Core circuits are used within the ASIC/IC for internal switching and processing. The current demand from core circuits can be complex and usually referred to as core current, which is not discussed in this paper.

Table 1: Clock buffer parameters.

	MPC905
$C_{PD}$	19.5 pF per output
$V_{CC}$	3.3 V
m (number of outputs)	6
n (number of loads)	6
f (operating frequency)	100 MHz
$t_r$ (20%-80%)	0.825 ns

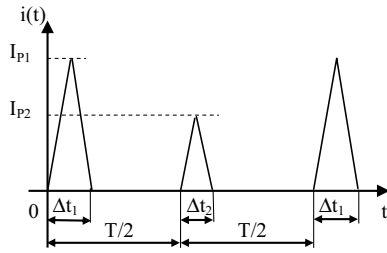


Figure 5: Power Pin Current Waveform for ASIC/ICs.

### Clock Buffer Current Demand

Clock buffers are an example of the ASIC/IC whose current demand is likely to be dominated by the I/O circuit current demand. While commercial modeling software tools can often simulate the current demand, not all designers have these available to them. Hence, there are alternative methods for estimating the current demand of devices dominated by I/O current (such as the clock buffer).

The total I/O current demand can be estimated by simply multiplying the individual trace current by the total number of active I/O lines. The most accurate technique for determining the pulse shape and to allow accurate determination of the frequency domain harmonic content of the current pulse is to use modeling software (typically, software intended to model the fidelity or integrity of the signal or the clock) which allows for inclusion of driver/receiver models (IBIS, for example). An alternative technique for estimating I/O current is to use a simple capacitive load method given by the following equation.

$$I_L = \frac{C_L n V_{cc}}{\Delta t_1 / 2} \quad (2)$$

where

$C_L$  = the capacitive load, normally about 10 pF for CMOS devices,

$n$  = the number of active loads,

$V_{CC}$  = the supply voltage, and

$\Delta t_1$  = the charging time of the load IC device, and can be approximated as the rise time (0-100% time to rise in the example).

The current pulse shape can be approximated as a triangular pulse with the peak amplitude found from Equation (2).

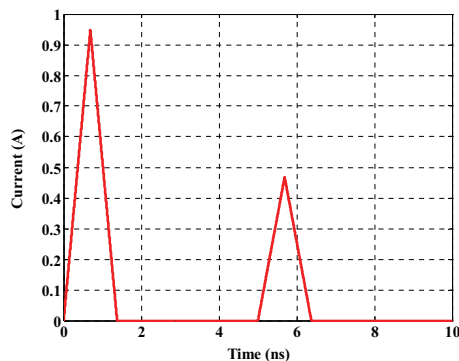


Figure 6: The total estimated I/O current for the MPC905 clock buffer during a single clock cycle includes both the load current occurring once per clock cycle and shoot-through current occurring twice per clock cycle.

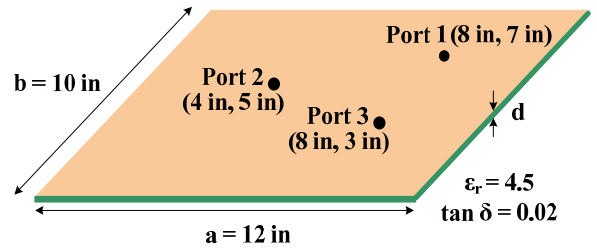


Figure 7: PCB configurations used for all calculations.

The width of the pulse at its base is assumed to be equal to the 0-100% rise time of the I/O voltage signal. While this method is not expected to be as accurate as a commercial analysis software tool with complex device models, this method can provide a reasonable estimate of the current demand.

For clock buffers and some other ICs, the peak amplitude of the shoot-through current can be estimated using a vendor data sheet parameter called power dissipation capacitance ( $C_{pd}$ ). Assuming the same triangular current waveform, the shoot-through current pulse amplitude is found from the following equation:

$$I_{p2} = \frac{C_{pd} * m * V_{cc}}{\Delta t_2} \quad (3)$$

where

$m$  = number of I/O drivers, and

$\Delta t_2$  = the switching time of the IC device, and can be approximated as the rise time (0-100%)

The total ASIC/IC I/O current is the sum of the shoot-through current and the load current. The simplified waveform for the total power current is shown in Figure 5, where the period of both the total current and the load current is  $T$ , and  $I_{p1} = I_{p2} + I_L$ .

As an example, this method of using the I/O load current and the  $C_{pd}$  parameter to predict the noise voltage at the IC power pins is applied to a standard clock buffer, the MPC905 clock buffer. Figure 6 shows the results for a clock buffer running at 100 MHz with a capacitive load of 10 pF. This device was placed on the 10 in. by 12 in. PCB (Figure 7) that has been

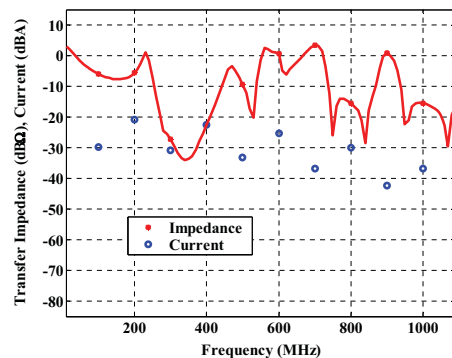


Figure 8: The transfer impedance,  $Z_{21}$  of the power bus PCB in Figure 7 and the MPC905 clock buffer current spectrum.

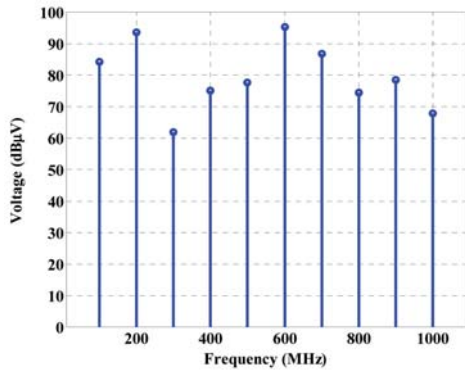


Figure 9: The predicted discrete noise voltage spectrum at port 2 of the PCB from Figure 7 caused by the MPC905 clock buffer.

used in previous articles in this series and analyzed using the cavity-mode analysis method discussed previously in this series [1-3, 7-9]. The power bus transfer impedances were calculated in the frequency domain in a manner identical to that seen in [1-3] to produce the plot of the magnitude of transfer impedance vs. frequency seen in Figure 8. The IC is placed at port 1. The noise voltage is observed at port 2. The frequency spectrum of the IC current drawn by the IC at port 1 is discrete and its magnitude is also shown in Figure 8. Both odd and even harmonics of the clock are present with significant amplitudes due to the asymmetry of the current waveform. The complex frequency spectrum of the current is multiplied by the complex transfer impedance between ports to produce a complex frequency domain voltage at port 2, whose predicted spectrum is also discrete and is seen in Figure 9.

While the cavity-mode modeling method is particularly suited to power bus modeling, power bus transfer impedances can be estimated using other means. A cursory examination of Figure 8 reveals that the transfer impedance is a complicated function. As such, simple equations are usually not sufficient to describe the impedance. A variety of full wave Maxwell's equations solvers can be used to calculate the power bus transfer impedance. In the restrictive case where the frequencies of interest lie below the lowest resonant frequency of the power bus, a simple capacitor model may suffice. The first resonant frequency of the cavity bus can be determined by:

$$f_r = 1 / 2a\sqrt{\epsilon\mu} \quad (4)$$

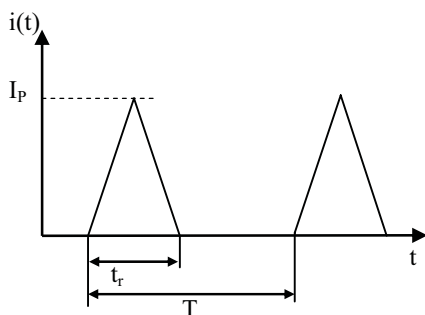


Figure 10: Estimated power current waveform (load current dominant, shoot-through ignored) for a large ASIC.

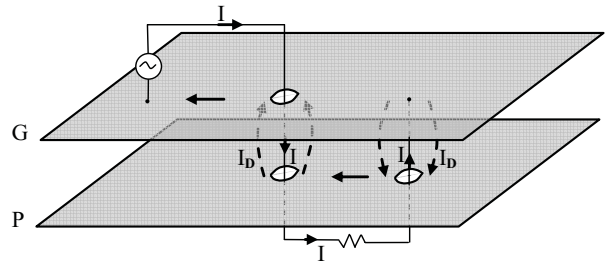


Figure 11: A common configuration of a plane pair penetrated by a signal line which excites the plane pair with a noise voltage. Return currents, especially at higher frequencies, follow the signal current path closely and can only return to the source through displacement current, which excite the plane pair.

where  $a$  = the largest dimension of the plane (in meters)  
 $\epsilon, \mu$  = permittivity and permeability of the power bus material  
 The  $C_{pd}$  parameter is available for some clock buffers and other ICs, but many IC clock buffer manufacturers do not specify this parameter. Depending on the complexity of the clock buffer, a first-order approximation can be made using the I/O drive current only. The agreement between measured and predicted values may not be as close as in the previous examples, but it is still an adequate estimation for many purposes.

A more detailed comparison of calculated and measured results for this and other ICs can be found in [10].

## Large ASIC/IC Current Demand

Design of large ASIC/ICs, such as processors, memory controllers, bus controllers, etc., require the manufacturer to do extensive simulations to insure the device operates properly. Major ASIC/IC manufacturers, such as IBM, Intel, ServerWorks, AMD, etc., create SPICE models to simulate the ASIC/IC under various load and operational conditions. Most of these SPICE models are developed for signal/data flow in the ASIC/IC, however, SPICE models are also created for the power requirements of the device. While ASIC vendors seldom provide these models (or the model results) to companies using these devices, these models can provide a very good indication of the power current requirements for large ASIC devices.

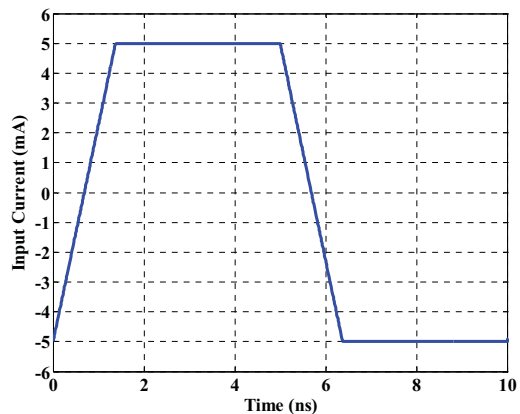


Figure 12: Input current for the clock signal applied to port 1.

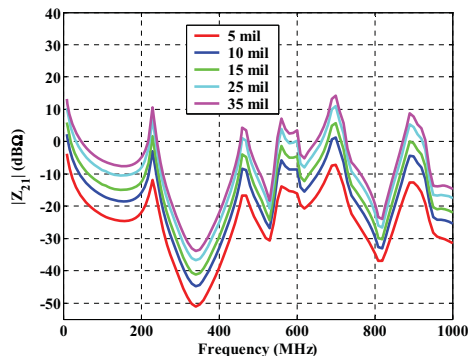


Figure 13: Magnitude of transfer impedance,  $Z_{21}$ , for the PCB in Figure 7 for five different plane spacings.

The most important consideration to estimating the noise associated with ASIC/IC power is to consider the current required by the ASIC/IC. Many ASIC/ICs have hundreds of pins, with one or more data/address busses. From one cycle to the next cycle, the specific I/O drivers that are turned ‘on’ change, but the overall number of drivers switching from logic state 0-to- logic state 1 tends to be statistically about half of the total number of drivers on that buss. This can provide a means for a rough approximation of the peak current demand by the ASIC/IC.

There are three levels involved to provide current to the I/O drivers when it is needed. The closest charge storage to the I/O driver is the capacitance on the silicon. Today’s ASIC technology provides approximately 750 pF of capacitance per square millimeter of silicon. This capacitance is the closest to the I/O drivers and therefore has the least inductance. However, the amount of charge stored in this on-chip capacitance is limited.

The next level of charge storage is contained within the ASIC package. Different manufacturers will have different numbers of discrete capacitors in the package, depending on cost, space availability, and data requirements. The remaining level of charge storage is on the PCB. This is the only level of charge storage that many PCB designers can affect.

A rough rule-of-thumb that is often used to estimate power current requirements is to assume that one-third of the total power consumption for that ASIC is associated with the time-varying current. For example, if the ASIC were a 60-watt device operating with a supply voltage of 2.5 volts, we would estimate that 20 watts of the power is time varying. For a first-order estimate, from a simple triangle current waveform (as in Figure 10) with the total pulse width twice the ASIC driver voltage output rise time, we can find the average current using the following relationship:

$$I_p = 2 \cdot \frac{I_{AVE} \cdot T}{t_r} \quad (5)$$

$$\text{where } I_{AVE} = \frac{P_{noise}}{V_{Supply}} \quad (6)$$

and  $t_r$  is the rise time of the output voltage.

In this example,  $P_{noise}$  which is the power consumption associated with the time-varying current, is 20 watts. With a 200 Mb/s waveform, the period,  $T$ , is 5 ns. The rise time,  $t_r$ , is 1 ns. This results in  $I_p = 80A$ .

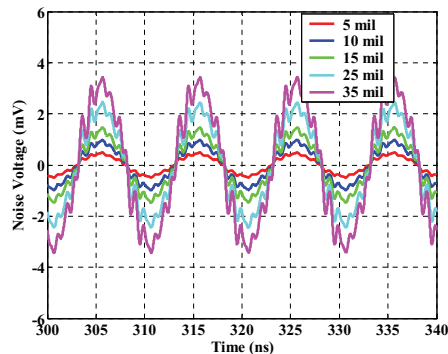


Figure 14: Noise voltage observed at port 2 for five different plane spacings.

Once  $I_p$  is determined, the frequency spectrum of the current waveform can be obtained from either a discrete Fourier series or an FFT. The impedance of the power/ground-reference plane structure can be determined in an identical manner to that used in the analysis of the clock buffer using cavity-mode analysis, or by other means of estimation. Once the estimated current and the power bus impedance is known, a calculation of the noise voltage created at the power pins can be made by multiplying the complex current by the complex impedance in the frequency domain. This calculated voltage provides a good first-order estimate. Note that the full complex current and impedance spectra must be used in order to determine the time-domain voltage waveform.

### III. VIA TRANSITION NOISE

Another source of noise generation on the power/ground plane pair is the power bus excitation that occurs when a signal or clock must be routed on multiple layers in a PCB and is forced to completely penetrate a plane pair in order for the signal or clock to run on a different layer. An example is seen in Figure 11. The return current for this signal or clock flows on the plane adjacent to the current trace and, because of the change in the plane carrying the return current, has no means of completing the return path other than to traverse the plane pair in the form of displacement current. (Note that an actual PCB will likely have decoupling capacitors connected between power and ground planes. These capacitors provide a path for some return current, but interconnection inductance often limits this to low frequency return current.) The potential difference between the planes due to the displacement current flow creates a voltage on the planes that is a noise voltage. Note that this phenomenon and the resulting noise voltage between the planes are independent of the schematic name for the planes, i.e., the planes do not always have to be power and ground. For example, this effect will occur between two planes labeled as VCC(5v) and VDD(2.7v), not just a power and ground plane pair.

This phenomenon is illustrated in an emulation based on the configuration in Figure 11. The PCB used in the emulation is seen in Figure 7. A clock current changes layers by means of a via and the return current must traverse the plane structure by means of displacement current. In the emulation, the via carrying a clock current at the location of port 1 is emulated by a trapezoidal clock current waveform of peak amplitude of 10 mA

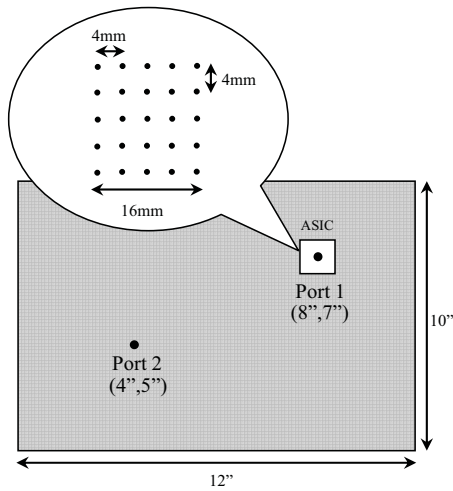


Figure 15: A large ASIC/IC placed on the PCB from Figure 7 has an array of pins that fit within a 16 mm square. Any of these pins may be power or ground pins.

between the two planes, seen in Figure 12. Using a cavity-model approach to model the plane pair, the transfer impedance between ports 1 and 2 is determined, as seen in Figure 13. Five different thicknesses,  $d$ , of the spacing between the two planes (5 to 35 mils) are examined. The transfer impedance is lower for small values of  $d$  than for higher values of  $d$  [3].

The resulting time domain ac noise voltage observed at port 2 is seen in Figure 14. The noise voltage has the same periodicity as the port 1 clock current. The amplitude of the noise voltage is higher for the larger plane spacing,  $d$ . The spectrum of the noise voltage at port 2 contains the same discrete frequencies as the input clock current at port 1.

The peak-to-peak noise voltages seen in Figure 14 increase substantially as the plane spacing,  $d$ , increases, which is consistent with the noise voltage being proportional to plane spacing over frequency. Increasing the plane spacing from 5 to 35 mils yields an increase in noise voltage of almost 17 dB. Doubling the plane spacing from its lowest value of 5 mils to 10 mils results in a 6 dB increase in ac noise voltage. Tripling the plane spacing from 5 to 15 mils results in almost 10 dB increase in ac noise voltage. Clearly, noise voltage induced by a via transition through a plane pair is greatly influenced by the spacing between the planes.

A 10 mA signal current on a trace is a value of current magnitude that is appropriate for many PCB situations. Resulting ac noise voltages of peak amplitudes between one and three mV is an indication that this noise mechanism is an important one that should be considered in PCB designs. The results in Figure 14 and Figure 9 can be compared, although one is a time domain voltage and the other a spectral plot of voltage. This example of via transition noise voltage is described in mV. The ASIC/IC induced noise from the clock buffer example has spectral components on the order of 100 dBmV (tenths of mV). While these comparisons are difficult to make precisely without both results described in the same domain, it can be said that, for these two examples, the via transition noise source appears to be as important a potential noise source on the power bus as is ASIC/IC current draw.

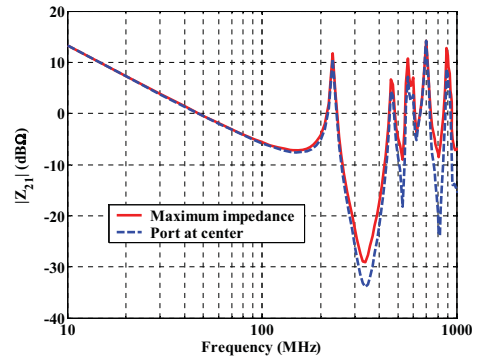


Figure 16: At any frequency that exhibits an impedance peak, the impedance at the center point in a grid under a 16 mm square ASIC is never more than approximately 5 dB lower than the maximum power-bus impedance at any point in a grid. Therefore, power-bus impedance for any power/ground pin pair may be estimated at the center point and adjusted upward by 5 dB to obtain a working estimate of maximum power-bus impedance seen by the ASIC/IC.

#### IV. EFFECTS OF LARGE ASICS AND POWER/GROUND PIN POSITION

Large ASIC/ICs typically have hundreds of pins for connection to the printed circuit board. Many of these pins are assigned as power or ground-reference pins and these pins are usually distributed across the entire ASIC. Previous articles in this series [1-3] have indicated how to determine the power bus impedance at any specific location on the PCB. Is it necessary to calculate the power bus impedance at each specific power/ground pin location on a large ASIC/IC, or is there a way to adjust the power bus impedance to account for the variations in location of power/ground pins under a large ASIC/IC?

The total noise voltage induced between the power/ground-reference consists of all the independent contributions due to the current drawn from each ASIC/IC pin. According to the investigation results presented in [11], the sum of all these contributions can be replaced by an equivalent current drawn located at the center of the ASIC/IC itself. Also, this assumption is shown to be accurate up to a frequency corresponding to ten times the diagonal length of the ASIC/IC device.

A study was conducted of the variations in power bus impedance experienced by a generic ASIC/IC that has a pin field 16 mm square placed on the same 10 x 12 inch PCB used in other examples (Figure 15). Cavity-mode analysis was used to calculate the power bus impedance at 25 locations equally spaced in a grid 4 mm apart within the 16 mm square pin field of the ASIC/IC.

Figure 16 shows a comparison of the maximum impedance at any of the 25 locations compared with the impedance at the location that is in the center of the 16 mm square area. Examining the peaks off the impedance curves (ignoring the valleys), the results indicate that the impedance at any location under the ASIC/IC is no more than 5 dB higher than the impedance at the center location, and often 2 dB or less. This indicates that a single estimation of power bus impedance under a large ASIC/IC may provide a sufficient basis to estimate the induced noise voltage on the power bus.

## V. DESIGN IMPLICATIONS

An important source of noise voltage on the power bus is the dominant active devices, i.e., ASIC/ICs. Designers of PCBs seldom have significant influence on the noise characteristics of the ASIC/IC, i.e., the number of decoupling capacitors placed either on the silicon within the package, placement of power/ground pins, or any other design features that could influence the noise properties of the device. Getting accurate information on the time-varying current requirements at the ASIC/ICs pins from the vendor is often either extremely difficult or impossible. Therefore, simple, fast, and reasonably accurate methods for generating an estimation that is suitable for making engineering PCB design decisions is very valuable.

Previous papers in this series have shown the effects of PCB plane separation, dielectric constant variation and decoupling capacitor location [1-3]. These papers focused on the response of the passive PCB without consideration of the amount of noise created by active devices. Lowering power bus impedance is the single, most effective, goal in reducing PDN noise. (Note that a low power bus impedance will not assure that an adequate amount of charge will be available to a specific ASIC/IC in a timely manner. The effects of charge starvation on a device and its associated contributions to power bus noise are not analyzed in this paper.)

With techniques indicated in this paper, it is possible to estimate the time-varying noise current source from an ASIC/IC. When the current is coupled with the techniques and methods from the previous papers referenced, the noise voltage created at the IC power pins can be estimated and the effects coupled with the known benefits of decoupling capacitor value, location, plane spacing, power bus dielectric constant, etc.

Power bus noise is caused by either device switching, or by a clock, or signal transitioning through power and ground layers with a via. When attempting to diagnose the source of power bus noise, the spectrum of the noise may provide a hint as to the dominant culprit.

When a device switches states, no matter whether it transitions from logic state 0-to-logic state 1 or the reverse, from logic state 1-to-logic state 0, shoot-through current flows from the power plane through the device to ground. Shoot-through current of a clock buffer, for instance, occurs twice during each cycle of the clock, at every rising and falling edge. Therefore, the noise voltage and current exhibits strong even harmonics of the clock frequency that the original clock waveform may not exhibit. Hence, observations of PCB EMI noise at even harmonics of clock frequencies indicate that the source of EMI noise is likely to be the power bus, rather than some other source. Many other sources of PCB EMI noise result in stronger odd harmonics than even harmonics.

For ASIC/ICs that have I/O circuits with relatively small load currents, the shoot-through current may dominate the total current drawn from the power plane by the device. In such cases, the generated power bus noise will have much stronger even harmonics than odd harmonics of the clock frequencies.

For ASIC/ICs with I/O circuits that have larger load currents, the shoot-through and load currents both exist in more balance than in the example in the previous paragraph. The load current, as shown in Figure 3, only occurs at the rising edges of the voltage waveform, which brings in the fundamental clock frequency and its odd harmonics into the noise spectrum. Even

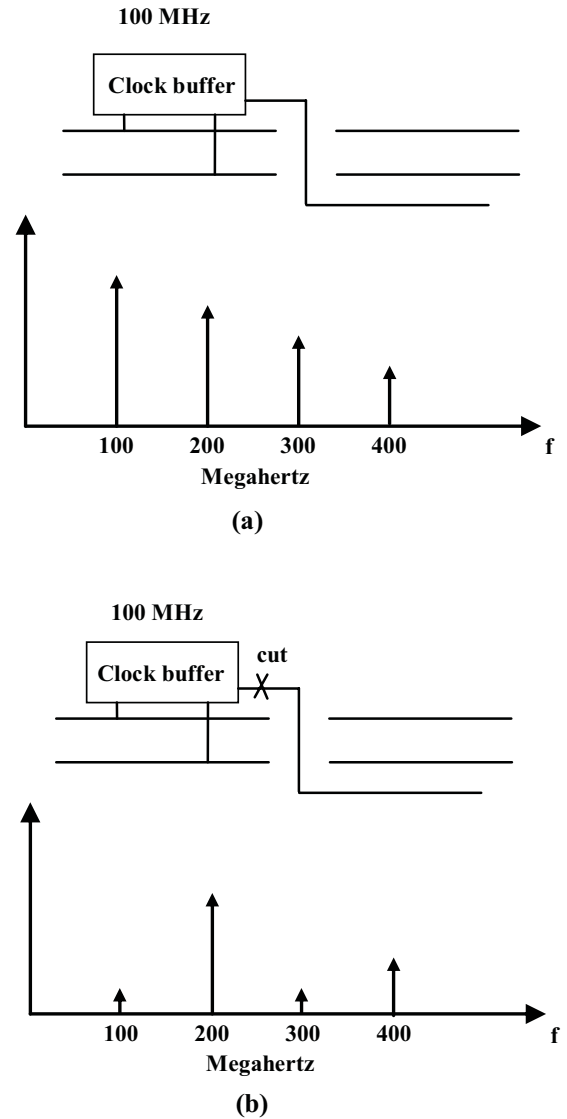


Figure 17: An example of diagnosing a PCB radiated emission spectrum to understand the source mechanisms.

harmonics result from shoot-through current. The distribution of energy among the odd and even harmonics may vary with the ratio of the shoot-through current to the load current; however, the magnitudes of the odd and even harmonics are generally in the same order.

Clock or other signals that transition (change layers) completely through a power/ground plane pair with a via can also generate noise on the plane pair. The current returns as a displacement current through the power/ground plane pair, which creates noise in the power bus. The generated noise will have the same frequency components as the signal being transferred through the via. For instance, if the clock has an approximately 50% duty cycle, the spectral components of the power bus noise have much stronger odd harmonics of the clock frequency.

The cause of the power bus noise can sometimes be divined by studying the noise spectrum for some simple cases. In reality, the noise spectrum might be complex due to multiple clocks, multiple devices, and data patterns. How-

ever, observing these spectrum characteristics might help identify the worst noise sources and point toward appropriate fixes.

As a case study based on an actual PCB design, Figure 17a shows a 100MHz clock buffer mounted on a multi-layered PCB. This case study is created in a way to be instructive, but is based on an actual EMI experience. The clock buffer I/O trace penetrates a plane pair as its trace changes layers. The PCB exhibits significant levels of radiated emissions at numerous frequencies. For this reason, investigations were undertaken to determine the sources of noise on the PDN. A decoupling capacitor on the primary power bus was removed in order to provide convenient power and ground connections to permit attachment with a voltage-sensing device, such as a spectrum analyzer. A measurement at the decoupling capacitor location with a spectrum analyzer and a probe connecting between power and ground can provide a good indication of the behavior of currents on the planes and, in this case, shows spectral peaks at 100 MHz, 200 MHz, 300 MHz, 400 MHz, etc. The 200 MHz spectral peak is relatively high in the sense that it is comparable to the level of the 100 MHz peak. This is consistent with the overall radiated emission profile observed. What are the mechanisms that cause this radiated noise and can anything be done to mitigate the problem? The first step in diagnosing the situation is to cut the clock I/O trace that penetrates the plane pair (or, temporarily reroute it with an external signal and return path so that it does not penetrate the plane pair). The resulting power bus measured spectrum is shown in Figure 17b, which shows that the fundamental and the other odd harmonics of the 100 MHz clock vanish, leaving a strong 200 MHz and other even harmonics in the power bus spectrum. What does this imply? The fundamental and odd harmonics of the clock in the spectrum are probably caused by the clock I/O via transition through the plane pair. (The clock waveform has half-wave symmetry so that it only has odd harmonics.) The remaining even harmonics are probably caused by shoot-through current in the clock buffer (frequency doubling). Notice that we have not identified the function of the planes, i.e., power, ground, etc., nor do we need to know their function to understand the noise generation mechanisms. What, then, are some noise mitigation strategies?

#### Possible Via Transition Noise Mitigation Strategies:

- Reroute the clock I/O line so that it does not penetrate the entire plane pair and, hence change reference planes for the return current.
- Alter the PCB stack-up so that the plane spacing,  $d$ , is smaller [3].
- Locate one of the decoupling capacitors to be near the clock I/O signal via to assist the flow of return current. Some refer to these capacitors as “reference” capacitors in that the intended benefit is more complex than that of a capacitor whose sole intended function is to lower power bus impedance. This is usually effective only over a limited frequency range.

#### Possible Shoot-Through Current Noise Mitigation Strategies:

- Select a different clock buffer that exhibits less shoot-through current noise (lower  $C_{pd}$  value).
- Add decoupling capacitors in the vicinity of the IC. The effectiveness of this is dependent on power bus thickness [2].

- Lower the inductance associated with the decoupling capacitors. In other words, provide lower interconnect connections, lower inductance pads and maybe lower ESL capacitors.
- Alter the PCB stack-up so that the plane spacing,  $d$ , is smaller [3].

#### Possible ASIC/IC Load Current Noise Mitigation Strategies:

- Add decoupling capacitors in the vicinity of the IC. The effectiveness of this is dependent on power bus thickness [2].
- Lower the inductance associated with the decoupling capacitors. In other words, provide lower interconnect connections, lower inductance pads and maybe lower ESL capacitors.
- Alter the PCB stack-up so that the plane spacing,  $d$ , is smaller [3].

Notice that in all cases, reducing the plane spacing,  $d$ , is a design strategy. In fact, it is the most powerful noise reduction technique available [3]. But, PCB designers may not always have the luxury of altering a PCB stack-up to provide a closely spaced plane pair. When they do have that flexibility, reducing plane spacing should be a design priority.

## VI. SUMMARY & CONCLUSIONS

There are two important potential sources of ac noise on the power bus of a PCB containing digital circuitry. The current requirements of ASIC/ICs can induce significant noise onto the planes. In addition, running signals or clocks through a via that penetrates a plane pair can also induce noise into the planes that may be comparable in magnitude to the noise induced by an ASIC/IC.

The time-varying current demand from large ASIC/ICs are difficult to predict, but a simple, rough approximation can be made based on a power consumption model. The time-varying current demand from ASIC/ICs of the clock buffer type can be made by estimates based on device capacitances. The ac noise voltage created by signal via transitions can be calculated based on estimates of the transfer impedance of a plane pair multiplied by the return current through the plane pair. AC noise generation by via transition does not require that the two planes be used for power and ground.

The nature of ASIC/IC shoot-through current occurring twice per cycle creates a noise spectrum on the power bus that doubles the frequency of the ASIC/IC. This fact can provide a powerful diagnostic tool in examining and understanding PCB noise characteristics.

Keeping plane spacing small is a powerful noise generation mitigation method for every noise generation mechanism discussed in this paper. Keeping the inductance associated with capacitors across the plane pair low is another important noise generation mitigation method.

## VII. REFERENCES

1. Knighten, J., B. Archambeault, J. Fan, G. Selli, S. Connor, J. Drewniak, “PDN Design Strategies: I. Ceramic SMT Decoupling Capacitors – What Values Should I Choose?,” *IEEE EMC Society Newsletter*, Issue No. 207, Fall 2005, pp. 46-53.
2. Knighten, J., B. Archambeault, J. Fan, G. Selli, L. Xue, S. Connor, J. Drewniak, “PDN Design Strategies: II. Ceramic SMT Decoupling Capacitors – Does Location Matter?,”

*IEEE EMC Society Newsletter*, Issue No. 208, Winter 2006, pp. 56-67.

3. Knighten, J., B. Archambeault, J. Fan, G. Selli, L. Xue, S. Connor, J. Drewniak, "PDN Design Strategies: III. Planes and Materials – Are They Important Factors in Power Bus Design?," *IEEE EMC Society Newsletter*, Issue No. 210, Fall 2006, pp. 58-69.
4. Hubing, T., T. Van Doren, F. Sha, J. Drewniak and M. Wilhelm, "An Experimental Investigation of 4-Layer Printed Circuit Board Decoupling," *IEEE International Symposium on Electromagnetic Compatibility*, August 1995, pp. 308-312.
5. Fan, Jun, James L. Drewniak, James L. Knighten, Norman W. Smith, and Antonio Orlandi, Thomas P. Van Doren, Todd H. Hubing, and Richard E. DuBroff "Quantifying SMT Decoupling Capacitor Placement in DC Power-Bus Design for Multi-Layer PCBs," *IEEE Transactions of Electromagnetic Compatibility*, Vol. 43, No. 4, November 2001, pp. 588-599.
6. Cui, Wei, Xiaoning Ye, Bruce Archambeault, Doug White, MinLi, and James Drewniak, "EMI Resulting from Signal Via Transitions through the DC Power Bus," *IEEE International Symposium on Electromagnetic Compatibility*, August 2000, pp. 821-826.
7. Okoshi, T., "Planar Circuits for Microwaves and Lightwaves," Springer-Verlag Berlin Heidelberg, 1985.
8. Lo, Y., D. Solomon, W. Richards, "Theory and experiment on microstrip antennas," *IEEE Trans. Antennas and Propagation*, vol. 27, pp. 137-145, March 1979.
9. <http://www.ems-plus.com>
10. Mao, Jingkun, Bruce Archambeault, James L. Drewniak, and Thomas P. Van Doren, "Estimating DC Power Bus Noise," *2002 IEEE International Symposium on Electromagnetic Compatibility Symposium Record - Volume 2*, Minneapolis, MN, Aug. 19-23, 2002, pp. 1032-1036.
11. G. Antonini, J. L. Drewniak, M. Leone, A. Orlandi, and V. Ricchiuti "Statistical approach to the EMI modeling of large ASICs by a single noise-current source", in *Proc. of EPEP*, Princeton, NJ, October 2003

## Biographies



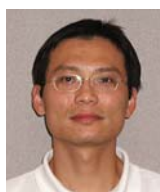
**James L. Knighten** (S'62-M'77-SM'97) received his B.S. and M.S. degrees in electrical engineering from Louisiana State University in 1965 and 1968, respectively, and his Ph.D. degree in electrical engineering from Iowa State University in 1976. He is employed by the Teradata Division of NCR Corporation in San Diego, CA where he works on EMI, and signal integrity design and testing of high-speed digital signal transmission systems in massively parallel processing computing systems. Prior to joining NCR, he worked for Maxwell Technologies, Inc., where he was engaged in the design of hardened electronic systems against the effects of the electromagnetic pulse created by nuclear weapon detonation, EMI, lightning, and high-powered microwaves on electronic systems.

He has authored numerous technical papers on topics involving various aspects of electromagnetics and taught short courses on electromagnetic pulse effects and electronics survivability both in the USA and in Europe. He is a member of the IEEE EMC Society.



**Bruce Archambeault** (M '85, SM '99, F '06) is an IBM Distinguished Engineer at IBM in Research Triangle Park, NC. He received his B.S.E.E degree from the University of New Hampshire in 1977 and his M.S.E.E degree from Northeastern University in 1981. He received his Ph.D. from the University of New Hampshire in 1997. His doctoral research was in the area of computational electromagnetics applied to real-world EMC problems.

Dr. Archambeault has authored or co-authored a number of papers in computational electromagnetics, mostly applied to real-world EMC applications. He is currently a member of the Board of Directors for the IEEE EMC Society and a past Board of Directors member for the Applied Computational Electromagnetics Society (ACES). He has served as a past IEEE/EMCS Distinguished Lecturer. He is the author of the book "PCB Design for Real-World EMI Control" and the lead author of the book titled "EMI/EMC Computational Modeling Handbook".



**Jun Fan** (S'97-M'00-SM'06) received his B.S. and M.S. degrees in Electrical Engineering from Tsinghua University, Beijing, China, in 1994 and 1997, respectively. He received his Ph.D. degree in Electrical Engineering from University of Missouri-Rolla in 2000.

He currently is an employee of the Teradata division of NCR Corporation in San Diego, CA, and serves as a Senior Hardware Engineer. His research interests include signal integrity and EMI designs in high-speed digital systems, dc power-bus modeling, PCB noise reduction, differential signaling, and cable/connector designs. He received the Conference Best Paper Award from the Applied Computational Electromagnetics Society in 2000.



**Giuseppe Selli** (S '00) received his Laurea degree from the University of Rome "La Sapienza" in June 2000. In January 2002, he joined the Electromagnetic Compatibility research group at the University of Missouri Rolla and he received his Master of Science Degree in Electrical Engineering in November 2003 with a thesis on "Time domain extrapolation and evaluation of surface-mount component parasitic inductance". He is a Ph.D. Candidate at the Electrical Engineering Department of the University Missouri-Rolla within the EMC Group. From May 2005 to December 2005, and from May 2006 to August 2006, he was at the IBM T.J. Watson Research Center on a co-op/intern program within the High Speed Electrical/Optical Packaging Group. His research interests include signal and power integrity issues.



**Abhilash Rajagopal** (S '00) received his B.E. degree in Electronics and Communication Engineering from Bharathiyar University, Tamilnadu, India, in 2003 and received his M.S. degree in Electrical Engineering at the University of Missouri-Rolla. He is currently pursuing his M.S degree in Computer Engineering at the University of Missouri-Rolla. He is a graduate

research assistant in the Electromagnetic Compatibility Laboratory, University of Missouri-Rolla. His main research interests are in the area of signal integrity and loss characterization.



**Sam Connor** (M '05) received his BSEE from the University of Notre Dame in 1994. He currently works at IBM in Research Triangle Park, NC, where he is a senior engineer responsible for the development of EMC and SI analysis tools/applications. Mr. Connor has co-authored several papers in computational electromagnetics, mostly applied to decoupling and high-speed signaling issues in PCB designs.



**James L. Drewniak** (S '85, M '90, SM '01, F '07) received B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Illinois at Urbana-Champaign in 1985, 1987, and 1991, respectively.

He joined the Electrical Engineering Department at the University of Missouri-Rolla in 1991 where he is one of the principle faculty in the Electromagnetic Compatibility Laboratory. His research and teaching interests include electromagnetic compatibility in high-speed digital and mixed signal designs, electronic packaging, and electromagnetic compatibility in power electronic based systems.

---

# Electrocardiogram (ECG) Susceptibility to Interference from Popular Electronic Devices

*Matthew Pinchuk Meland and Anthony Dedes, West Island College – Secondary II (Grade 8), Montréal, Quebec, Canada*

## Abstract

This experiment investigates the susceptibility of an ECG machine to emissions from unintentional emitters such as a GameBoy™ and iPod Nano™, and intentional emitters such as a Cell Phone, Portable 2.4 GHz Phone, Portable 5.8 GHz Phone and Walkie-Talkie. Experiments were conducted both in a “lab” and hospital environments. The authors demonstrate that all of the above popular electronic devices can interfere with an electrocardiogram (ECG) and corrupt the readings. Heartbeat changes ranging from 14 to 28 beats per minute were recorded due to EMI from these devices. Although Doctors and Medical Technicians have been alerted to the possibility of interference from intentional emitters, they are generally unaware that popular unintentional emitters can corrupt their equipment. These results clearly illustrate the need for including both intentional and unintentional emitters in the EMI control of hospitals, medical offices and home care environments.

## I. Introduction

It is well known that electromagnetic field emitters can interfere with medical equipment; consequently wireless communication devices are not permitted in hospitals or Doctor's Offices. Notwithstanding, some hospitals are challenging the extent of interference and are considering removing their bans on telecommunication devices [1]. In this research, the authors verify whether portable telecommunication devices (intentional emitters) interfere with medical devices; furthermore, they investigate if popular unintentional emitters such as a Game-Boy™ and iPod Nano™ can also cause interference.

Home care is becoming more and more common, and people are relying on medical equipment for either monitoring, medicating or relieving medical conditions. Generally people are not aware of the possibility that popular electronic devices can interfere with their medical equipment. Patients are generally

not warned which home electrical equipment should, or should not, be used in proximity of the medical device. In the home setting EMI from many intentional and unintentional emitters can result in faulty operation of the medical device and possibly lead to grave consequences for the home care patient.

Even in a hospital environment a kid in a children's hospital may be monitored for a long period of time, during that time the child may choose to listen to music on his iPod™ or play GameBoy™: Possibly, when he presses the “A” button to shoot the bad guy, his heart rate monitor goes crazy which can set off an unnecessary alarm and trigger an emergency response. Are these possible stories or just myths?

## II. Background Information

### A. Electrocardiogram

In 1791, the scientist Luigi Galvani discovered that electricity could make a muscle contract. The body emits electrical currents. The heart is the muscle that receives the most currents to make it contract. The skin is an isolator and therefore people do not feel these small electric currents. An Electrocardiogram uses sensitive conductors to detect these currents, amplifies them and displays them on a screen as well as calculating the heart beat rate. There is a universal system for this machine, every second, the line on the graph moves 12.5mm and for every millivolt recorded by the ECG, it grows by 5 mm.

In the Operating room there is often an electromagnetic field of electronic strength of 30V per meter or higher: In certain medical procedures it is common that the ECG makes unrealistic readings of the heart. The doctors at that time must guess if the patient's heart is functioning correctly or not.

### B. EMI and Medical Devices

The standard of electromagnetic shielding for medical equipment applies to all medical devices that operate at frequencies

ranging from 26 KHz to 1GHz. They must be shielded against an electromagnetic field up to 3V per meter. Those standards do not even apply to ECGs [2]. The army has much higher and more restrictive EMI standards and possibly if they would be adopted for hospitals, there would be much less interference [2].

It is very complicated to shield a medical device whose job is to measure the heart's electrical current produced to make it contract and pump the blood. The ECG has to pick up small currents. The ECG leads and electrodes can pick up an interfering electromagnetic field or the field may interfere directly with the monitor circuitry; consequently, the interfering currents can combine with the reading for the heart's real pulse. As a result, the heartbeat may appear to be either totally corrupted or have a normal appearance with a wrong value. This faulty operation will continue until the interfering electrical device is removed, which may not be for a very long time period.

For interference between two objects, the following conditions must apply:

- There must be a source that creates electromagnetic energy.
- There must be an object susceptible to the EM energy.
- There must be a physical relationship between the two objects, which means, they must share the same electromagnetic energy.

### III. Experiment

The experiment was performed in a secluded cabin - an environment that is less polluted with electromagnetic waves than in the city. All electrical equipment in the cabin was turned off. A Silogic EC60 Four lead ECG was used for the experiment. The potential interfering devices used during the test were: a Portable Telephone at 5.8 GHz, a Portable Telephone at 2.4GHz, a Cell Phone, a GameBoy Advance SP™, an iPod Nano™, and a Walkie-Talkie. The experiments were conducted over a period of several days.

The following experimental procedure was used:

1. For the initial setup, the four ECG leads were applied to Anthony while Matthew examined the ECG display for interference. The electrodes were placed with one on each inner thigh and one below each shoulder. If ambient interference was noticed, then the ECG was moved within the cabin to a place that did not show any interference.
2. For each potentially interfering device under test, the leads were applied to Anthony and the ECG control was positioned ON.
3. Each electrical device, one by one, was placed at a distance of 15 cm away from the ECG. Then the device was moved over a period of 45 seconds to try to get interference. For all the devices with antennas, the antenna was pointed towards the ECG and the opposite way.
4. The ECG display was video taped and heart beat readings were recorded.

The interfering devices were tested as follows:

1. Portable Phones that ring due to an outside call. Both 2.4 and 5.8 GHz phones were tested. The chargers (base stations) for the phones were placed 2m from the ECG.
2. A Cell Phone that rings due to an outside call.
3. A GameBoy™ that is ON but with nobody playing it.
4. An iPod Nano™ that is ON at maximum volume. The earphones were moved around the ECG and its leads without

touching them.

5. A Walkie-Talkie that rings in response to a page.

### IV. Experiment Results

Figures 1(a)-1(d) show typical ECG displays with and without interference. Table 1 lists the recorded Heartbeats with and without the various interfering devices energized. Figure 1 shows that in these cases, the EMI caused the ECG heartbeat to change; however, the waveform retained a normal appearance.

Device	iPod Nano™	Cell Phone	Portable Telephone 2.4 GHz	Walkie-Talkie	GameBoy™ Advanced SP	Portable Telephone 5.8Ghz
Heartbeat*	67→81	61→74	58→73	67→95	65→90	52→77
Change in Heartbeat	+14	+13	+15	+28	+25	+25 →

\* Heartbeat recorded in beats per minute. Device OFF  
Device ON

Table 1: Recorded changes in ECG heartbeats due to interference from popular electronic devices.



Figure 1(a): ECG with GameBoy™ OFF.



Figure 1(b): ECG with GameBoy™ ON.



Figure 1(c): ECG with iPod™ OFF.



Figure 1(d): ECG with iPod™ ON

## V. On-Site Hospital Experiment

Matthew had the occasion to further test their results at the Montreal Children's Hospital. During a routine Cardiology appointment he had to undergo an ECG test. Seizing the opportunity, he asked the Medical Test Technician if, after the test, he could experiment by using his GameBoy™ to try to interfere with the ECG (Hewlett Packard Model #M1700A). The technician's reply was "Sure, but you won't get any interference because only a cell phone can interfere with an ECG." As shown in Figures 2(a) and 2(b), there was a considerable amount of interference caused by the GameBoy™. Later on, he showed his results to the Cardiologist and the doctor's reply was, "Thank you very much for telling me this, I never knew that a GameBoy™ could interfere with an ECG."

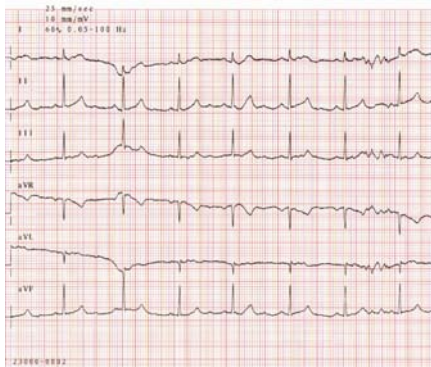


Figure 2(a): Hospital ECG GameBoy™ OFF.

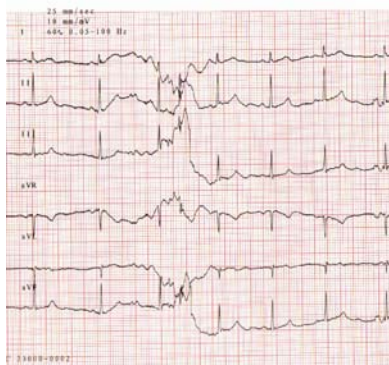


Figure 2(b): Hospital ECG GameBoy™ ON.

## VI. Conclusion

We proved through our experiments that modern hospital equipment, in particular the ECG, is susceptible to electromagnetic interference from many different popular electronic

devices including unintentional emitters such as a GameBoy™ and iPod Nano™. Doctors and Medical Technicians are not aware of these sources or interference that can lead to equipment malfunction. According to the signage in the hospitals we have visited, iPods™, GameBoys™ and even the GameBoy™ Advance DS (with wireless) are not banned. Especially in a Children's Hospital kids will play these games or listen to their iPod™ to pass time while undergoing lengthy tests and procedures. Air Lines know that these devices should not be used during critical operations. Now we are proving that the same applies to Hospitals, Home Care and Doctor's Offices.

## References

- [1] Emerson, Dan. Hospitals wheel in wireless future. Address URL: <http://www.bizjournals.com/twincities/stories/1999/03/08/focus2.html>
- [2] Institute of Biomedical Engineering Technology. Electromagnetic Interference: Causes and Concerns in the health care environment. Address URL: <http://ibet.asttbc.org/emi.htm>
- [3] White, Don. Magnetic fields and electromagnetic shielding Address URL: <http://www.magnetic-shield.com/faq/interference.html>
- [4] Encyclopaedia Britannica, Inc. Science and Technology: The World Around Us. Volume 9. Chicago, US. Encyclopaedia Britannica, Inc. 1983, 1151p.

## Acknowledgements

We would like to thank Merck Frosst for lending us the ECG Machine and Mary Panneton, at Merck Frosst, for arranging to get us the machine and teaching us how to use it. We would also like to thank Mr. Bailly, our Science Teacher at West Island College, for his guidance throughout this Science Fair Project. Finally, we would like to thank Dr. Amy Pinchuk for helping us with electromagnetics and editing this article.

## Biographies



**Matthew Pinchuk Meland**, born September 11, 1991, at the time of writing was a Secondary II (Grade 8) student at West Island College in Montreal, Quebec, Canada. This research was undertaken under the supervision of his teacher, Mr. Martin Bailly, as a Science Fair Project for which he and Anthony Dedes were awarded the Gold Medal. Matthew was introduced to EMC through his mother, Amy Pinchuk, and has attended the IEEE EMC Society Children's Workshops. Matthew's other interests include horseback riding, stamp collecting and skiing.



**Anthony Theodore Dedes**, born December 6, 1991, at the time of writing was a Secondary II (Grade 8) student at West Island College in Montreal, Quebec, Canada. This research was undertaken under the supervision of his teacher, Mr. Martin Bailly, as a Science Fair Project for which he and Matthew Meland were awarded the Gold Medal. Anthony's other interests include basketball and snowboarding.

EMC