

IEEE Circuits and Systems (CAS) Distinguished Lecturer Program (DLP)

Table 1 shows the contact information and term of the current IEEE Circuits and Systems (CAS) DLP speakers.

The remainder of this document includes the abstract(s) of the Distinguished Lectures, and speaker biographies.

If you are interested in inviting a DLP speaker to your region, please get in touch with your IEEE-CAS chapter chair. Your chapter chair will contact the DLP chair to make arrangements for sponsoring a DLP lecture. The current DLP chair is Tuna B. Tarim (tuna@ti.com). Please remember to check the DLP website for the latest updates: <http://www.ieee-cas.org>.

Distinguished lecturer	E-mail address	Term
Andreas G. Andreou	andreou@jhu.edu	2007-2008
Bert Shi	eebert@ee.ust.hk	2007-2008
Christian Schlegel	schlegel@ece.ualberta.ca	2007-2008
Corey Cheng	coreyc@miami.edu	2008-2009
Chua-Chin Wang	ccwang@ee.nsysu.edu.tw	2008-2009
David Z. Pan	dpan@ece.utexas.edu	2008-2009
Dinesh K. Bhatia	dinesh@utdallas.edu	2007-2008
Gerald E. Sobelman	sobelman@umn.edu	2008-2009
Georges G.E. Gielen	Georges.Gielen@esat.kuleuven.be	2008-2009
Hubert Harrer	hharrer@de.ibm.com	2007-2008
Huifang Sun	hsun@merl.com	2008-2009
John G. Harris	harris@cnel.ufl.edu	2008-2009
Kai-Kuang Ma	ekkma@ntu.edu.sg	2008-2009
Nam Ling	nling@scu.edu	2007-2008
Naveen K. Yanduru	n-yanduru1@ti.com	2007-2008
Sudhanshu Shekhar Jamuar	ssjamuar@eng.upm.edu.my	2008-2009
Tobi Delbruck	tobi@ini.phys.ethz.ch	2007-2008
Wallace Tang	kstang@ee.cityu.edu.hk	2007-2008
Zhiping Lin	ezplin@ntu.edu.sg	2007-2008
Zixiang Xiong	zx@ece.tamu.edu	2008-2009

Table 1: Current Distinguished Lecturer names, e-mail addresses, and terms being served.

Lecture abstract(s) and speaker biographies
(in alphabetical order of speaker name)

- **Andreas G. Andreou:**

Not available!

- **Bert Shi:**

Lecture #1: Bioinspired CNN visual systems

Depending upon the interest of the audience, this talk could have two flavors. One flavor is tutorial: its goal is to provide the audience with a snapshot of the current state of the art and research trends. It is based upon material presented during the tutorial organized by Csaba Rekeczky, Marco Gilli and myself at the CNNA Workshop in 2006. I consider a cellular neural/nonlinear network (CNN) as any spatial arrangement of mainly locally-coupled cells, where each cell is a dynamical system which has an input, an output and a state that evolves according to some prescribed dynamical laws. I cover a wide swath of of CNN research: From theoretical analysis of CNN dynamics, VLSI implementation and system level applications. The other flavor is more research oriented: Covering the development of multi-chip or multi-processor CNN systems inspired by the multi-dimensional selectivity in primary visual cortical neurons. I describe and compare two neuromorphic systems that model such neurons. The first is a low-power high speed system consisting of multiple mixed analog-digital CNN chips which communicate via spikes transmitted using the AER protocol. The second is a more rapidly reconfigurable DSP/FPGA hardware platform that also supports real-time implementation, but with higher power consumption. I describe visual processing applications enabled by these systems.

Speaker's biography: Bertram E. Shi (S'93-M'95-SM'00-F'01) received the B.S. and M.S. degrees in electrical engineering from Stanford University and the Ph.D. degree in electrical engineering from the University of California at Berkeley. He then joined the faculty of the Department of Electrical and Electronic Engineering at the Hong Kong University of Science and Technology. Dr. Shi's research interests are in bio-inspired and neuromorphic engineering, analog VLSI and cellular neural networks, machine vision, and image processing. He has served as a Distinguished Lecturer for the IEEE Circuits and Systems Society, an Associate and Guest Editor for the IEEE Transactions on Circuits and Systems-I, Secretary and Chair for the IEEE Circuits and Systems Society Technical Committee on Cellular Neural Networks and Array Computing and the Student Activities Chair of the IEEE Hong Kong Section.

- **Christian Schlegel:**

Lecture #1: Iterative demodulation and decoding: A new communications paradigm

With the invention of Turbo Coding, iterative processing has started its inexorable march towards domination in the field of communications signal processing. In order to underpin this claim, we present the basics and applications of iterative processing to demodulation and decoding for linear vector channels, such as code-division multiple access (CDMA), intersymbol-interference channels (ISI), and multiple-input multiple-output (MIMO) channels, among others. We show how iterative processing is applied to these channels, and how simple, yet effective cancellation structures emerge as the key processing elements. These elements find ready implementations in efficient FPGA and ASIC structures, and we present such implementation results. We also show how error control coding forms a natural component in this new methodology, and how the preferred implementation immediately and naturally decomposes into a demodulation and a (conventional) error control functionality. We present results of this methodology applied to CDMA and MIMO, and show how it gives rise to the concept of partitioned spreading, which we will show to be capacity achieving. Examples of other applications, such as on intersymbol-interference channels where large performance gains can be obtained with respect to the current DFE/FEC strategy, are also discussed. We round this presentation off with known results on optimality and efficiency, the state-of-the-art of implementing such complex circuits, as well as with open questions currently under investigation.

Speaker's biography: Christian Schlegel received the Dipl. El. Ing. ETH degree from the Federal Institute of Technology, Zurich, in 1984, and the M.S. and Ph.D. degrees in electrical engineering from the University of Notre Dame, Notre Dame, IN, in 1986 and 1989.

Dr. Schlegel held academic positions at the University of South Australia, the University of Texas and the University of Utah, Salt Lake City. In 2001 he was appointed chaired Professor for Digital Communications at the University of Alberta, Canada, heading a large research laboratory funded by the Alberta Informatics Circle of Research Excellence (iCORE). Dr. Schlegel's research focuses on the areas of error control coding and applications, multiple access communications, modulation and detection, as well as analog and digital implementations of communications system. He is the author of the research monographs "Trellis Coding" and "Trellis and Turbo Coding" by IEEE/Wiley, as well as "Coordinated Multiple User Communications", co-authored with Professor Alex Grant, published by Springer. Dr. Schlegel received a 1997 Career Award, a Canada Research Chair in 2001, and an iCORE Professorship in 2002 and 2007, providing 5Mio\$ in research funding.

Dr. Schlegel is associate editor for coding theory and techniques for the IEEE Transactions on Communications and a guest editor of the Proceedings of the IEEE for their special issue on turbo coding. He has served as the technical program co-chair of the IEEE Information Theory Workshop, ITW 2001, and the IEEE International Symposium on Information Theory, ISIT 2005, as well as the general chair of the IEEE Communications Theory Workshop, CTW 2005. He also served on numerous other IEEE conference program committees, and is an IEEE Distinguished Lecturer.

- **Corey Cheng:**

Lecture #1: Perceptual audio coding: An introduction and some current topics

This lecture will first provide an overview of how perceptual audio codecs work. We will investigate basic psycho-acoustic principles which are used to remove irrelevant and redundant portions of audio, respectively. After briefly reviewing some methods widely used to evaluate audio codecs, such as the ITU-R BS.1116 and ITU-R BS1534 (MUSHRA) standards, we will highlight relevant portions of one or two representative audio codecs, such as AC-3 or AAC (Advanced Audio Coding).

We will then move on to discuss some of our current work in audio coding, such as multiple description error mitigation for wireless networks. Streaming audio transmitted over wireless networks such as 802.11 (Wi-Fi) are susceptible to network packet losses, putting the decoder at risk of producing dropouts in decoded audio. We have devised a method which employs multiple description, a strategy whereby the encoder sends lower-quality “multiple descriptions” of the same audio source over multiple different channels in order to provide some redundancy protection against packet loss during transmission. The decoder then re-assembles all available “multiple descriptions” to make its best estimate of the source. We will then describe a simulation which uses typical packet loss statistics extracted from actual 802.11 (Wi-Fi) wireless networks to test our multiple description system. We found that audio quality is improved with this scheme, but that the overhead associated with this scheme can be high.

Finally, and time permitting, we will conclude the talk by briefly describing some other current topics in the world of audio coding, such as bandwidth extension, multi-channel upmixing, and decoder-side power estimation in the MDCT domain.

Note: it would be helpful to have a pair of speakers available for some simple audio demonstrations.

Speaker’s biography: Corey I. Cheng is associate professor and director of the Music Engineering Technology programs at the University of Miami, Coral Gables. He is also Associate Professor in the department of Electrical and Computer Engineering. Corey holds degrees in electrical engineering from the University of Michigan (Ph.D. 2001, M.S.E. 1998), electro-acoustic music from Dartmouth College (M.A. 1996), and physics from Harvard University (B.A. 1994). Before returning to academia in 2007, he previously worked for six years as a staff engineer in the sound technology division of the research department at Dolby Laboratories, San Francisco, where he developed improvements to the AC-3 (Dolby Digital) and AAC (Advanced Audio Coding) perceptual audio codecs. Corey also consulted regularly with Dolby’s intellectual property groups on patent strategy and patent claim analysis, and he has several U.S. and international patents and patents pending for his work. While at Dolby, Corey co-designed an audio codec for the Radio@AOL service at America-Online, researched multiple-description techniques for quality of service (QoS) improvements to audio streamed over 802.11 wireless (Wi-Fi) networks, developed novel power estimation techniques in the MDCT domain, and investigated novel audio-visual synchronization techniques. Prior to Dolby, Corey worked on car audio equalization research at Fujitsu-Ten Corporation, econosonometric analysis with the Finance Department at the University of Michigan School of Business Administration and the Chicago Board of Trade, and head-related transfer function (HRTF) measurement at the Naval Submarine Medical Research Laboratory (NSMRL), Groton, Connecticut. He has also worked with wavelet applications of signal processing for audio applications, and has composed electro-acoustic music for presentation at international music conferences.

- **Chua-Chin Wang:**

Lecture #1: Circuit and System Implementation of an Implantable Biomedical Device for Micro-stimulation and Neural Sensing

A total solution for an implantable biomedical chip without battery is revealed in this lecture. A system view of the implantable biomedical chip is adopted to carry out the wireless device. All of the design issues as well as the required function blocks are analyzed and designed. Physical measurement on silicon is also included to justify the functionality. The required functions and circuits of the implantable biomedical chip without battery include RF ASK and FSK circuits, inductive power supply and regulator, digital control, stimulating DACs and sensing IA, etc. A framing protocol compatible with RS-232 is adopted to facilitate the wireless transmission of control instructions and data. Several applications of the wireless implantable device are also presented to show its capability.

Speaker's biography: **Technical leader** with academia and industrial recognition for his innovative technical contributions and leadership in high-speed low-power memory design, implantable micro-stimulator circuit and system design, digital TV receiver design and product, and exponential bidirectional associative memory architecture (received both Engineering Professor Award of Chinese Institute of Engineers and Distinguished Engineer Award of Chinese Institute of Electrical Engineers in 2006). **Principle investigator** of over 4 National Science Council (NSC)- and National SOC (NSOC)-funded joint projects to lead multi-discipline teams during 1992-2006 with total funding exceeding 2.5M USD. These projects piloted pioneering and innovative concepts including DVB-T receiver design, ARM-based mobile phone baseband design, x86-compatible high-speed arithmetic circuitry, and implantable wireless biomedical micro-stimulator SOC implementation. **Research coordinator:** Established the VLSI Lab. and founded the SOC group and Wireless SOC Research Center at NSYSU. Developed a track record of research accomplishments, including contributions to wired/wireless communication hardware implementation, implantable bio-circuit SOCs, and hosting of the largest nation-wide SOC conference in Taiwan, namely the "2007 VLSI Design/CAD Symposium" with "SOC in Real" as the main theme, where a total of 952 attendees have participated in this international symposium. **Innovation catalyst** with a patent portfolio consisting of 29 issued patents and 25 pending patent applications, and ~ 230 journal and refereed conference papers. Several of the issued patents have been used in commercial products or factory manufacturing procedures. **Broad technology background** spanning IC and circuit design, communication system architecture/implementation, implantable biomedical circuit design and SOC, digital/analog TV receiver and display circuit design, bidirectional associative memory employed in neural networks, and mixed analog/digital circuit design.

- **David Pan:**

Lecture #1: Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration

Nanometer IC design and manufacturing are facing unprecedented grand challenges for 45nm and beyond, according to ITRS. On one hand, many entangled physical effects continue to pose tremendous challenges to reach design closure with stringent turn-around-time; on the other hand, design closure no longer guarantees manufacturing closure. The conventional contracts between design and fab through design rules are breaking, due to deep sub-wavelength lithography and growing process variations. The semiconductor industry has no alternative lithography solution to replace the 193nm optical lithography (e.g., at least until 22nm). Thus design/manufacturing integration and co-optimization will become more and more important. To enable true design/process integration, it is crucial to be able to model proper manufacturing/variability/yield metrics, and feed them upstream at various physical design implementation stages. This lecture will present synergistic modeling and optimization issues on both physical and electrical *design for manufacturing* (DFM). We will seek to address DFM from its root causes, in a holistic manner through better *manufacturing for design* (e.g., variation aware lithography modeling and optical proximity correction), *manufacturing-design interface* (e.g., predictive silicon image modeling, electrical characterization, and variational aware circuit analysis), and *true "design" for manufacturing* (e.g., manufacturability aware routing and variational aware clock synthesis).

Speaker's biography: David Z. Pan received his Ph.D. in computer science (with honor) from UCLA in 2000. He was a Research Staff Member at IBM T. J. Watson Research Center from 2000 to 2003. He is currently an Assistant Professor and Director of the [UT Design Automation \(UTDA\) Lab](#), at the Department of Electrical and Computer Engineering, University of Texas at Austin. His research is mainly focused on nanometer physical CAD and design for manufacturability. He is also interested in design/CAD of emerging technologies. He holds 5 U.S. patents and has published over 70 technical papers. He is an Associate Editor for *IEEE Transactions on CAD*, *IEEE Transactions on VLSI Systems*, *IEEE Transactions on CAS-II*, and *IEEE CAS Society Newsletter*. He is on the DFM committee of the *International Technology Roadmap for Semiconductor* (ITRS). He has served in the program committees of major VLSI/CAD conferences including ICCAD, ISPD, DATE, ASPDAC, ISQED, and ISCAS. He is the 2007 IEEE/CANDE Workshop Chair, Program/General Chair for ISPD 2007/2008, CAD Track Co-Chair for ISCAS 2006 and 2007. He has received a number of awards for his research contributions, including the *ACM/SIGDA Outstanding New Faculty Award (2005)*, *NSF CAREER Award (2007)*, *SRC Inventor Recognition Award (2000/2008)*, *IBM Faculty Award (2004-2006)*, *IBM Research Bravo Award (2003)*, *Best Paper Award Nominations* at DAC (2006) and ASPDAC (2006/2008), *ISPD 2007 Global Routing Contest Awards* (the 2nd place for 3D and the 3rd place 2D), *ACM Recognition of Service Award (2007)*, *Outstanding Ph.D. Award* from UCLA (2001), *Best Paper in Session Award* at SRC Techcon (1998 and 2007). He is a Senior Member of IEEE.

- **Dinesh K. Bhatia:**

Lecture #1: System level design of low power wireless sensor networks for biomedical applications

Wireless sensor networks (WSN) will become prevalent in many applications that relate to ubiquitous computing. Integrating a large scale system based on WSN is a challenging task that requires efficient management of hardware as well as software resources. Building a robust and reliable system is a must requirement for using WSN in biomedical applications like tele-health and health monitoring. This talk presents system level issues that must be accounted for building a large scale low power network. The talk is illustrated using the construction of a large health monitoring system. Also, as is evidenced by recent industry trends, this talk will highlight how various companies are positioning themselves to exploit this technology.

Lecture #2: No batteries required - Energy harvesting, storage, and management schemes for powering wireless transceivers

Ubiquitous computing, sometimes called as pervasive computing, requires deployment of large number of sensing, processing, and, sometimes, actuating elements. Powering these elements and maintaining their useful life is a challenging task. Although, low power design promises to extend the battery life for such applications, use of battery itself is not practical when the number of elements is large. Efficient energy scavenging methodologies will be described in this talk with construction examples. Also, mechanisms for storing the energy and managing energy use will be described.

Lecture #3: Architecture and CAD for ultra low power mobile FPGAs (mobiFPGA)

Field programmable gate arrays (FPGAs) have revolutionized the ASIC implementations. Advances in technology have resulted in devices that have the ability to support several million gate size designs. However, FPGAs have not been able to find good use in mobile and portable electronics applications. This is primarily due to excessive power requirements for FPGAs. Also, in the presence of scaled fabrication technologies of 65nm and beyond the static leakage power will make FPGAs even more power hungry devices. This talk will present architectures and CAD methodologies for aggressive reduction of dynamic and static power in FPGAs. Technology disclosures and their impact of future generation FPGA architectures will be discussed.

Speaker's biography: Dinesh Bhatia is on the faculty of electrical engineering department at The University of Texas at Dallas. He directs research activities within the Embedded and Adaptive Computing group and is also a member of Center for Integrated Circuits and Systems at the University of Texas at Dallas. He received a Bachelor's in Electrical Engineering from Regional Engineering College, Suratkal, India, and a MS and a Ph.D. in Computer Science from the University of Texas at Dallas. His research interests include all aspects of reconfigurable and adaptive computing, architecture and CAD for field programmable gate arrays (FPGAs), physical design automation of VLSI Systems, biomedical electronics and systems, medical devices, natural energy scavenging and, applications of wireless sensor networks. His recent work on wireless sensor networks operating on scavenged energy is gaining importance in health care applications involving tele-medicine and remote health monitoring as well as in problems related to monitoring and alleviation of wood logging in forests. He has extensive experience in building large scale embedded and reconfigurable systems. Some of these activities include principal designer and investigator for RACE and NEBULA systems for Wright Laboratories of USAF, principal investigator for DARPA funded REACT program, Co-PI on AFRL funded SPARCs program and several more. He has published extensively in leading journals and conferences and continues to serve on program committees of several conferences. He is a senior member of IEEE, Computer Society, Circuits and Systems Society, Eta Kappa Nu, and recently served on the editorial board of IEEE Transactions on COMPUTERS. He is IEEE Circuits and Systems society's distinguished lecturer for 2007.

- **Gerald Sobelman:**

Lecture #1: Flexible VLSI Architectures for UWB, MIMO and Cognitive Radio

Flexibility and efficiency will be key design requirements for future communications transceivers. Systems must be reconfigurable and adaptable in order to minimize power and maximize bandwidth as environmental conditions and user requirements change. This lecture will present architectures and design techniques to achieve these goals for Ultra Wideband (UWB), multiple antenna (MIMO) and Cognitive Radio systems. We will begin with a class of UWB systems based on Orthogonal Frequency Division Multiplexing (OFDM). The standard approach uses large FFTs, which can require a significant amount of hardware resources. An attractive design alternative known as Pulsed-OFDM UWB can achieve the same system-level performance while requiring less hardware and power. We will describe flexible architectures to implement these OFDM-based systems. In addition, we will also present a hardware model of the UWB channel in order to achieve faster system-level verification.

The performance of MIMO systems scales with the number of antennas, so extremely high throughputs are possible. In practice, however, the design complexity also increases rapidly with the number of antennas, so it is crucial to develop efficient implementations for such systems. We will describe a promising approach based on the Geometric Mean Decomposition (GMD) and we will give throughput and design complexity results for a range of MIMO systems.

Cognitive radio seeks to take advantage of the local spectrum conditions in order to maximize throughput whenever possible. This requires a flexible platform in which many aspects of the system can be reconfigured dynamically. For example, the parameters associated with digital filters, FFTs and interleavers may have to be adjusted in order to implement a new data rate, modulation scheme or detection algorithm. In addition, the connections between various functional units may have to be altered to implement different data flow requirements. Programmable functional units and network-on-chip architectures will be described to address these issues.

Speaker's biography: Gerald E. Sobelman received a B.S. degree in physics, summa cum laude, from the University of California, Los Angeles in 1974. He was awarded M.S. and Ph.D. degrees in physics from Harvard University in 1976 and 1979, respectively. He was a postdoctoral researcher at The Rockefeller University, and he has held senior engineering positions at Sperry Corporation and Control Data Corporation. He is currently an Associate Professor in the Department of Electrical and Computer Engineering at the University of Minnesota. He also serves as the Director of Graduate Studies for the Graduate Program in Computer Engineering at the University of Minnesota.

Prof. Sobelman is a Senior Member of IEEE and serves on the technical program committees for IEEE ISCAS, IEEE SOCC and IEEE ICCSC. He is currently Chair-Elect of the Technical Committee on Circuits and Systems for Communications (CASCOM) of the IEEE Circuits and Systems Society. He has also served as an Associate Editor of IEEE Signal Processing Letters. In addition, he has chaired many sessions at international conferences in the areas of communications and VLSI design.

He has developed and presented short courses on digital VLSI design at several industrial sites in the United States and for the Industrial Technology Research Institute (ITRI) in Taiwan. He has given invited lectures at universities in the U.S., South Korea, China and Malaysia. He has also been a consultant to several companies.

His current research interests are in the areas of digital VLSI circuit and system design for applications in communications and signal processing. He has authored or co-authored more than 90 technical papers and 1 book, and he holds 11 U.S. patents.

- **Georges G.E. Gielen:**

Lecture #1: Design of high-resolution CMOS digital-to-analog converters

Data converters are a key block in many applications ranging from telecommunications to medical and automotive applications. Being the interface between the analog and the digital worlds, the performance of data converters is often the bottleneck in the overall system performance. The challenge for digital-to-analog converters is to combine good static (INL/DNL) and dynamic (SFDR) performance. Current-steering DACs are the most frequently used architecture in CMOS technologies. This lecture describes the key fundamental limitations to the static and dynamic performance of this architecture, and also describes possible solutions to solve these problems. This will be illustrated with several practical designs.

Lecture #2: Systematic design of high-performance Delta-Sigma converters

Data converters are a key block in many applications ranging from telecommunications to medical applications. Oversampling Delta-Sigma converters have the benefit of offering high resolutions combined with more relaxed specifications for the analog blocks, at the expense of operating at an oversampled frequency, limiting the achievable signal bandwidth. All this makes the design of Delta-Sigma converters quite complex. This lecture describes methods for the systematic design of high-performance Delta-Sigma converters. The impact of basic circuit nonidealities on the converter performance is modeled in detail.

Lecture #3: Hardware implementation of ultra-low-power sensor networks

Wireless sensor networks are a very promising technology for many applications in logistics, tracking and monitoring. Such networks consist of networked sensor nodes that communicate wirelessly with each other and with central controllers. Many of these applications require a long autonomy, and therefore cannot be battery powered.

Ultra low power electronics and energy scavenging are therefore key requirements of many applications. This lecture describes solutions for ultra low power circuit design. Pulsed ultra wideband (UWB) communication is described as a low power communication technique for these networks. This is illustrated with practical design examples.

Speaker's biography: Georges G.E. GIELEN received the MSc and PhD degrees in Electrical Engineering from the Katholieke Universiteit Leuven, Belgium, in 1986 and 1990, respectively. In 1990, he was appointed as a postdoctoral research assistant and visiting lecturer at the department of Electrical Engineering and Computer Science of the University of California, Berkeley. From 1991 to 1993, he was a postdoctoral research assistant of the Belgian National Fund of Scientific Research at the ESAT laboratory of the Katholieke Universiteit Leuven. In 1993, he was appointed assistant professor at the Katholieke Universiteit Leuven, where he promoted to full professor in 2000.

His research interests are in the design of analog and mixed-signal integrated circuits, and especially in analog and mixed-signal CAD tools and design automation (modeling, simulation and symbolic analysis, analog synthesis, analog layout generation, analog and mixed-signal testing). He is coordinator or partner of several (industrial) research projects in this area, including several European projects (EU, MEDEA, ESA). He has authored or coauthored five books and more than 300 papers in edited books, international journals and conference proceedings. He regularly is a member of the Program Committees of international conferences (DAC, ICCAD, ISCAS, DATE, CICC...), and served as General Chair of the DATE conference in 2006. He serves regularly as member of editorial boards of international journals (IEEE Transactions on Circuits and Systems, Springer international journal on Analog Integrated Circuits and Signal Processing, Elsevier Integration). He received the 1995 Best Paper Award in the John Wiley international journal on Circuit Theory and Applications, and was the 1997 Laureate of the Belgian Royal Academy on Sciences, Literature and Arts in the discipline of Engineering. He

received the 2000 Alcatel Award from the Belgian National Fund of Scientific Research for his innovative research in telecommunications, and won the DATE 2004 Best Paper Award. He is a Fellow of the IEEE, served as elected member of the Board of Governors of the IEEE Circuits And Systems (CAS) society and as chairman of the IEEE Benelux CAS chapter. He served as the President of the IEEE Circuits And Systems (CAS) Society in 2005. He was elected DATE Fellow in 2007, and received the IEEE Computer Society Outstanding Contribution Award and the IEEE Circuits and Systems Society Meritorious Service Award in 2007.

- **Hubert Harrer:**

Lecture #1: Multi-chip module packaging and its impact on architectures

Multi-chip module (MCM) packages enable architectures with very high bandwidths between the processor chips and their cache chips. By that today's computer systems can achieve bandwidths of 440GB/s to the cache chips on a single processor node. It drives a tremendous challenge for the wiring of the chip I/Os into the system, which can be resolved by the use of ceramic multi-chip modules. MCMs also allow a high chip density on the package for chips with high power dissipation and efficient cooling by using a refrigeration unit. The lecture will show the architecture and packaging implementation of IBMs system z and then focus on the design of MCMs including high frequency aspects. The design methodologies have to cover the power delivery, electrical timing and cross talk for each net in the system as well as good decoupling strategies to achieve stable voltages for currents being larger than 1000A.

Speaker's biography: Dr. Harrer is a Senior Technical Staff Member (STSM) since 2002 working in the IBM Server and Technology Group. He received his Dipl.-Ing. degree in 1989 and his Ph.D. degree in 1992 from the Technical University of Munich. In 1993 he received a DFG research grant to work at the University of California at Berkeley in the paradigm of Cellular Neural Networks. During this time he has developed a new neural network architecture (Discrete Time Cellular Neural Networks) and implemented its structure on an analog VLSI chip. Since 1994 he has worked for IBM in the Boeblingen Packaging Department.

In 1999 he was on international assignment at IBM Poughkeepsie, New York. He was leading the z900 MCM designs and is the technical lead for z-series CEC packaging designs since 2001. This includes the system z990 and system z9 mainframe computers. His technical interests focus on packaging technology, high frequency designs and electrical analysis for first and second level packaging. He has published multiple papers and holds 7 patents in the area of packaging.

- **Huifang Sun:**

Lecture #1: Concept, Standards and New research topics of Digital Video Technology

In this lecture, I will give an overview of concept digital video technology and several new topics undergoing in research community and MPEG standard activities. During past few years, we have carried out many digital video related research topics and projects in several areas, which include: video compression, video transport and networking system, video transcoding, universal multimedia access, video summarization, video indexing, video segmentation, and video signal analysis. Some research results have been applied to the products and prototype of demonstrations. This lecture will briefly introduce several new areas such as high dynamic range video coding and full color professional video coding.

Lecture #2: MPEG Standards and its DTV Applications

Digital video signal processing is an area of science and engineering that has developed rapidly over the past decade. The maturity of the moving picture expert group (MPEG) video coding standards is a very important achievement for the video industry and provides a strong support for digital transmission and storage of video signals. So far, MPEG has developed well-known standards, MPEG-1, MPEG-2, which are Emmy Award-winning standards, MPEG-4 and recently developed H.264 or MPEG-4 Part 10 Advanced Video Coding. MPEG is currently also working on H.264 extension such as Scalable video coding, full color video coding. The core compression technology used in DTV application is the MPEG-2 standards, however, the potential applications of H.264 will greatly enhance the DTV applications in near future. In this talk we will introduce the MPEG standards and its impact on the video industries.

Lecture #3. Multiview video coding

Conventional video coding systems are designed to encode the video from a single video source. With the emergence of new interactive applications and display technology that require multiple views of video, there is a need to extend the conventional coding schemes to exploit the redundancy between camera views and provide higher coding efficiency than independent coding of each view. Disparity compensated prediction is one of the more common techniques to exploit inter-view correlations. In this scheme, certain views are encoded independently using a standard video encoder; these independently encoded views are reference views. The remaining views are then encoded using temporal prediction and inter-view spatial predictions based on reconstructed reference views. The prediction can be determined adaptively on a per block basis.

In this lecture, we describe the prediction of select views based on view synthesis methods. The potential advantage of this form of prediction over traditional spatial prediction is that the synthesized view attempts to reconstruct the view from neighboring views using camera parameters and depth information. Such an approximation of the view to be coded could have significant advantages in fast moving areas of a scene and for objects that undergo non-translational motion by providing a better predictor of the frame.

Speaker's biography: Huifang Sun graduated from Harbin Military Engineering Institute, Harbin, China, and received the Ph.D. from University of Ottawa, Canada. He joined Electrical Engineering Department of Fairleigh Dickinson University as an Assistant Professor in 1986 and was promoted to an Associate Professor before moved to Sarnoff Corporation in 1990 as a member of technical staff and was promoted to a Technology Leader of Digital Video Communication later. In 1995, he joined Mitsubishi Electric Research Laboratories (MERL) as Senior Principal Technical Staff and was promoted as Vice President and Fellow of MERL and Deputy Director of Technology Laboratory in 2003. His research interests include digital video/image compression and digital communication. He has published two books more than 140 Journal and Conference papers. He holds 48 US patents and has more pending. He received AD-HDTV Team Award in 1992 and Technical Achievement Award for optimization and specification of the Grand Alliance HDTV video compression algorithm in 1994 at Sarnoff Lab. He

received the best paper award of 1992 IEEE Transaction on Consumer Electronics, the best paper award of 1996 ICCE and the best paper award of 2003 IEEE Transaction on CSVT. He is now an Associate Editor for IEEE Transaction on Circuits and Systems for Video Technology and was the Chair of Visual Processing Technical Committee of IEEE Circuits and System Society. He is an IEEE Fellow. He is invited as guest professor for many universities in China including Peking University, Shanghai Jiaotong University, Tianjin University, Zhejiang University, Chinese Academia, and few others.

- **John Harris:**

Lecture #1: Biologically Inspired Signal Processing

There is growing interest in using biological-inspiration to improve the design of computation systems, particularly in the areas of sensory processing and pattern recognition where biological systems far outperform the best man-made devices. For instance, state-of-the-art speech and face recognition algorithms pale in comparison to human performance despite hundreds of man-years of research in these fields. We survey several examples of biologically-inspired engineering designs including work with Motorola on improving cell-phone speech quality, a new type of digital camera with much wider dynamic range and user-friendly interfaces for next-generation smart appliances. In each case, the study of biology leads to natural and effective engineering solutions that can be implemented in DSPs or in special-purpose analog VLSI circuits.

Lecture #2: Automatic Speech Processing Techniques for Enhancing Cell Phone Speech

Cell phones regularly provide extremely challenging listening scenarios. Together with Motorola iDEN, we have addressed this problem in several ways. First, we have developed real-time DSP enhancement algorithms to make speech louder and more intelligible without losing naturalness or adding any energy to the signal. Second, we are designing a cell phone that will adapt to an individual's unique hearing abilities and the noise environment in which the cell phone is being used. In this way, the phone will compensate for a listener's hearing loss whether permanent or due to temporary environmental noise conditions. We summarize these approaches and comment on the future use of these techniques.

Lecture #3: Biologically Inspired Sensing and Coding of Signals

We discuss the role of biologically inspired spike representations in various engineering applications including sensor design, time-based signal processing, and power-efficient strategies for neural recording circuitry in brain-machine interfaces. These spike-based systems are shown to outperform conventional approaches in terms of power consumption, size, SNR, and dynamic range. We also consider the implications this work has on our understanding of neurobiological systems.

Speaker's biography: Dr. John G. Harris received his BS and MS degrees in Electrical Engineering from MIT in 1983 and 1986. He earned his PhD from Caltech in the interdisciplinary Computation and Neural Systems program in 1991. After a two-year postdoc at the MIT AI lab, Dr Harris joined the Electrical and Computer Engineering Department at the University of Florida (UF). He is currently a full professor and leads the Hybrid Signal Processing Group in researching biologically-inspired circuits, architectures and algorithms for sensing and signal processing. Dr. Harris has published over 100 research papers and patents in this area. He co-directs the Computational NeuroEngineering Lab and has a joint appointment in the Biomedical Engineering Department at UF.

- **Kai-Kuang Ma:**

Lecture #1: Super-Resolution Imaging

The goal of *super-resolution* (SR) image reconstruction is to produce one high-resolution image from its lower resolution counterparts; hence, this is beyond the conventional, single-image-based interpolation. In this talk, we shall introduce our two newly invented novel approaches; one is stochastic method and the other deterministic method. For the former, a stochastic SR image reconstruction based on *Markov chain Monte Carlo* (MCMC) technique is introduced. For the deterministic approach, a new state-space approach by incorporating more observation correlation will be discussed as well. Artifacts issue will be addressed. Extensive experiments are conducted to demonstrate the superior performance of the proposed methods

Lecture #2: Image and Video Compression: Algorithms, Optimization, and Trend

With multiple international image and video coding standards being successfully introduced after decades of intensive research endeavored in their respective fields, a fundamental question has been often raised in recent years --- has image compression reached the saturation point? In this talk, we shall have an overview of this topic from several angles, revisit some state-of-the-art components, and discuss the optimization issues and future trend.

Speaker's biography: Professor Ma received his B.E. degree (electronic engineering) from Chung Yuan Christian University, Chung-Li, Taiwan, Republic of China, M.S. degree (electrical engineering) from Duke University, Durham, NC, U.S.A., and the Ph.D. degree (electrical engineering) from North Carolina State University, Raleigh, NC, U.S.A.

He is now Full Professor of Information Engineering, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore. He had served as Deputy Director of Centre for Signal Processing (CSP; 2002~2007) and Programme Director of Master of Science Degree (on Signal Processing; 2002~2006). From 1992 to 1995, he was a Member of Technical Staff at Institute of Microelectronics, National University of Singapore, working on digital video coding and the MPEG standards. From 1984 to 1992, he was working in IBM Corporation at Kingston, NY, and then Research Triangle Park, NC, U.S.A., engaging on various DSP and VLSI advanced product development. His research interests are in the areas of digital signal, image and video processing. These include digital image/video coding and standards, wavelets and filter banks, image/video processing, denoising, super-resolution, error resilience and concealment, content-based image indexing and retrieval, and scene analysis and recognition. Prof. Ma has produced more than one hundred publications in well-known international journals (mainly, IEEE), conferences, and MPEG standardization meetings. He holds one USA patent on fast motion estimation algorithm.

He was serving as Singapore MPEG Chairman and Head of Delegation (1997-2001). On the MPEG contributions, two fast motion estimation algorithms (Diamond Search and MVFAST) produced from his research group have been adopted by the MPEG-4 standard, as the reference core technology for fast motion estimation. He is the General Chair of organizing a series of international standard meetings (MPEG and JPEG), JPEG2000 and MPEG-7 workshops held in Singapore (March 2001).

He is Technical Program Co-Chair of two IEEE international conferences: the International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS) 2007, and the IEEE International Conference on Image Processing (ICIP) 2004, which is one of the flagship conferences of the IEEE Signal Processing Society. He was serving as Video Processing Track Co-Chair of the International Conference on Acoustics, Speech and Signal Processing (ICASSP) 2007. Dr. Ma is currently serving as (Associate) Editor or Editorial Board Member of five international journals: the *IEEE Transactions on Image Processing* (2007~now), *IEEE Transactions on Communications* (1997~now), the *IEEE Transactions on Multimedia* (2002~now),

the *International Journal of Image and Graphics* (2002~now), and the *Journal of Visual Communication and Image Representation* (2005~now). He is an elected member of three Technical Committees: *Image and Multidimensional Signal Processing* (IMDSP) Committee from the IEEE Signal Processing Society, *Multimedia Communications* Committee from the IEEE Communications Society, and *Digital Signal Processing* from the IEEE Circuits and Systems Society. He has been serving as Technical Program Committee member, reviewer and Session Chair of numerous international journals and conferences. He is Chairman of IEEE Signal Processing Singapore Chapter (2000-2002). He is a Senior Member of the IEEE and member of Eta Kappa Nu.

- **Nam Ling:**

Lecture #1: Simplified fast motion estimation: Simplified and unified multi-hexagon search (SUMH) with context adaptive Lagrange multiplier (CALM)

Fast motion estimations are especially important to speed up the time-consuming encoding processes for H.264 video encoding. In this talk, we first present our simplified fast motion estimation method, called Simplified and Unified Multi-Hexagon Search (SUMH), that produces a significant speed-up as compared with today's fast motion estimations, yet encounters only a small PSNR degradation when compared to that of full search. In addition, we present a novel method to refine the Lagrange multiplier, called Context Adaptive Lagrange Multiplier (CALM), for rate-constrained motion estimation. Both our methods were recently adopted into the H.264/MPEG-4 AVC video coding international standard (including the text document and the JM reference software). Our SUMH method was adopted as JVT-P021 and our CALM method as JVT-T046.

Our SUMH is based on two principles, partial distortion search (PDS) and dual-halfway-stop (DHS) algorithms. PDS generally produces less video quality degradation of the predicted images than those of conventional fast block matching algorithms (BMAs). However, the speedup gain of PDS algorithms is usually limited. In this talk, we present an enhancement over a normalized PDS (NPDS) algorithm to further reduce block matching motion estimation complexity and improve video fidelity. The novelty of our algorithm is that, in addition to the halfway-stop technique in NPDS, a dual-halfway-stop (DHS) method, which is based on a dynamic threshold, is proposed so that block matching is not performed against all searching points. The dynamic threshold is obtained via a linear model utilizing already computed distortion statistics. An adaptive search range mechanism based on inter block distortion further constrains the searching process. Experimental results show that our proposed method reduces the encoding time by about 55% on the average when compared to those of the state-of-the-art methods, with similar rate-distortion performances. Our SUMH algorithm, making use of DHS-NPDS, consists of two parts, an integer-pel fast search and a sub-pel fast search.

To extend motion estimation further, we propose a new simple and efficient method to adjust Lagrange multipliers based on the context (CALM), which improves the accuracy for the detection of true motion vectors as well as the most efficient encoding modes for luma, which are used for deriving the motion vectors and modes for chroma. Simulation results show that the chroma bit rates can be reduced by 4.36% and 4.80% (on the average) for U and V components, respectively, when compared with that of the JM 10.2 reference software. In addition, the coding efficiency improvement is comparable to the more complicated rate-distortion optimized (RDO) mode decision techniques.

A demo will be given in the talk.

Speaker's biography: Prof. Nam LING received a B.Eng. degree in Electrical Engineering from the National University of Singapore (NUS). He received M.S. and Ph.D. degrees, both in Computer Engineering, from the University of Louisiana at Lafayette, U.S.A. Prof. Ling is currently a full Professor with the Department of Computer Engineering and the Associate Dean (Research and Faculty Development) for the School of Engineering at Santa Clara University (SCU), California, U.S.A. He is also a Consulting Professor and Honorary Advisor to the National University of Singapore (NUS Overseas Colleges) and a Guest Professor of Shanghai Jiao Tong University (China). He has served as Visiting Professor/Consultant/Scientist/Scholar to institutions such as the Institute for Infocomm Research (I²R) (Singapore), Nanyang Technological University (Singapore), National Dong Hwa University (Taiwan), and National Chiao Tung University (Taiwan).

Prof. Ling has more than 130 publications in the fields of video/image coding, video decoder design, video communications, and systolic arrays. He is the primary author of the book entitled

Specification and Verification of Systolic Arrays. Prof. Ling received the Arthur Vining Davis Junior Faculty Fellowship in 1991 and the SCU Outstanding Achievement Award in Teaching, Research, and Service, in 1992. Prof. Ling was named 1999 Researcher of the Year by SCU Engineering. He received the SCU Award for Recent Achievement in Scholarship in 2002 and the SCU President's Recognition Award in 2005. He was named IEEE Distinguished Lecturer (Circuits and Systems) for 2002-2003 and 2007-2008. Prof. Ling also received the 2003 IEEE ICCE Best Paper Award (First Place Winner) for his work on MPEG-4 face animation. He and his team's proposal on simplified fast motion estimation (SFME) method was adopted in 2005, and their context adaptive Lagrange multiplier (CALM) method was adopted in 2006, both into the H.264/MPEG-4 AVC video coding international standard.

Prof. Ling served as an Associate Editor for the IEEE Transactions on Circuits and Systems - I in 2002-03. He was a Guest Editor for the Journal of VLSI Signal Processing Systems special issue in 2006. In 1993 - 1995, Prof. Ling served as the Chair of the IEEE Computer Society Technical Committee (TC) on Microprocessors and Microcomputers. Currently, he serves as the Chair of the IEEE Circuits and Systems Society Circuits and Systems for Communications Technical Committee. He is also a member of the VSPC TC (IEEE Circuits and Systems Society) and a member of the DISPS TC (IEEE Signal Processing Society). Prof. Ling was the General Chair for the IEEE Hot Chips Symposium in 1995. He is currently Technical Program Co-Chair for ISCAS'07 and Program Co-Chair for SiPS'07. He served as Program Chair/Co-Chair for DCV'02 and SiPS'00. He was Track Co-Chair for ISCAS'04, ISCAS'05, and ISCAS'06. Prof. Ling served in program committees, organizing committees, and as session chairs for many IEEE conferences. He has delivered more than 70 invited/distinguished/keynote colloquia in six different countries.

- **Naveen Yanduru:**

Lecture #1: WCDMA receiver design: System budgeting, circuit architecture and circuit design

Practical aspects of WCDMA receiver design from understanding the 3G specifications to budgeting the RF parameters, receiver architecture selection and circuit design details will be discussed. The designs of two generations of WCDMA receivers led by the author at Texas Instruments will be used as examples. Special attention will be paid to understanding the derivation of RF system parameters considering that the signals and blockers are WCDMA modulated and not CW. The two designs discussed are in RFSiGe vs. 90nm CMOS providing the audience in appreciating the difference in design challenges in each case.

Lecture #2: Highly re-configurable RF receivers in deep sub-micron CMOS and challenges towards a true SDR receiver

Multiple RF bands, modulation schemes, duplex mechanisms and signal bandwidths needed for the various standards for the mobile terminal, call for a highly reconfigurable RF receiver. Designing a “multi-mode” RF receiver for a given RF band with highly reconfigurable performance is thus important. FDD based standards such as WCDMA demand high linearity and normally require a SAW filter between LNA and mixer. TDD based standards like EDGE do not have the same challenges. A WCDMA/EDGE receiver without inter-stage SAW filter in 90nm CMOS is used as an example in illustrating the architecture, circuit and system considerations for such a receiver. However, to achieve a true Software Defined Radio receiver, the RF pre-select filter forms a bottleneck in terms of achieving a “multi-band” receiver. A few of the possible architectures for a multi-band receiver and their limitations are presented.

Speaker’s biography: Naveen Yanduru serves as Receiver Design Manager and a Member of Technical Staff at Texas Instruments, Inc. While at TI he has led several RF receiver design teams and projects for various cellular standards including GSM, WCDMA, TDSCDMA and GPS. Most recently, he served as an architect and led the design of a dual mode UMTS (WCDMA, EDGE) receiver in 90nm CMOS that did not require an external inter-stage filter. His research interests include multi-mode, multi-band receiver front-ends in deep submicron CMOS, quantifying the effect of AM blockers on RF receiver performance and design of on-chip RF filters. He has more than 10 years of experience in RF IC design, published over 15 papers in professional journals and international conferences, and holds 6 patents and patent applications. He has given invited talks and workshop tutorials at IEEE conferences including RFIC Symposium. He has MSEE from Kansas State University.

- **Sudhanshu Shekhar Jamuar:**

Lecture #1: Current Trends of Low Voltage Analog Design for Wireless Application

The importance of power consciousness is well understood by many in wireless applications. With the growing experience on the fundamental principles of power conscious design, current mode approach for low voltage analog designs are now becoming known. Current mode approach has proven to be a better alternative for a low voltage high performance analog circuit design. This paper covers the current trends of design techniques for low voltage analog circuit designs utilizing current mode approach within the CMOS environment. Some of the new techniques are decoupling scheme, improved current mirror, transistors operating in subthreshold region, active cascode scheme and controllable gain. This talk presents the design techniques applied on various building blocks (i.e LNA, mixer, filter, VCO and VGLNA) of a typical wireless receiver system including RF circuits using MEMS technology is also included with its role on low power consumption. These techniques are expected to find use in most analog circuits emphasizing on low power consumption especially in the wireless applications.

Lecture #2: Design Techniques and CMOS Implementation of Low Noise Amplifier (LNA)

The rapid growth of portable RF communication systems in various standards has led to the demand for one chip to cover several standards such as WCDMA, WLAN, GSM etc. The RF front-end would have to cover a huge range of different carrier frequencies for all standards, thus to integrate all this in one chip would be very area inefficient. Competitive technologies have emerged for wireless system implementation taking into account scaling, integration ability and cost. Any wireless system consists of a transmitter and a receiver. The transmitter delivers the signal modulated through an antenna while the receiver recovers the received signal from the antenna. The performance of the system depends on the system design, circuit design and system requirement. The acceptable level of noise varies with system requirements. Noise and interference as unwanted signals set a limit on the usable signal level at the output. Thus, for the signal to be usable, the signal power must be larger than the noise power specified by minimum signal-to-noise ratio. The stringent requirements for different wireless systems place particular emphasis on each building blocks of the receiver. Thus, improved design techniques are needed for different standard of RF systems. A receiver system consists of the following circuits: a low noise amplifier, mixer, voltage-controlled oscillator (VCO), intermediate frequency (IF) amplifier and filters. Low noise amplifier (LNA) is typically the first active stage for the RF front-end. Its main function is to amplify low signal without adding noise, thus preserving the signal-to-noise ratio (SNR) of the system at low power consumption. Many tradeoffs involved in designing the LNA such as noise figure (NF), linearity, gain, impedance matching and power dissipation. Therefore, proper LNA design considerations and techniques are crucial in today's communication technology. A novel LNA is typically implemented using voltage-mode techniques. Rivaling classical designs, techniques for a variable-gain LNA can be designed using current mode approach. The tutorial includes current-mode approach, which offers several advantages that might be suited for certain communication standard. The tutorial would covers steps involved in designing a LNA – DC biasing voltage, stability design analysis, noise matching and impedance matching. This lecture would place an emphasis on improved design techniques for one of the building block of RF system, low noise amplifier (LNA). In order to meet the objectives of tutorial, DC biasing techniques, impedance matching techniques, noise matching and stability analysis will be discussed. Voltage mode design and current mode design techniques will be elaborated. Variable gain low noise amplifier design techniques will also be discussed. All the design techniques and simulations presented in the tutorial will be based on EDA tools.

Speaker's biography: Sudhanshu S. Jamuar received his M. Tech and Ph. D. in Electrical Engineering from Indian Institute of Technology, Kanpur, India in 1970 and 1977 respectively. He worked as Research Assistant, Senior Research Fellow and Senior Research Assistant from 1969 to 1975 at IIT Kanpur. During 1975-76, he was with Hindustan Aeronautics Ltd., Lucknow. Subsequently he joined the Lasers and Spectroscopy Group in the Physics Department at IIT

Kanpur, where he was involved in the design of various types of Laser Systems. He joined as Lecturer Electrical Engineering Department at Indian Institute of Technology Delhi in 1977, where he became Assistant Professor in 1980. He was attached to Bath College of Further Education, Bath (UK), Aalborg University, Aalborg (Denmark) during 1987 and 2000. He was a Professor in the Department of Electrical Engineering at IIT Delhi from 1991 to 2003. He was Consultant to UNESCO during 1996 in Lagos State University, Lagos (Nigeria). He was with University Putra Malaysia during 1996–97 in the Faculty of Engineering. Presently he is Professor in the Electrical and Electronic Engineering Department in the Faculty of Engineering, University Putra Malaysia (Malaysia) since 2001. He has been teaching and conducting research in the areas of Electronic Circuit Design, Instrumentation and Communication Systems.

He has coauthored more than 40 papers in International Journals and conferences. He recently received Taiwan Patent on “A Simulation Circuit Layout Design for Low Voltage, Low Power and High Performance Type II Current Conveyor”. He is recipient of Meghnad Saha Memorial Award 1976 from IETE, Distinguished Alumni Award from BIT Sindri in 1999, Best paper award in IETE Journal of Education 2004 from IETE. He also holds the position of independent director on the Board of Tanla Solutions, which has been ranked sixth in the 2007 Deloitte Technology Fast50 in India.

He is Senior Member of IEEE and Fellow of Institution of Electronics and Telecommunications Engineering (India). He is on the Editorial Board of Wireless Personnel Communication Journal. He is presently the Chapter Chair for IEEE CAS Chapter in Malaysia.

- **Tobi Delbruck:**

Lecture #1: Building a high performance silicon retina for machine vision

There is an assumption underlying machine vision that it must be based on sequences of image frames that are pulled from the camera and then processed on computers. Frame based image sensors are highly evolved but have fundamental drawbacks, including limited dynamic range, limited sampling rate, and the necessity for expensive post-processing. Biology teaches us that the outputs of the eye are very sparse and are asynchronously pushed to the brain in the form of digital spikes. Recent developments in building asynchronous vision sensors that offer this same form of spike output have shown that they offer advantages in terms of dynamic range (>100dB), temporal resolution (several kHz), and especially post processing cost. This lecture will discuss these developments; in particular how good matching is obtained using self-timed switched capacitor operation, and shows a live demonstration of the capabilities of a silicon retina for machine vision.

Speaker's biography: Tobi Delbruck (<http://www.ini.uzh.ch/~tobi>) is a group leader at the Institute of Neuroinformatics (INI), part of ETH Zurich and the University of Zurich, Switzerland and visiting scientist at Caltech. His group develops neuromorphic electronics, particularly vision sensor chips. He studied physics and applied mathematics as an undergraduate and received his PhD from Caltech in 1993 in Computation and Neural Systems with Carver Mead. He co-invented the standard neuromorphic adaptive photoreceptor circuit and bump circuit. Subsequently he worked for several years for Arithmos, Synaptics, National Semiconductor, and Foveon, where he was one of the founding employees. In 1998 he moved to Switzerland to join INI. In 2002 he was lead developer of the tactile luminous floor used in INI's exhibit "Ada: Playful Intelligent Space". He has been awarded 8 patents, and has over 30 refereed papers in journals and conferences, 4 book chapters, and 1 book. He has been awarded 4 IEEE awards, including the 2006 ISSCC Jan Van Vessel Outstanding European Paper Award.

- **Wallace Tang:**

Lecture #1: Identification and monitoring of complex networks based on synchronization

Complex networks are ubiquitous in our life. Power systems, internet, biological neural networks, and even our community are just a few examples, but each one is greatly affecting us. During the last decade, the characteristics of different network models, such as small-world networks, scale-free networks, and random networks, have been largely explored so as to promote a more accurate topological modeling, a better understanding or more detailed analysis of these networks. However, it still remains as a technical challenge to uncover the exact topology of a complex network in question. The difficulty further escalates when the accessibility of the network is very limited.

In this lecture, it is to discuss the methodology for identifying the underlying topology of a complex network, and monitoring the connectivity of its nodes. The design is based on the concept of auto-synchronization. By building an adaptive observer system for the complex network, it is possible to identify the network topology with a limited number of observable states, even if the node model is not exact or some of the parameters are unknown. This method not only can improve the model of a complex network, but also monitor the targeted system and report any fault occurrence.

Some real-world complex networks, including biological neural network and power system network, will be considered as examples. The proposed method is found to be useful for fault detection in a network, improving biological neuron model and providing a better understanding of the biological neural network.

Speaker's biography: Dr Tang obtained his BSc from the University of Hong Kong in 1988, and both MSc and PhD from the City University of Hong Kong in 1992 and 1996, respectively. Prior to his doctorate programme which was started in September 1993, he has worked in Industry for over five years. He is currently an Associate Professor in the Department of Electronic Engineering, City University of Hong Kong. He has published over 60 journal papers and four book chapters, and co-authored two books, focusing on the area of genetic algorithms, chaotic circuits, synchronization and control.

He was an associated editor for IEEE Transactions on Circuits and Systems II in 2004-2005. Currently, he is the associated editor for Dynamics of Continuous, Discrete and Impulsive Systems Series B: Applications & Algorithms. He is also a member of Nonlinear Circuits and Systems (NCAS) Technical Committee in IEEE CAS Society, a member of IFAC Technical Committee on Optimal Control.

- **Zhiping Lin:**

Lecture #1: State space realization of a 3D image set with application to noise reduction of fluorescent images

A new method is presented to calculate state space realizations of a three-dimensional (3D) image set. It is based on interpreting the image set as the impulse response of a 3D separable system. The proposed realization algorithm consists of two parts:

- 1.) Decomposition of a 3D image set into the product of three 1D components;
- 2.) Balanced state space realizations of finite 1D sequence.

The proposed method can be used for realizing the given 3D images exactly or approximately. The advantage of the method is noise can be reduced with little degradation on the image quality. It has been successfully applied in noise reduction of various 3D image sets of fluorescently labeled cells acquired by a fluorescent microscope. It can be used for noise reduction in a 3D image set or for noise suppression of a point spread function (PSF) which is an essential component in any 3D deconvolution algorithms.

Speaker's biography: Zhiping Lin received the B. Eng degree from South China Institute of Technology, China in 1982, and the Ph.D. degree from the University of Cambridge, England in 1987. Subsequently, he worked as a postdoctoral researcher at the University of Calgary, Canada. He was an associate professor at Shantou University, China from 1988 to 1993, and a senior engineer at DSO National Laboratories, Singapore from 1993 to 1999. Since Feb. 1999, he has been an associate professor at Nanyang Technological University (NTU), Singapore. He is currently serving as the Program Director of Bio-Signal Processing, Center for Signal Processing, NTU.

Dr. Lin was an editorial board member from 1993 to 2004, a guest editor for the special issue on "Applications of Grobner bases to multidimensional systems and signal processing" in 2001, and a Co-Editor since 2005, all for the Journal of Multidimensional Systems and Signal Processing. He has been an associate editor for the Journal of Circuits, Systems and Signal Processing since 2000. He is currently serving as the Chair of the IEEE Circuits and Systems Singapore Chapter. Dr Lin is a member of the Digital Signal Processing Technical Committee (TC) and the Life Sciences Systems and Applications TC of the IEEE Circuits and Systems Society. He has served in organizing/technical committees of various international conferences, including Program Co-Chair of ICICS 2001, General Vice-Chair of IEEE ICICS-PCM 2003, and Finance Chair of IEEE APCCAS 2006. His research interests include multidimensional systems and signal processing, array and radar signal processing, and biomedical signal processing.

- **Zixiang Xiong:**

Lecture #1: Optimized error protection of scalable image bit streams

The growing importance of the Internet and the development of new communication devices such as 3G and 4G mobile phones have raised interest in robust image communication systems over unreliable channels. Error control can be achieved with forward error correction (FEC), error concealment, or error detection and retransmission. This talk focuses on FEC for scalable image coders. For various channel models, we survey recent progress made in system design and discuss efficient source-channel bit allocation techniques, with emphasis on unequal error protection.

Lecture #2: Distributed video coding

Driven by a host of emerging applications (e.g., wireless video and sensor networks), there has been a flurry of recent research activities on distributed video coding (DVC). Specifically, several DVC schemes have been proposed with encouraging results, showing that DVC has the benefit over standard video coding in terms of lower encoding complexity, improved error robustness, and enabling layered Wyner-Ziv coding and multiterminal/ multiview video coding. MPEG has recently identified DVC as one of the future directions of video coding.

This talk will give an overview of DVC with focus on my group's work on layered Wyner-Ziv coding, distributed source-channel coding of video based on fountain codes and Raptor codes, and multiterminal video coding.

Lecture #3: Wyner-Ziv and dirty-paper coding: Duality, limit-approaching code designs and applications

Network information theory, although still partial, generalizes Shannon's classic information theory and offers strong potential gains over conventional point-to-point communication techniques. However, most results in network information theory have remained at the theoretical level and the lack of practical code designs for multiterminal networks has limited the potential applications of the theory in practice.

Aiming to change this situation, this talk examines two well-known dual problems in network information theory, namely, quadratic Gaussian Wyner-Ziv coding and dirty-paper coding. An algebraic binning framework is put forth in terms of source-channel coding for both problems that leads to syndrome-based binning for the former and message-based binning for the latter. Practical designs based on TCQ and LDPC/IRA codes show that we are approaching the theoretical limits for both problems. Applications of Wyner-Ziv coding to video compression and receiver cooperation and those of dirty-paper coding to image data-hiding and coding for Gaussian broadcast channels will be highlighted.

Speaker's biography: Zixiang Xiong received the Ph.D. degree in Electrical Engineering in 1996 from the University of Illinois at Urbana-Champaign.

From 1995 to 1997, he was with Princeton University, first as a visiting student, then as a research associate. From 1997 to 1999, he was with the University of Hawaii. Since 1999, he has been with the Department of Electrical and Computer Engineering at Texas A&M University, where he is a Professor. His research interests are network information theory, code designs and applications, biomedical engineering, genomic signal processing, and networked multimedia.

Dr. Xiong received a National Science Foundation Career Award in 1999, an Army Research Office Young Investigator Award in 2000, and an Office of Naval Research Young Investigator Award in 2001. He also received the 2006 IEEE Signal Processing Magazine best paper award. He served as associate editor for the IEEE Trans. on Circuits and Systems for Video Technology

(1999-2005), the IEEE Trans. on Image Processing (2002-2005), and the IEEE Trans. on Signal Processing (2002-2006). He is currently an associate editor for the IEEE Trans. on Systems, Man, and Cybernetics (part B). He is the publications chair of ICASSP'07 and the technical program committee co-chair of ITW'07.

Dr. Xiong is a fellow of the IEEE. He was elected as a member of the IEEE Signal Processing Society Multimedia Signal Processing Technical Committee, the IEEE Communications Society Multimedia Communications Technical Committee, and the IEEE Circuits and Systems Society Multimedia Systems & Applications Technical Committee. He was also a tutorial presenter at ICASSP'05, VCIP'05, ICME'07 and Globecom'07.