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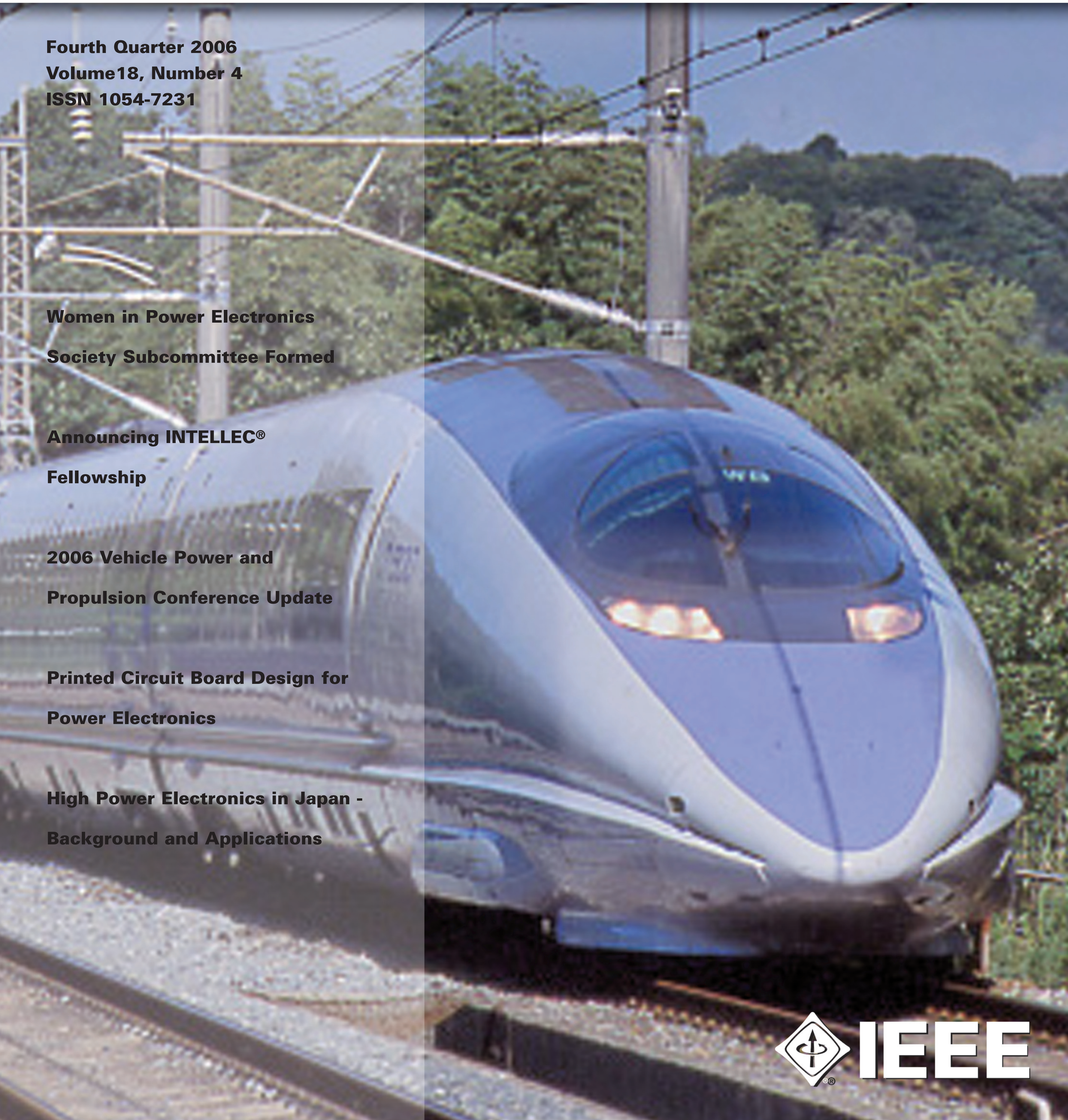

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From The Editor

John M. Miller

This is the final issue for 2006 and I am pleased to say it has been my pleasure to bring news items and other noteworthy articles to our membership. Looking back over the past year our issue themes have covered interesting topics: January 2006 covered the notification of a new standards sponsoring committee within PEL's; a post script on the 2005 Future Energy Challenge, and technical articles focused on extreme environment electronics. In April 2006 we completed the extreme environment electronics topic and added a technical article on single event effects in space electronics and then we turned our attention to describing getting a paper accepted in the transactions. In the July 2006 issue our topics of interest centered almost exclusively on wind energy and wind turbine systems. Completing the year with this issue we turn to power electronics circuits.

In this issue readers will find three technical articles, two of which are at the core of power electronics applications and one that fits into our technical tips category. Mr. Tsuyoshi Funaki writes on High Power Electronics in Japan and how power electronics has become the enabler for quality and reliability of the social infrastructure. This contention is supported by case studies of high voltage dc transmission and the Shinkansen train. This is followed by a very interesting article on Printed Circuit Board Design by Robert Balog and Jonathon Kimball. The authors describe the integration of planar magnetics, advanced thermal design, electromagnetic compatibility, grounding and safety considerations into circuit card layout. Lastly, we are pleased to include an insightful topic on rms Value Determination of Phase Currents in Full Bridge Rectifiers with Capacitive Filter Using Parabolic Approximation by Mr. Juan Carlos A. Floriani.

Currently technical topics for 2007 (PEL's newsletter Vol. 19) are in the planning stages.

January 2007	Technical committee topic
April 2007	Technical committee topic
July 2007	Technical committee topic
October 2007	Technical committee topic

John M. Miller, EIC
pelsnews@ieee.org

Front cover photo courtesy of West Japan Railway Company

President Column

Dear power electronic colleagues,

This will be my last column in our newsletter. Time to report on what we achieved over the past two years, summarize the work we still need to accomplish and last but not least introduce our incoming President.

As you remember from my first column last year, we embarked on preparing our global conference vision in lieu of our flagship conference PESC, which is scheduled for the last time 2008. Our vision to make strong regional conferences and to bundle conferences in North America, Europe and Asia became clearer and has been implemented for some part. Together with IAS-IPCSD we will organize in the US, starting from 2009 the Energy Conversion Congress and Expo. Together with APEC (in cooperation with IAS and PSMA), we will cover all aspects and applications (low to high power, automotive, household, power generation, transportation) of power electronics in the regions 1 to 7 (US and Canada). The first ECCE09 conference will be in San Jose, Sept. 20-24, 2009: mark your calendar! This year, we signed in Shanghai the MOA to jointly organize IPEMC'06 with the Chinese Electrotechnical Society, the largest society in our field in China. Next year, we will plan the same financial cooperation with the Korean Institute for Power Electronics (KIPE) and in 2008 with IEEJ to organize jointly a conference on power electronics, alternating on a three-year cycle in each country (China, Korea, Japan). In Europe, we started discussions, even forming committees, with leading associations to establish a joint international conference and Expo. I am convinced that we can serve better more members, especially from industry by teaming up with well-established associations. Furthermore, together with VTS we organize now a conference specifically dedicated to vehicle power and propulsion systems (VPPC). Representing PELS, I enjoyed attending VPPC06 in Windsor, UK. I highlöy recommend this IEEE conference to all those who still believe in electric vehicles: we shall overcome!

Needless, to say that the re-organization of our conference will also pose new responsibilities to our technical committees because they will provide our reviewer base not only for transaction paper review but also for the future conference. I am happy to report that all technical committees (TCs) are very active, organizing workshops, symposia, special issues, etc. We welcome all PELS members to become involved in the work of the TCs in particular industry members to support our standard committee.

Furthermore, PELS will keep supporting the International Future Energy Competition for students: the topics are out for next competition in 2007 (see: http://www.pels.org/ under "News"). Within Membership Development, we also started the Women in PELS (WIPELS) sub-committee, under guidance of Maria Pfeifer to promote power electronics and our society to female students and colleagues.

PELS is the only large society in IEEE that can claim a steady growth of membership of over 3.5% in the last two years. I really enjoyed helping out volunteers who came forward to start or reactivate their PELS Chapter. In particular, last August, I enjoyed opening the first Chinese PELS Student Chapter at Xi'an Jiaotong University. This is the second PELS student chapter in existence. During the inauguration ceremony, which coincided with tutorials organized by Prof. Jinjun Liu, I was able to invite well over 250 students to attend a President's dinner followed by a late night panel discussion organized on behalf of the Chinese PELS Student Chapter. I simply could not resist the enthusiasm of the Xi'an students and did not want to miss the opportunity to spend some of our society's money to a good cause. Besides, I had a good feeling about this as our society seeks projects (read spend money) to supports our members. When I got the bill, I was flabbergasted…the bill did not even exceed 250 $, i.e. 1 $ per person and let me assure you the food was good and plentiful! I am sure this will be an investment which we'll never beat again.

From January 2007 onwards, our President Elect, Hiro Akagi, Professor at Tokyo Institute of Technology, will become president of PELS. Being our first president from Region 9, our society once more showed its internationalism, anticipating further growth of membership, in particular in Region 9. I am convinced that we could not find a better candidate for the tasks at hand in Region 9 and I wish Hiro all the best and the same enthusiastic support which I experienced of our AdCom members, society officers, TC chairs and all society members. In particular, many thanks to our Society VPs, Grahame Holmes and Vassilios Agelidis. Thanks to our Newsletter Editor, John Miller and Transaction Editor-in-chief, Frede Blaabjerg, for all the great work and many hours they spent and keep spending on our publications. Thanks to Braham Ferreira, our treasurer, who had the difficult job of balancing the budgets. I also like to thank our Division Director, Bob Lorenz for his relentless support within IEEE and the Past PELS President, Dean Patterson for all his advice. All your help made it a great and unforgettable experience.

Looking forward meeting you at one of our next meetings.

Aachen, Sept. 2006

Rik De Doncker
IEEE PELS President

WIPELS Sub-Committee Created at last AdCom Meeting

The amazing thing about power electronics is that it is almost everywhere we look. As it is a major growth area within many industry applications, we need more qualified engineers in this field worldwide and, in fact, we need more women who can bring innovative ideas. However, being a woman in engineering is different from being a man in engineering. Not better, not worse, just different.

Currently, only 3% of all PELS active members are women! One may think the reason is because women are simply not interested in power electronics. I don't believe this, since even in developed countries girls are discouraged from careers in engineering, and particularly in electrical engineering, at a young age. So, it is often a social consequence.

For many years, the IEEE Women in Engineering Committee (WIEC) has done a lot of efforts to recruit women to engineering, increase the number of female IEEE members, educate current and future members, provide networking and mentoring opportunities and improve the climate for women in IEEE and the workplace.

In order to take advantage of the obtained results and joint WIE efforts for the benefit of the power electronics career, at the last meeting in Korea, PELS AdCom decided to start with the "Women in PELS (WIPELS)" as a sub-committee under membership development. This sub-committee will be our contact with WIE.

As chair of WIPELS, I invite interested female and male members of our society to join us! A lot of work has to be done to make our profession and PELS more attractive to women and to increase substantially membership of female colleagues. In a short-term, we may identify women working in the field and recruit them to PELS. In a long-term, we have to encourage young girls to hurdle the traditional barriers when they choose their career, enter their professional studies and begin their specialization.

WIE provides assistance through several of their activities. An important vehicle are the WIE Affinity Groups (AG), which represent the contact to local industry and academia. There are already 115 established AG all over the world with 9742 members (30% of them being men). Most of them are student branch affinity groups at universities. They host events like lectures, workshops, networking events and eweeks. We need to take advantage of AG established at universities offering the power electronics carrer.

We can request WIE to organize receptions at major PELS technical conferences to enhance networking and to promote their membership. And last but not least, we can participate in the IEEE STAR program (Student-Teacher and Research Engineer/Scientist Mentoring program) to mentor young women in junior and high schools and inspire them a positive image of electrical engineering careers. STAR has been developed and implemented in 1995 by the IEEE Electron Devices Society (EDS) and IEEE Microwave Theory and Techniques Society (MTT). In January 1998, all IEEE societies and sections were given the opportunity to offer the STAR Program to their respective members.

To achieve our goals, we need active WIPELS members and the involvement of local power electronics chapters as well.

Maria Cotorogea
WIPELS Chair

Announcement INTELEC® Fellowship

The INTELEC® Advisory and Conference Executive Committees sponsor the Joseph J. Suozzi INTELEC Fellowship in Power Electronics. This fellowship is named in honor of the late Dr. Joseph Suozzi, a founder and long-time leader of INTELEC. This grant of $10,000 is made annually to an electrical engineering graduate student studying in an area of power electronics applicable to communications systems. Such systems include wireline, optical, wireless or combinations of such systems such as the Internet or embedded telecommunications infrastructures. Alternative energy systems for communications networks or network elements is also a suitable area.

This fellowship is international and is therefore open to electrical engineering graduate students in all countries. It is a one-time grant to an individual and is not renewable.

Interested electrical engineering graduate students should submit:

- an essay not exceeding one page in length that explains how his/her proposed project can be applied to powering of communications systems
- a transcript of his/her grades
- a letter of support from his/her Faculty Advisor.

These materials should be sent by 1 February 2007 to the Chair of the IEEE Power Electronics Society Educational Activities Committee:

Leon M. Tolbert
Chair, PELS Education Activities Committee
The University of Tennessee
Electrical and Computer Engineering
311 Ferris Hall
Knoxville, TN 37996-2100 USA

The recipient of the 2007 INTELEC fellowship will be notified by 23 April 2007.

Vehicle Power and Propulsion Conference 2006, Windsor, England, UK

The 2006 IEEE Vehicle Power and Propulsion Conference (VPPC) was held at the Royal Windsor, England UK. Professor John Economou of Cranfield University, UK, was the General Chair of the conference. The VPPC Organizing Committee and its Steering Committee would like to thank the IEEE co-sponsoring societies VTS and PELS for their strong support. This year's conference was organized from three UK universities, Cranfield University, The University of Sheffield, and Manchester University. Professor David Howe, Dr Jiabin Wang, Dr Antonios Tsourdos, Dr Nigel Schoffield and the Dr John Economou worked together with their respective University colleagues for the delivery of a high quality and high class conference thus maintaining the co-sponsor societies standards and also delivering to the conference delegates a unique event in the area of electric vehicle power and propulsion. The program consisted of six keynote presenters from academia and industry who stimulated some very interesting discussions. Professor Anna Stefanopoulou, Professor C.C.Chan, Professor Mark Ehsani, Dr Peter Miller, Dr Thomas Keim, Mr Dominique Burton shared their views in their respective areas and stimulated an excellent debate. Professor's Bolognani and Professor Bianchi, Dr Peter Miller and Mr John West also contributed an excellent choice of Workshops, tutorials and interactive workshop sessions. This year over 100 delegates had the opportunity to attend the regular and special sessions with over 200 authors and co-authors. This year we were indeed pleased that the IEEE PELS President Professor Rik DeDoncker also attended VPPC 2006 and together with the VPPC Steering Committee Chair, Professor Mark Ehsani, and VPPC 2006 General Chair Dr John Economou welcomed the delegates during the opening ceremony.

By Prof. John Economou
VPPC2006 General Chair

IEEE Transactions on Power Electronics

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- Electronic ballasts for automotive applications
- Reduction of acoustic resonances in HID lamps
- Modeling of lamps and electronic ballasts
- Energy-saving and environmental-friendly issues in electronic ballasts
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Paper submission deadline: February 28, 2006
Planned publication date: May 2007

All the papers must be submitted, in electronic format through the Manuscript Central at http://mc.manuscriptcentral.com/tpel-ieee as described in the web http://www.pels.org

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Printed Circuit Board Design for Power Electronics

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I. INTRODUCTION

The role of the printed circuit board (PCB), today ubiquitous in power electronics, has changed substantially as power supplies have become more complicated. Originally used as a medium to connect components (the printed wiring board), current applications incorporating planar magnetic design and advanced thermal management treat the PCB as an integrated component of the power supply and may also include mixed analog and digital control signals.

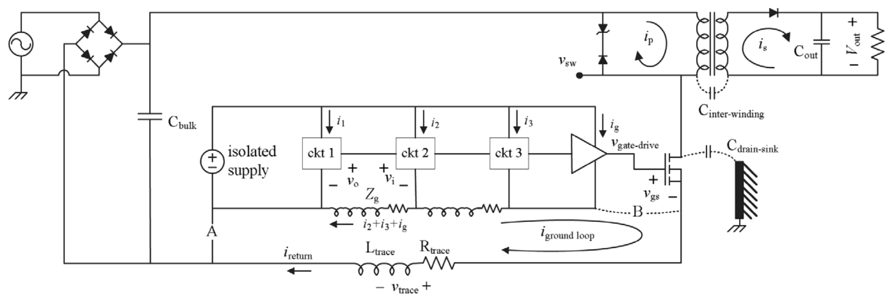

Fig. 1. Off-line flyback converter example

Engineers and managers not familiar with PCB design often mistakenly view it as a trivial process. Those familiar with the process, however, know that PCB design is an art as well as a science and that good PCB design involves more than simply converting an electrical netlist into copper traces. The skilled PCB engineer recognizes the importance of design for manufacturability, thermal management, safety, EMI, and regulatory compliance.

The design approach for PCBs in power electronic circuits differs significantly from the approach taken in digital or analog systems and requires careful attention to circuit details. For example, in a digital circuit, the PCB designer might first route buses and critical clock signals to ensure impedance control and uniform propagation delay. Power and ground, typically implemented as planes, receive lesser priority. In power electronics, there is no clear order in which to route traces. The circuit designer and the PCB designer must work together to identify the critical circuit nodes with high dv/dt, loops with high di/dt, sensitive analog control signals, and other special layout requirements such as heatsink placement and isolation requirements.

A designer can used a number of resources to guide the PCB development. Many suppliers to the industry provide application notes with guidelines directed specifically to power electronics PCBs [1-3]. There are standards that provide design recommendations specifically for PCBs [4-7] and also for the products containing the PCB [8-11]. Practical "how-to" books such as [12, 13] reduce to practice the black art of electromagnetic compliance. Many universities and professional development groups offer training in various aspects of the PCB design process. Finally, the designer is encouraged to directly contact his or her PCB vendor to learn of any special manufacturing requirements and limitations. Many vendors provide a free design for manufacturability (DFM) service.

Before beginning a PCB design, it is important to consider the intended use of the PCB. Because the printed circuit board is a multipurpose component of a switching power supply it is integral to the electrical connectivity, mechanical coupling, thermal management, and assembly of the switching power supply. Each of these roles places different requirements of the design of the PCB. Although this article is not meant to be comprehensive or to be used as a substitute for proper engineering design and review, it does highlight some of the electrical issues in printed circuit board design for power electronics.

II. CIRCUIT CONSIDERATIONS

The off-line flyback converter topology shown in Fig. 1 is a good choice for low power applications when input-to-output isolation on one or more output voltages is required. However, proper circuit operation requires tight coupling in the transformer which introduces significant inter-winding capacitance, shown as a lumped capacitor in the figure. Safety regulations require isolation between the primary and secondary. The stored energy in the resulting increased leakage inductance must be dissipated when the main switch is turned off which requires a snubber across the main switch or a diode-clamp across the primary winding as shown in the figure. Flyback converters typically operate at frequencies greater than 50 kHz and generate high instantaneous voltages which can create electrical interference problems. Thus, the off-line flyback converter is a good example to illustrate some key aspects of PCB design for power electronics.

III. UNINTENTIONAL COUPLING

Electromagnetic interference (EMI) is most generally defined to be the unintentional coupling of signals and can occur between different circuits, inter-circuit coupling, or within a circuit, intra-circuit coupling. EMI has two requirements: a source and a coupling path. In power electronics, the sources are time-varying voltages and currents. The coupling path is through parasitic and un-modeled impedances – the so called "hidden schematic" [12]. The path can also be through field coupling where dv/dt couples by electrical field and di/dt couples by magnetic field. Because various coupling mechanisms many not always be obvious, many circuit designers consider electromagnetic compliance (EMC) to be a form of black magic. The "art" of EMC is to understand how circuit elements behave at high frequencies – well beyond the fundamental frequency of the switching power converter. This implies that the circuit designer must consider the unintended as well as the intended circuit design.

Switching frequency alone does not create an EMI issue. Rather, the important criterion is the time rate of change of voltages and currents. In the flyback topology in Fig. 1, the drain of the main switch experiences high dv/dt when the magnetizing current of the transformer is suddenly interrupted. When the FET is attached to a heatsink through an electrical insulator, a capacitor is inadvertently formed between the electrically live drain of the FET and the grounded heatsink. Fast switching devices, beneficial to minimize switching losses, create high dv/dt which injects common-mode current into earth ground through the drain-to-sink capacitor. The inter-winding capacitance in the transformer provides an additional common-mode path for current induced by the FET drain voltage dv/dt through the output of the converter.

EMI is also generated by di/dt in loops containing switch elements including the main switch, output rectifier, transformer clamp, and gate drive ciruit. To prevent unintentional coupling, first identify nodes with high dv/dt and loops with high di/dt. Then, place components to shorten these critical paths and minimize loop areas. Avoid using 90 degree corners which exhibit current crowding at the inside edge and sharp corners with high electric field strengths. Instead, use 45 degree corners or smooth bends for the most critical traces. While placing and routing these EMI emitting circuits, also consider the placements and routing of EMI susceptible circuits that include voltage references, feedback circuits, current sensing circuits, PWM control circuits, and clock signals.

A. Switching induced ground-bounce

An example of intra-circuit conducted EMI is the ground-bounce often observed in the gate-drive portion of a switching power supply. In Fig. 1, the circuit designer followed the "single-point ground" rule and coupled the gate-drive power supply to the converter circuit common at point A. The circuit is deceptively simple because the "low-side" switch appears to be referenced to the control common. However, the current ireturn in the return trace from the FET to the bulk capacitor causes a voltage drop vtrace in series with the FET vgs and output of the gate drive vgate-drive. This compromises proper switching. Tying the control common directly to the FET source terminal at point B bypasses the impedance of the return trace but introduces an undesirable ground loop iground_loop -if the connection at A is not removed.

B. Polluted Ground

Another example of intra-circuit EMI occurs when power is routed to circuit components in a daisy-chain configuration as shown in Fig. 1. This can be particularly troublesome when one or more circuit elements draw pulsed-power such as in the gate-drive. The current pulses flowing through the impedance of the ground trace Zg cause a gradient in the ground potential between circuits. The input voltage vi and the output voltage vo of interconnected circuits no longer share a common reference. When this occurs in a control circuit, undesirable switching of the power converter may result. It is better to use a radial architecture where each subsystem has its own power and ground trace originating from the common isolated supply. Proximally routing the traces minimizes loop area and mutual inductance. This strategy keeps pulsing currents from corrupting sensitive analog control voltages.

IV. SAFETY ISSUES

Power conversion products are subject to many safety regulations [8-11] which vary among different countries. In addition to the general requirements of UL840 and IEC61010-1, designers must be aware of more stringent product-specific requirements such as UL508C and EN50178 for motor drives.

Spacing is the most relevant safety concern for PCB design. The space required between any two conductors, or a conductor and a metallic object, depends on the differential voltage between them, the common-mode voltage to ground, the materials involved, and the type of circuit involved. For example, much greater spacing is required between conductors that are energized directly from the mains (the power circuit) than between conductors on the secondary side of a transformer. European standards add additional spacing requirements for electrical conductors that directly affect personnel safety – so called touch-proofing. Generally, spacing between the power circuit and user circuits must be two to three times greater than the spacing within the power circuit itself.

Consider the example flyback converter in Fig. 1. A safety barrier is required between the primary and the secondary of the transformer if the output is accessible to the user. This implies solid insulation within the transformer and significant spacing on the PCB. The high voltage across the primary also requires spacing between its terminals greater than manufacturability issues alone would dictate. This additional space results in increased leakage inductance and reduced overall circuit performance. Similarly, the tab of the MOSFET is connected to the drain terminal, and so is electrically live. If the heat sink is earthed, substantial spacing and insulation is required. If the heat sink is instead connected directly to the MOSFET tab, then the spacing or insulation is required elsewhere within the product design. Heat sinks are also better electromagnetic radiators than MOSFETs alone, so EMC may suffer.

When a project involves research rather than product development, these regulatory requirements are often neglected. A good designer, however, considers the spirit of the requirements and follows them as much as possible. Remember, personnel safety is involved – nobody wants a student or researcher to be electrocuted or other laboratory equipment affected by operation of the experimental design. In this sense, the European philosophy should be applied: minimal spacing within a live circuit, but large spacing between live circuits and the user. If the design is intended for long-term testing, environmental factors that may promote dendrite growth or tracking on the PCB should also be considered and spacing increased.

V. CONCLUSION

Whether in a production environment or a research laboratory, printed circuit boards are ubiquitous in the modern switching power supply design. A well designed board provides improved performance and shorter manufacturing time compared to other assembly techniques. However, power electronics circuits present special challenges for the PCB designer that differ from other applications. Proper planning, consideration of current loops and stray capacitance, and an understanding of regulatory requirements early in the design will help the design process go smoothly.

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Robert S. Balog (S'92—M'96) received the B.S. degree in electrical engineering from Rutgers – The State University of New Jersey, New Brunswick, in 1996 and the M.S. degree in electrical engineering from the University of Illinois at Urbana-Champaign (UIUC) in 2002 where he is currently pursuing the Ph.D. degree in electrical engineering.

He was an engineer at Lutron Electronics, Coopersburg, Pa from 1996 through 1999. Now, at the University of Illinois, he is a Research Assistant as well as a Teaching Assistant for the power electronics laboratory class. He holds one issued U.S. patent and has an additional pending.

Mr. Balog is a registered professional engineer in Illinois. He was the first Fellow of the International Telecommunications Energy Conference (IEEE, 2002), an Ernest A. Reid Fellow (UIUC) for outstanding contributions to education (2003), and is currently a Harriett & Robert Perry (UIUC) Fellow. He is a member of Eta Kappa Nu, the Electric Manufacturing and Coil Winding Association, the Illinois Society of Professional Engineers, and the National Society of Professional Engineers.

Jonathan W. Kimball (M'96—SM'05) received the B.S. degree in electrical and computer engineering from Carnegie Mellon University in 1994 and the M.S. degree in electrical engineering from the University of Illinois at Urbana-Champaign (UIUC) in 1996.

He was an engineer at Motorola for two years designing IGBT modules. He was then a design engineer at Baldor Electric for four years designing industrial drives ranging from 1 hp to 150 hp. He returned to UIUC in 2003 as a Research Engineer. He is also the Vice-President of Engineering for SmartSpark Energy Systems, Inc., a power electronics start-up company based in Champaign, IL. Research interests include industrial drives, low-voltage high-current power supplies, battery management, and magnetic design.

Mr. Kimball is a registered professional engineer in Illinois and is a member of Eta Kappa Nu, Tau Beta Pi, and Phi Kappa Phi.

Call for Papers: 2007 IEEE Sensors Applications Symposium

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The 2007 IEEE Sensors Applications Symposium (SAS-2007) provides a unique forum for sensor users and developers to meet and exchange information about novel and emergent applications in smart sensors, biology, homeland security, system health management, and related areas. Collaborate and network with scientists, engineers, developers and customers, in a balance of formal technical presentations, workshops, and informal interface meetings-

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- Virtual sensors

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- Homeland security
- Multisensor data fusion
- Nondestructive evaluation and remote sensing
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- Commercial development

Additional topics for workshops and new session tracks are especially welcome-please contact the Program Chairs.

Important Dates:

01 October 2006:	Abstract submission deadline
01 December 2006:	Notification of acceptance
01 January 2007:	Final manuscript submission deadline

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High Power Electronics in Japan – Backgrounds and Applications

Tsuyoshi Funaki (Kyoto University)

Abstract

This article describes the current status of apparatuses based on high power electronics in Japan and explains the main motivations for developing and installing them. High-voltage dc links for interconnecting two power systems and the high speed electric train Shinkansen are provided as representative examples. While both of these power electronics apparatuses are not nouveau power electronics applications, they are representative of base technologies utilized to achieve high quality and reliability of the social infrastructure.

1. Introduction

Japan, located at the fringe of East Asia, has a land area of 377,835 km2 (placing the country around 60th in the world) and a population of about 127 million (a 2004 estimate placing it 10th in the world). The underground resource holdings in Japan, especially for fossil fuel, are basically non existent and the energy self-sufficiency rate is only 20% including the nuclear power plants (if excluding them, it becomes just 4%). Hence, energy savings while maintaining the quality of life is a compelling issue in Japan. Power electronics technology is one of the most important candidates to enable energy savings while at the same time adding more functional capabilities. Therefore, most newly installed or upgraded equipment, ranging from microwatts to gigawatts, utilizes power electronics. This article focuses on high power electronics applications in Japan and describes the background to their development and installation. HVDC interconnections are given as examples of utility applications and the high-speed electric trains are examples for mass-transportation applications.

2. HVDC Systems in Japan

Economics of HVDC transmission become favorable for lines longer than about 500 km for overhead transmission or 50 km for underground transmission. The advantages are the simple transmission line configuration, fast and flexible control, and the elimination of reactive power generation challenges. These are offset by high converter station cost. These advantages rarely favor overhead dc transmission in Japan owing to limited available space. For underground transmission, HVDC represents a better technological alternative because the country consists of many islands surrounded by sea. Other merits of an HVDC interconnection are asynchronous operation of interconnected power systems and full power flow control, which cannot be attained by conventional ac transmission. Although the land area of Japan is small, its electric power consumption, supplied by 9 privatized utility companies, is large. There are 7 HVDC interconnections in Japan as listed in Table 1. The

Table 1. HVDC link facilites in Japan

No	Name	ratings		type	running-in
		voltage (kV)	power (MW)		
1	Sakuma	125	300	FC-BTB	1965
2	Shin-Shinano	125	600	FC-BTB	1977
3	Hokkaido-Honshu	±250	600	Submarine cable	1979
4	Minami-Fukumitsu	125	300	BTB	1999
5	Kii Channel	±250	1,400	Submarine cable	2000
6	Higashi-Shimizu	125	10	FC-BTB	2006

Figure 1

number of HVDC interconnections is large for such a small land area, but there are historical reasons as well as technical advantages.

At the beginning of electricity commercialization in 1887. a synchronous generator of 50 Hz manufactured in Germany was imported and installed in Tokyo. However, a U.S.-manufactured synchronous generator of 60 Hz was adopted in Osaka. As a result, power systems in the eastern part of Japan evolved as 50 Hz and those in the western part as 60 Hz. Hence, electricity in Japan is divided into two parts as shown in Fig. 1. Furthermore, the 60 Hz western part has a surplus of generation capacity while the 50 Hz eastern part has insufficient reserve capacity. Hence, it is necessary to interconnect both parts to establish the required reliability and flexibility of operation. Same-frequency power systems are easy to interconnect under synchronous operation, but different-frequency power systems cannot be interconnected directly. Therefore, HVDC systems without a dc transmission line are utilized for interconnecting ac systems of different frequencies to enable interchanging electric power. Currently, there are 3 frequency converter (FC) stations in Japan. The Sakuma FC began service in 1965, and was the first HVDC system in Japan. It utilized mercury arc valves manufactured by ASEA because high power thyristors were not available at that time. This station was refurbished with direct light triggered thyristor valves in 1993. The Shin-Shinano FC, rated at 300 MW, began service in 1977. The electric triggered thyristor valves were designed for oil insulation and oil cooling in an outdoor installation. The station capacity was expanded to 600 MW in 1992. For this expansion, direct light triggered thyristor valves were used in an air-insulated, water-cooled configuration. The Higashi-Shimizu FC, whose thyristor valves are shown in Fig. 2, is the latest HVDC station in Japan. It entered service in March 2006. The direct light triggered thyristor valves shown in Fig. 2 are air-insulated, water-cooled, and configured for indoor installation. Two 6-pulse converter units are connected in series at the dc bus and in parallel at the ac bus with wye-wye and delta-wye converter transformers to obtain 12-pulse operation. One arm consists of 4 modules with each module having 7 thyristors connected in series.

Figure 2

Japan is surrounded and divided by sea. Although Honshu, the main island, and the northern island of Hokkaido have the same operating frequency (i.e., 60 Hz), they were not interconnected until 1979 because they are separated by the Tsugaru channel. Since 1979, they have been interconnected by the 150 MW Hokkaido-Honshu HVDC link consisting of a submarine cable and an overhead line. The rated capacity was upgraded to 300 MW in 1980 and to 600 MW in 1993. The Minami-Fukumitsu back-to-back (BTB) converter station is an asynchronous dc link of 300 MW installed in 1999. The purposes of this BTB interconnection are to break loop connections of the ac network and to permit flexible control of power flow. A multi-variable automatic frequency controller (AFC) is included to suppress frequency fluctuations after a disturbance. The Kii-Channel HVDC system is also an asynchronous dc link rated 1,400 MW. This link was installed in 2000 to match the increased power generation capacity of newly established coal-fired power plants. The line uses a 50 km long and 500 kV high voltage dc submarine cable and a 50 km overhead dc transmission line. The power modulation control adopted for this HVDC system enhances damping of low frequency oscillations among interconnected ac power systems after a disturbance.

Table 2. Major specification of Shinkansen train

Type	300 sereis	500 sereis	700 sereis
Train formation	10M 6T	16M	12M 4T
Switching device	GTO	GTO	IGBT
Rated power	12,000 kW	17,600 kW	12,960 kW
Maximum design speed	270 km/h	300 km/h	285 km/h

3. High-Speed Train by Variable Frequency Drive

The transportation system in Japan is very extensive, and includes an elaborate rail network. The airline network is well established, but the high-speed Shinkansen train network is competitive owing to punctuality, convenient access, and a good match to modest travel distances within Japan. The original Shinkansen, which connects the two most populous cities - Tokyo and Osaka - in 4 hours and covers a distance of 514 km, was established in 1964 independent from the existing railroad lines. It has been extended since then, and currently the Shinkansen network has 6 routes as shown in Fig. 3 covering a total distance of approximately 2,000 km. The entire network is electrified with a 25 kV ac trolley line. The maximum speed of the train was 200 km/h at the beginning of its service, but it has been raised to 300 km/h thanks to not only weight savings in the rail cars but also the application of power electronics. Table 2 gives the specifications of the Tokaido-Sanyo Shinkansen train.

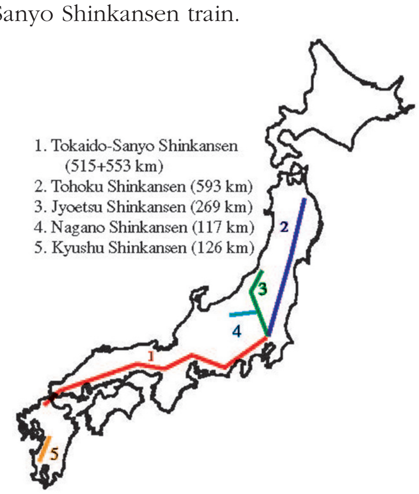

Figure 3

The 300 series train is the first Shinkansen that utilizes induction motor drives that incorporate variable frequency inverters. Each inverter consists of 4.5 kV 2,500 A GTOs. The 10 motor cars and 6 trailer cars can run at a maximum speed of 270 km/h, which reduced the travel time

Figure 4

between Tokyo and Osaka to about 2 hours 30 minutes. This train is equipped with a regenerative braking system, which is realized by a PWM-controlled self-commutated rectifier.

The 500 series train in Fig. 4 was developed to reduce further the travel time by increasing the acceleration performance and maximum speed. To this end, 4.5 kV 3,000 A GTOs were utilized in the variable frequency inverters and all 16 cars were motorized. The total output power of the motor drives reaches 17,600 kW. This type of train entered service in 1997 with a maximum speed of 300 km/h, which at that time was the fastest train in the world.

The high-speed capability of the 500 series train was realized at the expense of ride quality and cost. The 700 series train was then developed to satisfy both high-speed travel objectives and improved on-board amenities. It utilizes three-level IGBT inverters for the variable frequency induction motor drives. Total output power is 12,960 kW with 12 motor cars and 4 trailer cars. Although the maximum speed of the train was reduced to 285 km/h, the noise generated from the power electronics equipment was considerably suppressed by the application of high frequency switching to the IGBTs. Thus, the travel experience was improved thanks to reduced vibration and acoustic noise.

A high-speed train network is realized not only by vehicle technology, but also by excellent system operation technology. All trains are equipped with ATC (automatic train control) and supervised by CTC (centralized traffic control). Tight schedule coordination and precise traffic control enables trains to run every 5 minutes. The average delay is only about 1 minute.

4. Conclusions

This article discussed the background and motivations for apparatuses based on high power electronics used in Japan and provided two examples; namely, HVDC interconnection systems and the Shinkansen high-speed rail network. Power electronics has high impact within a well-coordinated system since it is an enabler for energy savings in countries like Japan that are basically net energy importers.

Acknowledgements

The authors acknowledge the materials supplied by Mr. H. Ishikawa (Chubu Electric Power Co., Inc) and Mr. H. Iijima (West Japan Railway Company).

Authors Bio

Tsuyoshi FUNAKI, was born 1969 in Japan. He got Bachelor, Master and PH. D degree from Osaka University in Electrical Engineering. He joined Osaka university electrical engineering department as a research associate on 1994, and was promoted to assistant professor on 2001. He moved to Kyoto university electrical engineering department as an associate professor on 2002.

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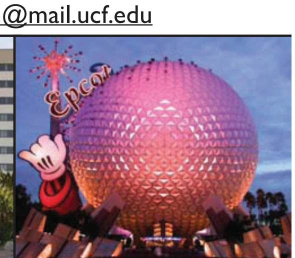

RMS Value Determination of Phase Current in Full-Bridge Rectifiers With Capacitive Filter Using a Parabolic Approximation

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Abstract---In the present article a method to determine the Root Mean Square (RMS) value of phase currents in rectifier circuits with capacitive filters, using a parabolic approximation, is shown. The methodology to compute the RMS value of capacitor current is proposed, and two numerical examples to demonstrate the approach validity are presented.

Introduction

In most modern electronic systems (low or high power) that are fed from a net, it is common to find a full-bridge rectifier (three-phases or single-phase) with a capacitive filter. As it is well-known, this allows to generate a DC voltage starting from an AC voltage. This circuit arrangement generates a pulsating phase current that also generates the increase of resistive losses in the net, a decrease of power factor, etc. In Figure 1, the three-phase and single-phase rectifier circuits are shown, with the respective phase currents corresponding to a generic phase.

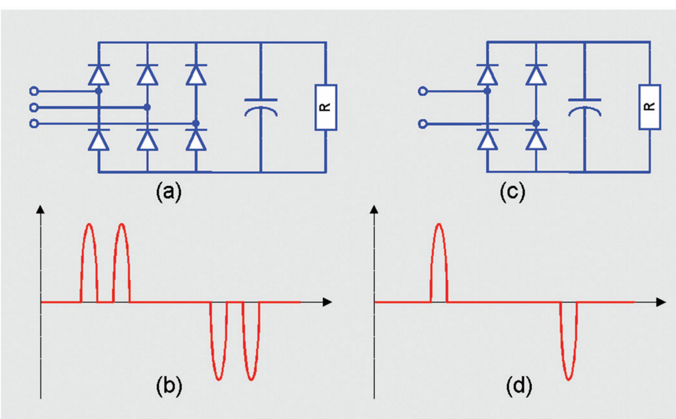

Figure 1 (a) Three-Phase full-bridge rectifier; (b) Phase current in the three-phase rectifier; (c) Single-Phase full-bridge rectifier; (d) Phase current in the single-phase rectifier.

It is well-known that each pulse of phase current could be approximated with a parabolic function [1], allowing this a bigger theoretical simplicity since the real current possesses quite complex expressions [2], [3]. However, it is not really known how and when to use such parabolic approach. Indeed, and according to the author's knowledge, it has not been referenced in the English literature yet. In the existent bibliography, it has not been specified any method, and the ones exposed is only limited to the single-phase rectifiers in a very simplified fashion [1]. In this article the determination of RMS value of phase current is described, by a parabolic approach. In Figure 2, a current pulse corresponding to the phase current $i_P(t)$ is shown, with a generic superimposed parabolic approximation.

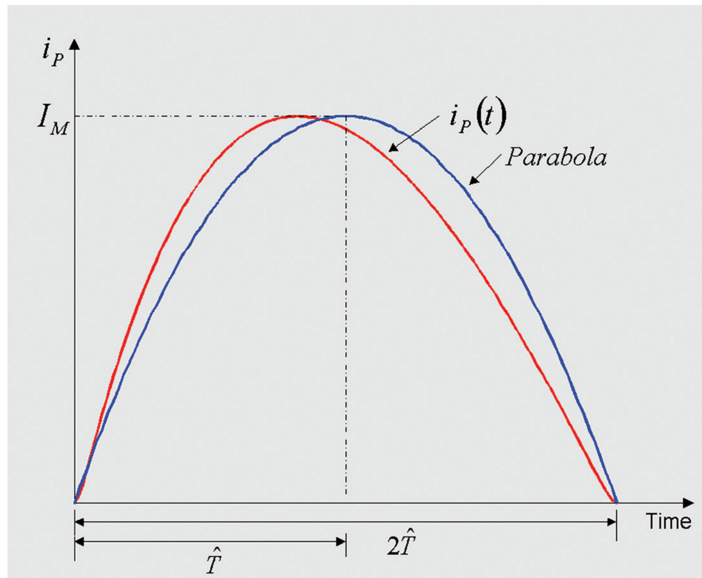

Figure 2 Pulse of phase current in a full-bridge rectifier with capacitive filter, and the respective parabolic approximation.

The equation for the approximating parabola shown in Figure 2 is

$$i(t) = I_M \left(\frac{2t}{\hat{T}} - \frac{t^2}{\hat{T}^2} \right) \tag{1}$$

Where, I_M is the peak value of current pulse; $\hat{T}$ is half of conduction time of such a pulse.

As we could observe in Figure 2, the characteristics of the parabola are:

1) to possess the same height that the current pulse (I_M);
2) to possess the same width that the current pulse ($2\hat{T}$).

With these characteristics, it is possible to see that the areas under such curves are very similar, and consequently the generated error in the integration process to compute the RMS value is reduced.

RMS Value of Phase Currents

Three-Phase Rectifier. As we could observe in Figure 1 (b), the phase current is composed by four pulses in one period. Due to this reason, the RMS value considering the parabolic approximation, is:

$$\tilde{I}_P = \sqrt{\frac{4}{T}\int_0^{2\hat{T}} i^2(t)\,dt} = 8 I_M \sqrt{\frac{\hat{T}}{15T}} \tag{2}$$

Where T is the current period.

Equation (2) shows that to obtain the RMS value of phase current, it is only necessary to know the peak value of current pulse and the width of such a pulse. These parameters could be obtained, for example, by measuring then in any oscilloscope.

NOTE: In all equations the upper symbol ~ indicates RMS value.

Single-Phase Rectifier. Applying the precedent approach to the single-phase rectifier, and considering that the same one possess two current pulses in one period (Fig. 1), the RMS value is:

$$\tilde{I}_P = \sqrt{\frac{2}{T}\int_0^{2\hat{T}} i^2(t)\,dt} = I_M\sqrt{\frac{32\hat{T}}{15T}} \tag{3}$$

The reader could ask: Is the three-phase pulse of similar type to the single-phase pulse? The answer is: Yes, and it is possible to verify such an affirmation in the examples below. Moreover, it is possible to deduce from Fig. 1 that both phase currents are described by the same differential equation type [2]-[3].

Suggestions. Like in any approximation, in general, in Figure 2 it is easy to observe that the approximation with a parabola is not perfect, but an approach of this type is defined as "good" [1]. The reader could judge about the quality of the approximation considering the examples below. The quality of such approximation depends on the constants of rectifier circuit in a complex form, but it is mainly influenced by the load resistance. When the load resistance decreases, considering constant filter capacity, the pulse peak of real current shifts toward the left (see Fig. 2), and the approximation is less efficient, increasing the error. It is normal to find, in practice, situations where the errors are lower than 5%. Naturally, the error could be larger, depending on each case. A possible error indicator is given by the distance between the peak of the current and the peak of the parabola (see Fig. 2). When such a distance diminishes, the precision of the approximation increases. Note that the peak of the parabola always coincides with half of the conduction time ($\hat{T}$).

A consideration to keep in mind is the one corresponding to the measuring of current pulse width (conduction time). In general, the beginning and the end of the current pulse are shaped by "rounded lines", as it is shown in Figure 3. Therefore, the method shown in Figure 3 is the more convenient one to measure the conduction time.

RMS Value of Capacitor Current

Naturally, the parabolic method allows us to compute other circuit parameters like the average value of the current in a half cycle, and the RMS value of capacitor current. For this last one, it should be considered the following current relationship: the output current of the bridge is equal to the sum of capacitor current plus the load current.

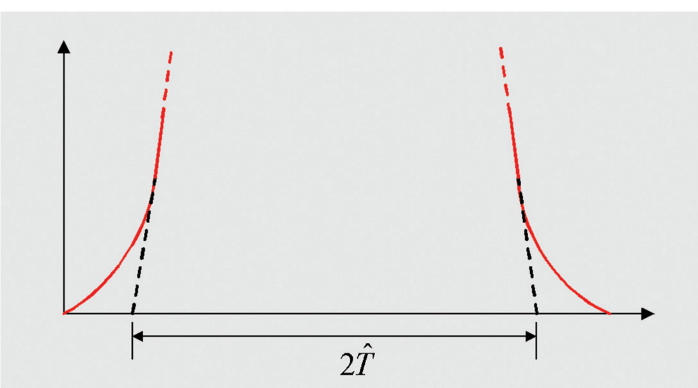

Figure 3 Measuring the conduction time of current pulse.

Therefore, the current in the capacitor is approximately: $i_C \cong i_0 - \bar{I}$. With this expression we proceed to compute the RMS value of capacitor current, considering that for the three-phase case such current has 6 pulses, and for the single-phase case 2 pulses, in one period. For the pulse we obviously use the approximation (1). The results, for the three-phase and single-phase rectifiers respectively are:

$$\tilde{I}_{CT} = \sqrt{\left(\frac{32}{5}I_M^2 - 16 I_M \bar{I} + 12\bar{I}^2\right)\frac{\hat{T}}{T}} \tag{4}$$

$$\tilde{I}_{CS} = \sqrt{\left(\frac{32}{15}I_M^2 - \frac{16}{3} I_M \bar{I} + 4\bar{I}^2\right)\frac{\hat{T}}{T}} \tag{5}$$

Where, $\bar{I}$ is the average load current, considered constant (null ripple) in the integration processes.

If the filter is composed by n paralleled capacitors, the RMS current of each single capacitor is obviously $\tilde{I}_C/n$. It is important to remember that the RMS value of capacitor current is a primordial design parameter.

Examples

In the two following numerical examples we would like to show the kindness of the parabolic approach, in the three-phase and single-phase rectifiers, respectively. In order to do so, digital simulations with PSpice software of two typical 50Hz examples are shown. The simulations allow us to know the different circuit variables with precision, and thus to compare the simulated values with the approximated ones. We consider the simulated RMS values as true.

a) In Figure 4 an example of three-phase pulse corresponding to a generic phase current, with its RMS value, is shown. In such a figure, it is observed that:

$$I_M = 14.3\text{A} \quad \hat{T} = 320\mu s \quad \tilde{I}_P = 3.56\text{A}$$

Using Equation (2), we have:

$$\tilde{I}_{P(approx)} = 3.74\text{A} \qquad \Delta\tilde{I}_P \cong 5\%$$

b) In the same way for Figure 5, showing a single-phase pulse, we have:

$$I_M = 10.87\text{A} \quad \hat{T} = 686\mu s \quad \tilde{I}_P = 2.89\text{A}$$

Using Equation (3), the results are:

$$\tilde{I}_{P(approx)} = 2.94\text{A} \qquad \Delta\tilde{I}_P \cong 1.7\%$$

In both precedent examples $\tilde{I}_{P(approx)}$ indicates the approximate RMS values to distinguish these from the simulated ones.

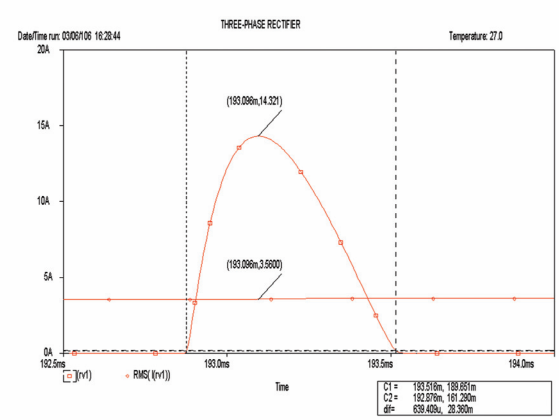

Figure 4 Three-phase pulse of phase current and RMS.

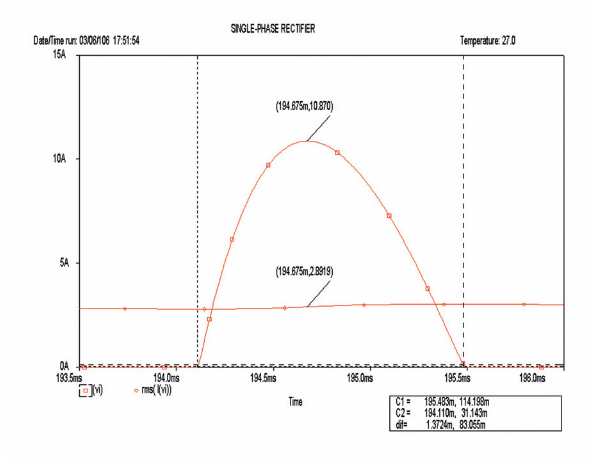

Figure 5 Single-phase pulse of phase current and RMS.

With this information, the reader could have a more clear vision regarding the parabolic approach.

Conclusions

In this article, we have exposed the method of determination of RMS value of phase current in the three-phase and single-phase rectifiers with capacitive filters, by means of a parabolic approximation. The method demonstrates to be very simple to be applied. Two numerical examples shown that such a method is applicable in three-phase and single-phase rectifiers.

The increase of approximation error due to the displacement to the left of current's pick value is observed in Figure 4, as it was previously exposed.

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[2] J. C. A. Floriani, "Analysis of a Full-Bridge Rectifier with Capacitive Filter, First Part: Single-phase Rectifier", Nueva Telegrafica Electronica, N° 29, pp. 174-178, Buenos Aires, 1998 (in Spanish).

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Juan Carlos A. Floriani (M'98) was born in Santa Fe, Argentina. He has received the Engineer degree in Electronics from U.T.N., Córdoba, Argentina, in 1985, and the Doctor Engineer degree in Electronics from the Polytechnic of Milan, Italy, in 1997. From 1986 to 1989 he has been with the Electronics Department of U.T.N., Córdoba, Argentina. From 1989 to 1990 he has worked like Designer Engineer of SMPS, in Selcom Elettronica, Bologna, Italy. From 1990 to 1996 he has worked like Designer Engineer of electrical drives, in Vickers Casella, Italy (currently is a Moog factory). From 1999 to 2003 he has been with the Computer Department of U.N.L., Santa Fe, Argentina. His areas of interest are Power Electronics, Electrical Drives and Applied Control. Dr. Floriani is author of a book on SMPS (in Spanish).

Book Review: Electromagnetic Compatibility

David A. WESTON, EMC Consulting Inc., Merrickville, Ontario, CANADA
Principles and Applications
Marcel Dekker, Taylor and Francis Group, 2nd edition, 2001
864 pp B5, 900 figs and tb., $123. ISBN : 0-8247-8889-3

All electronic and electrical equipment, and especially switching ones, is a source of more or less severe electromagnetic interference (EMI). Hence the challenges grow of ensuring the electromagnetic compatibility (EMC) of products and systems, that is making them function properly together. Books about this subject are then **necessary**.

The book with similar title authored by K.L. Kaiser [1] and published by CRC Press is an encyclopaedia, good for those who know or want to know in depth a large domain. This book is a **handbook, useful for those who teach, learn, or must solve a practical problem** in a given delay. This book is written for the design/system engineer, technician, or engineering manager who designs, maintains, or specifies equipment to meet an EMC requirement or to operate safely in a given environment. The book fits for **technical libraries**.

The presentation is clear, useful for applications, with many figures, tables and graphics, and case studies. Programs are included for field calculation. Equations are mentioned when they are invaluable in EMI prediction and EMC design.

This book covers key topics involved in EMC:

- E and H near and far fields, typical EMI sources, radiated and conducted emissions, noise immunity, antenna coupling, EMI measurements and prediction techniques, electromagnetic field shielding, cable shielding, grounding and bonding,
- crosstalk between PCB wires and cables, printed circuit board layout for EMC, non-ideal R L C, electrical equivalent length, wire impedance,
- american and european, military and commercial standards, explanation of technical data meaning, minimum theoretical basis necessary for using them correctly. The aim has been to avoid the overly simplistic cookbook approach, and yet to limit the mathematics to that used by the practicing engineer or technician.

The book is based on experience gained in EMC consulting, EMC teaching and answers to many questions posed by clients and by seminar attendees. The numerous references provided allow the user further study, if necessary.

This second edition is revised, updated and much enlarged, mainly with figures, formulas and computer programs.

1. Kenneth L. KAISER, **Electromagnetic Compatibility Handbook**, CRC Press, Taylor and Francis Group, end Sept. 2004, 2600pp B5, 2300 tb and figs., $150. ISBN : 0-8493-2087-9. Review published in PELS Newsletters, vol. , n° /200 .

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- **Notification of paper acceptance** **15 July 2007**
- **Tutorial proposal deadline** **15 July 2007**
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Several tutorials will be held prior to the technical presentations. Speakers, who are interested in delivering a tutorial, please contact the PEDS'07 Secretariat.

Exhibition

A comprehensive exhibition will be held during the conference. Exhibitors will include participants from commercial firms and organizations involved in the manufacturing, sales or distribution of power electronics equipment and professional or technical services. If interested in exhibiting, please contact PEDS'07 Secretariat.

Meetings of Interest

CIEP 2006, International Power Electronics Congress, to be held 16-18 October 2006 in Puebla, Mexico with venue Universidad de las Americas Puebla. CIEP is co-sponsored by IEEE Power Electronics Society. For more information visit the website at www.udlap.mx/electronica/ciep2006/ or contact Dr. Pedro Banuelos-Sanchez at pbanuelo@mail.udlap.mx for more information.

The 22nd Annual IEEE Applied Power Electronics Conference, APEC®2007, is scheduled for 25 Feb. through 1 March, 2007 at the Disneyland Hotel, Anaheim, CA. Co-sponsored by IEEE PEL's, IEEE IAS and Power Sources Manufacturers Association. See announcement in this issue. For more information visit the website at: www.apec-conf.org.

4th Power Conversion Conference, PCC2007 will be held 2-5 April 2007 at the Nagoya Congress Center, Nagoya, Japan. Important dates: author's notice of acceptance 30 November 2006, and final paper due 31 January 2007. For more information please visit the PCC'07 website: http://www.ics-inc.co.jp/pcc/

International Electric Machines and Drives Conference, IEMDC 2007, is scheduled for 3-5 May 2007 in Antalya, Turkey. IEMDC 2007 is jointly sponsored by the IEEE Power Electronics Society. For more information, please visit the conference website http://www.iemdc07.org/ or contact the General Chair, Okyay Kaynak kaynak@boun.edu.tr or the Technical Chair, Herb Hess, hhess@ieee.org

The 38th IEEE Power Electronics Specialists Conference, PESC'07, is scheduled for 17-21 June, 2007 at the Hilton in the Walt Disney World® Resort, Orlando, FL. PESC'07 is sponsored by IEEE PEL's. Deadline for abstract and digest submission is 10 Nov. 2006. General Chair is Prof. Issa Batarseh, batarseh@mail.ucf.edu and technical program chair Prof. John Shen, johnshen@mail.ucf.edu. For more information visit the website at www.pesc-conf.org.

12th European Conference on Power Electronics and Applications, EPE2007, is scheduled for 2-5 Sept. 2007 in Aalborg, Denmark. Intending authors should note these deadlines: receipt of synopses by 1 Nov.1, 2006, notification of acceptance March 1, 2007, final review May 15, 2007. Further information can be found at http://www.epe2007.com/

4th Vehicle Power and Propulsion (VPP) Conference is announced for Arlington, Texas from 9-12 September 2007 at the Wyndham Hotel in Arlington. Prospective authors are directed to the website for further details: http://www.vppc07.com/ and notified to submit proposal via that site. Important dates: April 1, 2007 for submission of the paper proposal (abstract and digest); June 1, 2006 author's notification of acceptance; August 1, 2007 for submission of camera-ready manuscript. VPP'07 general chair: Dr. Babak Fahimi, University of Texas-Arlington: fahimi@uta.edu VPP'07 is co-sponsored by PEL's.

International Telecommunications Energy Conference INTELLEC® rome'07 will be held 30 September to 4 October 2007 at the Rome Marriott Park Hotel, Rome, Italy.

5th Vehicle Power and Propulsion (VPP) Conference is announced for 3-5 September 2008 in Harbin, China. Correspondence may be directed to: vppc2008@hit.edu.cn. VPP'08 general chair: Prof. C.C. Chan, Harbin Institute of Technology. Abstracts with contact details should be submitted by 1 March 2008. VPP'08 is co-sponsored by PEL's.

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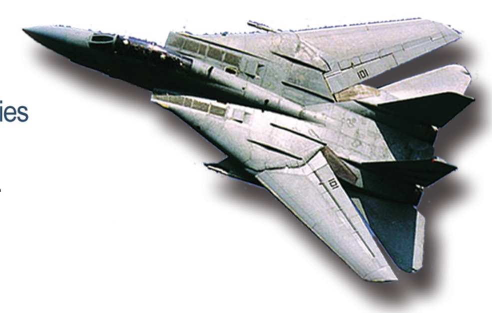

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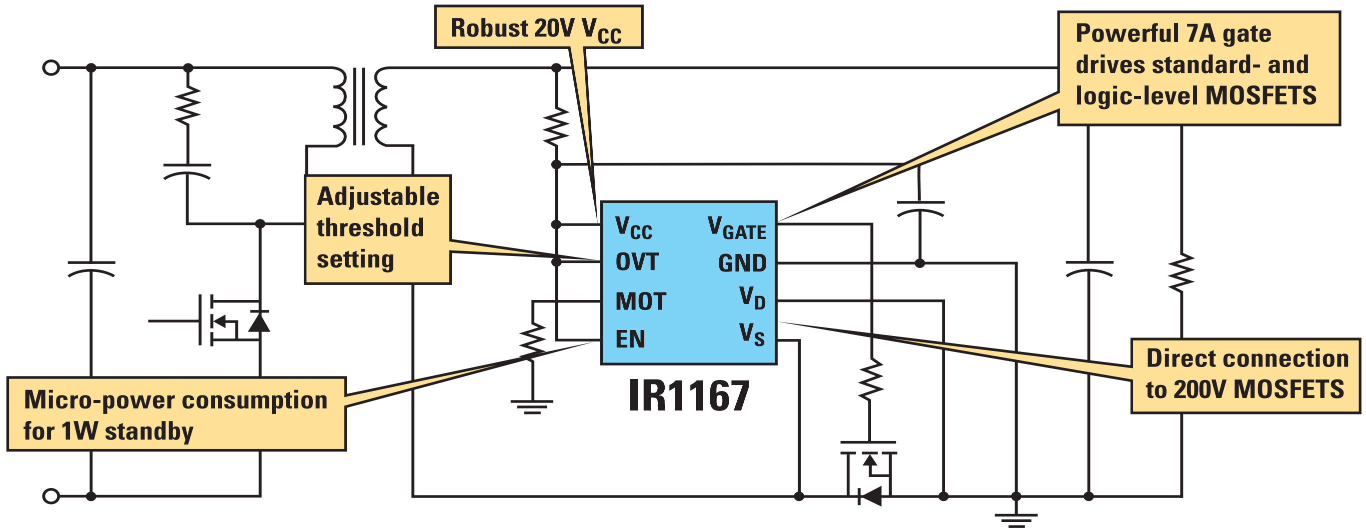
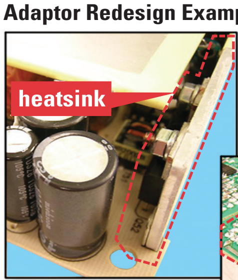


Adaptor Redesign Example:



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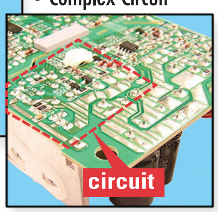
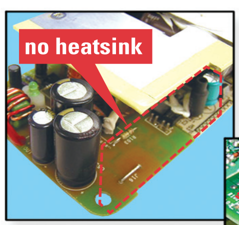
- Bulky Heatsink
- Current Transformer
- Complex Circuit





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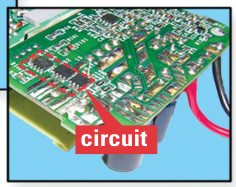

Specifications

Part Number	Package	V_{CC} (V)	V_{FET} (V)	Sw. Freq. Max. (kHz)	Gate Drive +/- (A)	V_{GATE} Clamp (V)	Sleep Current Max. (µA)
IR1167A/S	DIP-8/SO-8	20	<=200	500	+2/-7	10.7	200
IR1167B/S	DIP-8/SO-8	20	<=200	500	+2/-7	14.5	200

MOSFETS to use with the IR1167 SmartRectifier as a total chipset solution:

Part Number	V_{DSS} (V)	$R_{DS(on)}$ max @ 10V (mΩ)	Package
IRFB4110	100	4.5	TO-220
IRF7853	100	18	SO-8
IRFB4227	200	24	TO-220

Design Tools

A data sheet, application notes, technical papers and online design software are now available on IR's myPower™ site (http://www.irf.com/design-center/mypower/).

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- Works independently from primary-side control
- No current transformer required
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