



## *IEEE PES DSASC Test Feeder Working Group*

### **Minutes**

Meeting on July 26<sup>th</sup>, 2011  
2011 PES General Meeting, Detroit, MI

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A formal meeting of the DSASC Test Feeder Working Group was held at 2011 PES General Meeting. Fourteen participants were in attendance:

<b>Attendee</b>	<b>Affiliation</b>
Andrew Keane	University College Dublin
Bo Yang	General Electric
Chee-Wooi Ten	Michigan Technology University
Yonghe Cuo	Michigan Technology University
Greg Shirek	Milsoft Utility Solutions
Bikash Pal	Imperial College London
Kevin Schneider	Pacific Northwest National Laboratory
Jason Fuller	Pacific Northwest National Laboratory
Roger Dugan	Electric Power Research Institute
Sukumar Brahma	New Mexico State University
Jignesh Solanki	West Virginia University
Sandoval Cameiro Jr.	Federal University of Rio de Janeiro
Ilhan Kocar	Ecole Polytech
Sarika Khushalani-Solanki	West Virginia University
Jason Taylor	Electric Power Research Institute
Tom McDermott	Meltran



## Action Items

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1. Sandoval to look at 80 node network model to see if it is applicable as a new networked test feeder.
2. Roger (and all) to look for someone to generate a one-line diagram of larger networked test feeder.
3. Greg (and all) to start short circuit analysis on radial test feeders.
4. Find someone able/willing to validate Bill's comprehensive test feeder.
5. Tom to post DG protection fuse curves in a general format.

## Contact Information

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Working Group Chair: Roger Dugan ([rdugan@epri.com](mailto:rdugan@epri.com))

Working Group Secretary: Jason Fuller ([jason.fuller@pnl.gov](mailto:jason.fuller@pnl.gov))

Working Group Website: <http://ewh.ieee.org/soc/pes/dsacom/testfeeders/index.html>

## Test Feeder Working Group Meeting Minutes

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1. Roger led discussion of where the working group stands on the road map presented in Seattle 2009.
  - a. Neutral-Earth-Voltage test cases: Two now exist, and have been validated and posted on the working group website.
  - b. Short Circuit Benchmarks: Only DG case exists now. Forward motion is to post short circuit currents for every object in current test feeders (4-, 13-, 123-, etc.) with no loads, since this is standard for planning. If assumptions are made, please document and post assumptions also. Everyone will try to compare answers for possible presentation at T&D or GM.
  - c. DG Protection: Tom's case is posted (in his 2011 PSCE paper) but not validated or posted to website. Believe it is only missing the fuse curves to be complete.



- d. Large Distribution System: 8500 node system is completed, validated, and posted.
- e. Comprehensive Test Feeder: Posted but not tested.
- f. Inverter Based DG Models: EPRI has some in power flow, but not in the dynamic models (almost completed, possibly by end of year).
- g. Asymmetrical contingencies test feeder has not been addressed.
2. A lot of discussion was had about the networked test feeder.
  - a. Sandoval has a network system of approximately 80 buses and possibly with cable values and coordinates. This would be an in-between model from the large 2000 bus model presented.
  - b. Looking for someone who can generate a one-line diagram of 2000 bus system. Possibly if model is available in GIS or Roger has a lead on folks who might be able to do it using OpenDSS tool.
  - c. Follow up on whether cable data is available for 2000 bus network.
  - d. Jason, using Greg's data, to look at replacing sequence values with approximate cable data.
3. Greg will perform short circuit tests on existing IEEE test feeders. Should include all assumptions including (but not limited to) load assumptions, symmetrical faults components, impedances for regulators, fault impedance, fault voltages, etc. All others encouraged to do similar to validate results.
4. Roger to look at putting together a panel for T&D on new test models, possibly short circuit analysis. TBD.