



Electron Devices Technology and
Manufacturing Conference

EDTM 2017 PROGRAM

Toyama, Japan

Toyama International Conference Center

February 28 - March 2, 2017



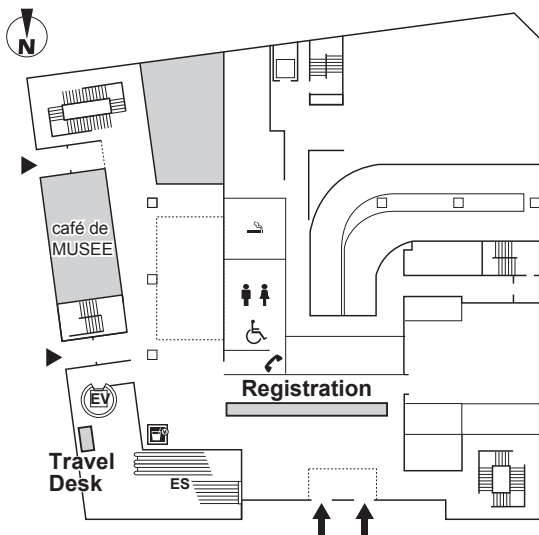
IEEE



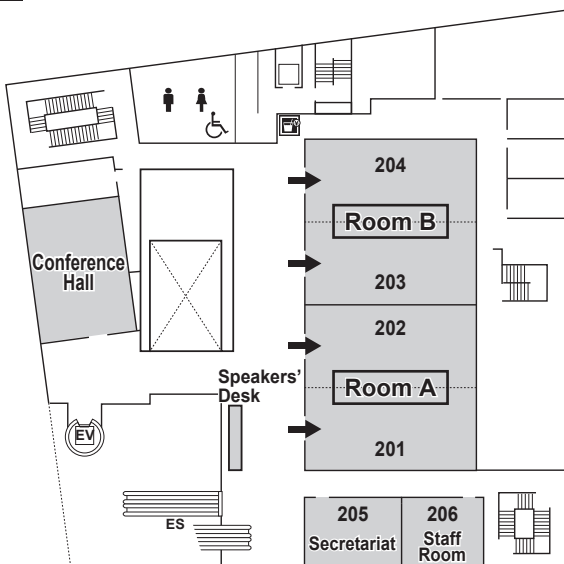
<http://ewh.ieee.org/conf/edtm/2017/>

Floor Map

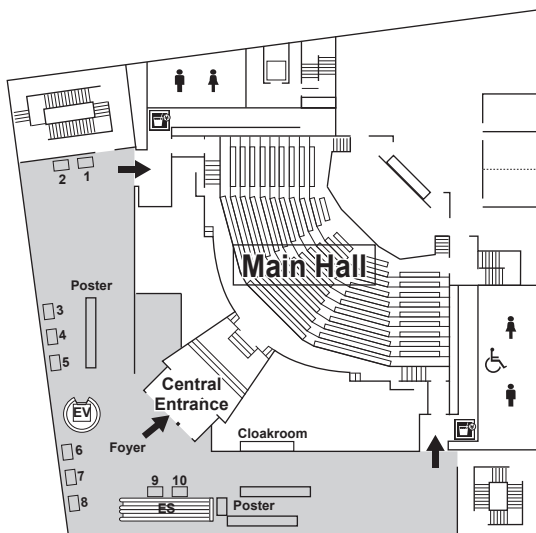
1F



2F



3F



Exhibition Booths

Booth No.

1. Yokogawa Solution Service Corporation
2. YONEKURA MFG Co., Ltd. / Tateyama Machine Co., Ltd.
3. National Institute of Advanced Industrial Science and Technology (AIST)
4. Advantec Co., Ltd.
5. TowerJazz Panasonic Semiconductor Co., Ltd.
- 6-7. Atomera Inc.
8. SCIVAX Corporation
9. Toshiba Corporation, Storage & Electronic Devices Solutions Company
10. Hitachi Kokusai Electric Inc.

Program at a glance

Day 1 - Tuesday, February 28

Time	Room A (201+202), 2F	Room B (203+204), 2F
8:30-8:45	Introduction	Introduction
8:45-10:15	Tutorial 1 (in Japanese) Nano Imprint	Tutorial 2 (in English) 3D Design and Process
10:15-10:30	Break	
10:30-12:00	Tutorial 1 (in Japanese) Adhesion and Bonding	Tutorial 2 (in English) 3D Design and Process
12:00-13:00	Break	
13:00-15:00	Short Course 1 Memory-Based Technology	Short Course 2 Advanced FET Technology
15:00-15:15	Break	
15:15-17:15	Short Course 1 Memory-Based Technology	Short Course 2 Advanced FET Technology
17:15-18:00	Lecturers Interview	
18:00-19:00	Reception @ Foyer, 3F / Exhibition	

Day 2 - Wednesday, March 1

Time	Main Hall, 3F	Room A (201+202), 2F	Room B (203+204), 2F
8:30-9:00	Opening Remarks		
9:00-11:00	Plenary Session		
11:00-12:00	Exhibition Talks		
12:00-13:35	Break (Poster display starts)	Luncheon Seminar	Break
13:35-15:40	Session 3M - Emerging: Emerging Technologies	Session 3A - Process: Process Technology for Advanced Devices	Session 3B - Modeling Reliability Analysis
15:40-15:55	Break		
15:55-18:25	Session 4M - Package: Subsystem Integration & Packaging	Session 4A - Material: Advanced FEOL Materials	Session 4B - Device: Advanced FET Technology
18:25-19:05	Authors Interview @ Main Hall / Poster Session @ Foyer, 3F		
19:15-21:15	Banquet @ Banquet Room "OHTORI", 3F, ANA Crowne Plaza Toyama		

Day 3 - Thursday, March 2

Time	Main Hall, 3F	Room A (201+202), 2F	Room B (203+204), 2F
08:30-10:10	Session 5M - Process: Innovative Process Tools	Session 5A - Device: More-than-Moore Technologies	Session 5B - Modeling: Multi Physics Simulation
10:10-10:25	Break		
10:25-12:05	Session 6M - Material: Advanced BEOL Materials	Session 6A - Device: FET Reliability	Session 6B - Modeling: Reliability & Modeling
12:05-13:00	Break		
13:00-14:20	Poster Session / Exhibition @ Foyer, 3F		
14:20-16:00	Session 7M - Modeling: Device Characterization	Session 7A - Device: Non-conventional Material- based FET Technologies	Session 7B - Process: Process Innovation in MEMS and Sensors
16:00-16:15	Break		
16:15-17:55	Session 8M - Device: Memory Technology	Session 8A - Process: Process Innovation on Ge Surface and Interface	
17:55-18:25	Authors Interview @ Main Hall		
18:25-19:25	Farewell Session / Best Poster Award Ceremony @ Foyer, 3F		

Social Events

Reception

Time & Date: 18:00-19:00, Tuesday, February 28

Venue: Foyer, 3F, Toyama International Conference Center

Banquet

Time & Date: 19:15-21:15, Wednesday, March 1

Venue: Banquet Room "OHTORI", 3F, ANA Crowne Plaza Toyama

*The venue is connected to the conference center on the first basement level.



Farewell Session / Best Poster Award Ceremony

Time & Date: 18:25-19:25, Thursday, March 2

Venue: Foyer, 3F, Toyama International Conference Center

Luncheon Seminar

Time & Date: 12:00-13:00, Wednesday, March 1

Venue: Room A (201+202), 2F, Toyama International Conference Center

Sponsor: SCIVAX Corporation

Instruction for Presentations

Instruction for Oral Presentations

Time Allocation for Presentations

	Presentation Time	Discussion Time	Total
Plenary	35 min	5 min	40 min
Invited	20 min	5 min	25 min
Oral	20 min	5 min	25 min
Tutorial 1	40 min	5 min	45 min
Tutorial 2	85 min	5 min	90 min
Short Course 1	55 min	5 min	60 min
Short Course 2	55 min	5 min	60 min

Audio Visual Equipment

PowerPoint will be the only method of presentation available in EDTM. Please provide slides with sufficient font size and contrast to ensure your text can be seen clearly from the back of large session rooms.

- Session rooms only support digital presentations using only one LCD projector.
- Please bring your power point file in a USB memory to the speakers' desk located on the 2nd floor. We recommend you to save the back-up data as a PDF file.
- It is necessary to upload and check your presentation data prior to 30 minutes of your session starts. Please complete it one day prior to the session if it is a first slot of the day.
- A Windows PC (with Windows 7, PowerPoint 2007, 2010, 2013, 2016) is available. If you are a Macintosh user or wish to use moving images, please bring your own PC. Please make sure to bring an AC adapter when you bring your PC.
- Your PC will be connected to the projector with a "15-pin, mini D-sub" cable. Some PCs (Macintosh or thin laptops) will require a conversion adapter.
- Please turn off the screen saver, power save mode.
- Set the resolution to XGA (1,024×768).
- After you finish your presentation, please receive your PC immediately inside the room.
- The Technical Program Committee will be responsible for deleting all copied data.

Speakers' Desk

Speakers' desk will open 8:00-17:00 from February 28 to March 2.

Before Presentation

Please be in the session room at least 15 minutes prior to your session so that you can make a short preparation with your session chairs. We will prepare a computer, a monitor, a microphone and a laser pointer on the podium in session rooms. Your presentation data will be automatically uploaded on the conference computer in advance.

On Presentation

You can control the slides on the podium. The presenting timer will be set so that you can easily find how many minutes you can use.

	Timer Window Indicates	Caution
Presentation starts	Allotted time ---> 3:00	GREEN light
Last 3 minutes	3:00 ---> 0:00	From Green to YELLOW light
Presentation finishes	0:00	From Yellow to RED light
Discussion starts	0:00 ---> 5:00 (count up)	

Authors Interview

Authors interview sessions are scheduled 18:25-19:05 March 1 and 17:55-18:25 March 2. Oral presenters of each day are requested to be in Main Hall, 3F and interact with the audiences.

Instruction for Poster Presentations

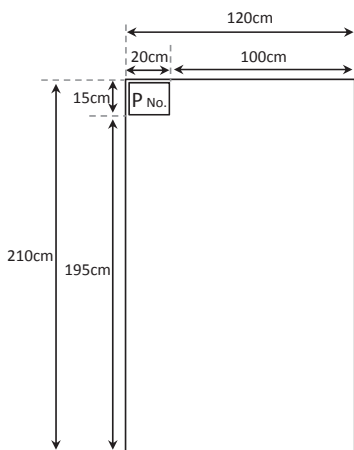
Poster Display and Removal

	Time and Date
Set-up	8:00 - 12:00, March 1
Presentation Time	18:25 - 19:05, March 1 13:00 - 14:20, March 2
Removal	14:20 - 16:00, March 2

On Presentation

Poster sessions will be held at the Foyer on the 3rd floor. Each poster presentation is allotted one poster board as shown below. All poster presenters are responsible for putting up and removing their posters on the designated board during the times shown in the table above. Posters remaining after the removal time will be removed and disposed by the Secretariat.

Please arrive at least 10 minutes ahead of the scheduled presentation time to check that all necessary supplies are present. One or more of the authors including a prime presenter should be present in front of the poster boards and be capable of explaining it.



The size of one poster board is 120cm wide x 210cm high.

Presenters should use pushpins to put up posters. Pushpins will be prepared by the Secretariat and provided in the poster area. Equipment or electricity for use of projector or computer animation accompanying a poster presentation will not be provided.

Tutorials

Tuesday, February 28, 2017

Tutorial 1 (in Japanese)

Moderator: A. Toriumi, The University of Tokyo

8:30 Introduction

“Nano Imprint”

8:45 ナノインプリント技術
S. Matsui, University of Hyogo

9:30 ナノインプリントリソグラフィ (NIL); 半導体応用
A. Mitra, Toshiba Corporation, Storage & Electronic Devices
Solutions Company

10:15 Break

“Adhesion and Bonding”

10:30 接着・粘着の基礎と応用
K. Horigome, Lintec Corporation

11:15 原子拡散接合法による室温接合技術
Room Temperature Bonding Using Thin Metal Films
(Atomic Diffusion Bonding)
T. Shimatsu, Tohoku University

Tutorial 2 (in English) *No handouts are distributed.

Moderator: F. Guarin, GLOBALFOUNDRIES Inc.

8:30 Introduction

“3D Design and Process”

8:45 Design for 2.5D- and 3D-Stacked ICs
P. D. Franzon, North Carolina State University

10:15 Break

10:30 Overview of Monolithic 3D IC Processing
Z. Or-Bach, MonolithIC 3D™ Inc.

Short Course 1

“Memory-Based Technology”

Tuesday, February 28, 2017

Moderator: A. Toriumi, The University of Tokyo

13:00 **Fundamentals for Resistance Switching RAM**
C. S. Hwang, Seoul National University

14:00 **ReRAM and PCM Device Structure and Technology**
D. Ielmini, DEIB – Politecnico di Milano and IU.NET

15:00 Break

15:15 **Nano-Scale Analog Synaptic Devices for Neuromorphic System**
H. Hwang, POSTECH

16:15 **Emerging Non-Volatile Memory (NVM) based Computing System**
S. Yu, Arizona State University

Short Course 2

“Advanced FET Technology”

Tuesday, February 28, 2017

Moderator: J. Ida, Kanazawa Institute of Technology

13:00 **Device Challenges in Advanced CMOS Technologies**
F. Bøeuf, STMicroelectronics, The University of Tokyo

14:00 **Gate Stack Reliability**
T. Grasser, Technische Universität Wien

15:00 Break

Moderator: T. Nabatame, NIMS

15:15 **Contact and Doping Technology for Advanced CMOS**
K.-W. Ang, National University of Singapore

16:15 **Characterization-Based Yield Engineering**
K. Nemoto, Hitachi High-Technologies Corporation

2017 IEEE Electron Devices Technology and Manufacturing Conference (EDTM)

Wednesday, March 1
Main Hall, 3F

8:30-9:00 Opening

Opening Remarks, Shuji Ikeda, EDTM 2017 General Chair, tei SOLUTIONS Inc.

9:00-11:00 Plenary Session

Chair: H. Wakabayashi, Tokyo Institute of Technology

PL-1 9:00-9:40 (Invited)

Dimensions of Innovation to Enable the Next Era of Intelligent Systems, John G. Pellerin, GLOBALFOUNDRIES Inc.

PL-2 9:40-10:20 (Invited)

Flexible and Printed OTFT Devices for Emerging Electronic Applications, Shizuo Tokito, Yamagata University

PL-3 10:20-11:00 (Invited)

Advanced Heterogeneous Integration Technology Trend for Cloud and Edge, Douglas C. H. Yu, Taiwan Semiconductor Manufacturing Company

11:00-12:00 Exhibition Talks

Chairs: K. Ishimaru, Toshiba Corporation
R. Arghavani, Lam Research Corporation

Ex-1 Hitachi Kokusai Electric Inc.

Ex-2 Toshiba Corporation, Storage & Electronic Devices Solutions Company

Ex-3 Atomera Inc.

Ex-4 National Institute of Advanced Industrial Science and Technology (AIST)

Ex-5 TowerJazz Panasonic Semiconductor Co., Ltd.

Ex-6 Yokogawa Solution Service Corporation

13:35-15:40 Session 3M - Emerging: Emerging Technologies

Chairs: B. Zhao, ON Semiconductor
H. Akinaga, AIST

3M-1 13:35-14:00 (Invited)

Future Computing Devices – Excitation, Physarum, Fluorics, Actin, Andrew Adamatzky, University of the West of England, Bristol

3M-2 14:00-14:25 (Invited)

Neuromorphic Technologies for Next-Generation Cognitive Computing, Robert M. Shelby¹, Pritish Narayanan¹, Stefano Ambrogio¹, Hsin-yu Tsai¹, Kohji Hosokawa², Scott C. Lewis³, and Geoffrey W. Burr¹,
¹IBM Research-Almaden, ²IBM Tokyo Research Laboratory, ³IBM T. J. Watson Research Center

3M-3 14:25-14:50 (Invited)

Stateful Logic Circuit and Material Using Memristors, Nuo Xu^{1,2}, Xinglong Shao¹, Kyung Jean Yoon¹, Hae Jin Kim¹, Kyung Min Kim³, and Cheol Seong Hwang¹, ¹Seoul National University, ²National University of Defense Technology, ³Hewlett Packard Enterprise

3M-4 14:50-15:15 (Invited)

New-Paradigm CMOS Ising Computing for Combinatorial Optimization Problems, Masanao Yamaoka, Hitachi, Ltd.

3M-5 15:15-15:40 (Invited)

Understanding the Limit and Potential in Emerging Perovskite Solar Cells, Wolfgang Tress and Michael Graetzel, Swiss Federal Institute of Technology (EPFL)

Wednesday, March 1
Room A (201+202), 2F

13:35-15:15 Session 3A - Process: Process Technology for Advanced Devices

Chairs: J. Yugami, Hitachi Kokusai Electric Inc.
X. Guo, Shanghai Jiao Tong University

3A-1 13:35-14:00 (Invited)

The Impact of Fin Number on Device's Performance and Reliability in Tri-Gate FinFETs, Wen-Kuan Yeh^{1,2}, Po-Ying Chen³, Chia-Hung Shih⁴, Wenqi Zhang¹, and Yi-Lin Yang⁵, ¹National University of Kaohsiung, ²National Applied Research Laboratories, ³National Chin-Yi University of Technology, ⁴National Pingtung University, ⁵National Kaohsiung Normal University

3A-2 14:00-14:25

Impact of e-SiGe S/D Processes on FinFET PFET TDDF Reliability, R. Ranjan, S. Uppal, H. Yu, B. Parameshwaran, T. Nigam, A. Kerber, C. LaRow, and M. I. Natarajan, GLOBALFOUNDRIES Inc.

3A-3 14:25-14:50

In Content Dependence of Pre-Treatment Effects on Al₂O₃/In_xGa_{1-x} as MOS Interface Properties, C. Yokoyama, C.-Y. Chang, M. Takenaka, and S. Takagi, The University of Tokyo

3A-4 14:50-15:15

Deep Junction by Low Thermal Budget Process for Advanced Si Power Electronics, Inès Toqué-Trésonne, Toshiyuki Tabata, Sébastien Halty, Fulvio Mazzamuto, Karim Huet, and Yoshihiro Mori, SCREEN Semiconductor Solutions Co., Ltd

Wednesday, March 1
Room B (203+204), 2F

13:35-15:40 Session 3B - Modeling: Reliability Analysis

Chairs: A. Oates, TSMC
S. Koul, Indian Institute of Technology Delhi

3B-1 13:35-14:00 (Invited)

Assessing Device Reliability Margin in Scaled CMOS Technologies Using Ring Oscillator Circuits, A. Kerber, S. Cimino, F. Guarin, and T. Nigam, GLOBALFOUNDRIES Inc.

3B-2 14:00-14:25

The Impact of RTN-Induced Temporal Performance Fluctuation Against Static Performance Variation, Takashi Matsumoto¹, Kazutoshi Kobayashi², and Hidetoshi Onodera³, ¹The University of Tokyo, ²Kyoto Institute of Technology, ³Kyoto University

3B-3 14:25-14:50

Critical Discussion on Temperature Dependence of BTI in Planar and FinFET Devices, P. Srinivasan and Tanya Nigam, GLOBALFOUNDRIES Inc.

3B-4 14:50-15:15

Characterization of Critical Peak Current and Model of Cu/Low-k Interconnects under Short Pulse-Width Conditions, M. H. Lin, W. S. Chou, Y. T. Yang, Y. C. Peng, and A. S. Oates, Taiwan Semiconductor Manufacturing Company

3B-5 15:15-15:40

New Analytical Equations for Skin and Proximity Effects in Interconnects Operated at High Frequency, Haojun Zhang, Jian-Hsing Lee, Natarajan Mahadeva Iyer, and Linjun Cao, GLOBALFOUNDRIES Inc.

Wednesday, March 1
Main Hall, 3F

15:55-18:25 Session 4M - Package: Subsystem Integration & Packaging

Chairs: S. Yamamichi, IBM
Y. Kurita, Toshiba Corporation

4M-1 15:55-16:20 (Invited)

System Integration in a Package for Cloud and Edge, Tadahiro Kuroda, Keio University

4M-2 16:20-16:45 (Invited)

III-V/Si Low Temperature Direct Bonding Technology for Photonic Device Integration on SOI, Nobuhiko Nishiyama, Yusuke Hayashi, Junichi Suzuki, and Shigehisa Arai, Tokyo Institute of Technology

4M-3 16:45-17:10 (Invited)

Focused Technologies in Near Future from OSAT View Point, Akio Katsumata, Akira Takashima, Kazuhiro Sawada, Hideki Sumihara, and Norio Ito, J-DEVICES Corporation

4M-4 17:10-17:35

BGA Packaging Process for a Device Made by Minimal Fab, Sommawan Khumpuang^{1,2}, Fumito Imura^{1,2}, and Shiro Hara^{1,2}, ¹National Institute of Advanced Industrial Science and Technology (AIST), ²Minimal Fab

4M-5 17:35-18:00

Electrodeposited Cobalt for Advanced Packaging Applications, Bryan Buckalew, Justin Oberst, and Thomas Ponnuswamy, Lam Research Corporation

4M-6 18:00-18:25 (Invited)

Packaging Design Considerations for Mobile and Internet of Things (IOT), Piyush Gupta, Qualcomm Inc.

Wednesday, March 1
Room A (201+202), 2F

15:55-18:00 Session 4A - Material: Advanced FEOL Materials

Chairs: I. Muneta, Tokyo Institute of Technology
P. Li, National Chiao Tung University

4A-1 15:55-16:20 (Invited)

Biocompatible ALD Barrier Coatings for Medical Devices, Mikko Matvejeff¹, Satu Ek¹, Riina Ritasalo¹, Jesse Kalliomäki¹, Päivi Järvinen¹, Oili Ylivaara², and Erik Östreng¹, ¹Picosun, ²VTT

4A-2 16:20-16:45 (Invited)

Enablement of Cost Effective CVD/ALD Processing through Precursor Design, Jean-Marc Girard, Air Liquide Advanced Materials Inc.

4A-3 16:45-17:10

Impact of Hydrogen Annealing Behavior of C₃H₅ Carbon Cluster Ion Implanted Projection Range Using Microwave Heat Treatment, Takeshi Kadono, Ryosuke Okuyama, Ayumi Masada, Ryou Hirose, Yoshihiro Koga, Hidehiko Okuda, and Kazunari Kurita, SUMCO Corporation

4A-4 17:10-17:35

New Opportunity of Ferroelectric Tunnel Junction Memory with Ultrathin HfO₂-Based Oxides, Xuan Tian and Akira Toriumi, The University of Tokyo

Wednesday, March 1
Room B (203+204), 2F

15:55-18:25 Session 4B - Device: Advanced FET Technology

Chairs: J. Ida, Kanazawa Institute of Technology
N. Horiguchi, imec

4B-1 15:55-16:20 (Invited)
Withdrawn

4B-2 16:20-16:45

Punch-Through Stop Doping Profile Control via Interstitial Trapping by Oxygen-Insertion Silicon Channel, Robert J. Mears¹, Hideki Takeuchi¹, Robert J. Stephenson¹, Marek Hytha¹, Richard Burton¹, Nyles W. Cody¹, Doran Weeks¹, Dmitri Choutov¹, Nidhi Agrawal^{2*}, and Suman Datta^{2**}, ¹Atomera Inc., ²Pennsylvania State University, ^{*}currently at Micron Technology Inc., ^{**}currently at Notre Dame University

4B-3 16:45-17:10 (Invited)

FinFET/Nanowire Design for 5nm/3nm Technology Nodes: Channel Cladding and Introducing a “Bottleneck” Shape to Remove Performance Bottleneck, Victor Moroz, Joanne Huang, and Munkang Choi, Synopsys, Inc.

4B-4 17:10-17:35

A Computational Study of Fundamentals and Design Considerations for Vertical Tunneling Field-Effect Transistor, Sheng Luo, Kain Lu Low, Xiaoyi Zhang, Qianyu Zhao, Hsin Lin, and Gengchiau Liang, National University of Singapore

4B-5 17:35-18:00

Analysis of Break-Even Time for Nonvolatile SRAM with SOTB Technology, Daiki Kitagata, Yusuke Shuto, Shuu'ichirou Yamamoto, and Satoshi Sugahara, Tokyo Institute of Technology

4B-6 18:00-18:25

Role of Floating Body Effect on Super Steep Subthreshold Slope PN-Body Tied SOI FET, Takahiro Yoshida, Jiro Ida, Syouta Inoue, Syougo Uchikura, Atsushi Hashimoto, Keisuke Hayashi, Taichi Iwasaki, Masanori Kamako, and Takashi Horii, Kanazawa Institute of Technology

18:25-19:05 Authors Interview in Main Hall, 3F
Poster Session in Foyer, 3F

*For Poster Session, please see the detailed information from page 22.

Thursday, March 2

Main Hall, 3F

8:30-10:10 Session 5M - Process: Innovative Process Tools

Chairs: K. Nojiri, Lam Research Corporation
Y. Kawasaki, SMIT

5M-1 8:30-8:55 (Invited)

EUV Lithography Insertion for High Volume Manufacturing: Status and Outlook, Alek Chen¹ and Junji Miyazaki², ¹ASML US Inc., ²ASML Japan Co., Ltd.

5M-2 8:55-9:20

Local, Isotropic, and Damageless Doping to Oxide Semiconductors by Using Electrochemistry, Takeaki Yajima, Tomonori Nishimura, and Akira Toriumi, The University of Tokyo

5M-3 9:20-9:45 (Invited)

Process Development for CMOS Fabrication Using Minimal Fab, Sommawan Khumpuang^{1,2}, Kazuhiro Koga^{1,2}, Yongxun Liu¹, and Shiro Hara^{1,2}, ¹National Institute of Advanced Industrial Science and Technology (AIST), ²Minimal Fab

5M-4 9:45-10:10

New Compact ECR Plasma Source for Silicon Nitride Film Formation in Minimal Fab System, Tetsuya Goto¹, Kei-ichiro Sato², Yuki Yabuta³, Shigetoshi Sugawa¹, and Shiro Hara⁴, ¹Tohoku University, ²Kotec Co., Ltd., ³Seinan Industries Co., Ltd., ⁴National Institute of Advanced Industrial Science and Technology (AIST)

Thursday, March 2

Room A (201+202), 2F

8:30-10:10 Session 5A - Device: More-than-Moore Technologies

Chairs: R. Huang, Peking University
K. Uchida, Keio University

5A-1 8:30-8:55

A Scalable Si-Based Micro Thermoelectric Generator, Takanobu Watanabe¹, Shuhei Asada¹, Taiyu Xu¹, Shuichiro Hashimoto¹, Shunsuke Ohba¹, Yuya Himeda¹, Ryo Yamato¹, Hui Zhang¹, Motohiro Tomita¹, Takashi Matsukawa², Yoshinari Kamakura³, and Hiroya Ikeda⁴, ¹Waseda University, ²National Institute of Advanced Industrial Science and Technology (AIST), ³Osaka University, ⁴Shizuoka University

5A-2 8:55-9:20 (Invited)

Health Monitoring of Houses and Communities by Recording Earthquake Response of Buildings, Minoru Yoshida¹, Yoichi Tanaka¹, Shoichi Ikeda¹, Soichiro Murata², Yoshiya Oda³, and Masatake Ushiro⁴, ¹Hakusan Corporation, ²SAP Japan, ³Tokyo Metropolitan University, ⁴Business Break-Through University

5A-3 9:20-9:45 (Invited)

Smart Biosensing Technologies to Detect Single Bacteria and Viruses, Masateru Taniguchi, Osaka University

5A-4 9:45-10:10

Strain-Engineering in Germanium Membranes Towards Light Sources on Silicon, D. Burt¹, A. Z. Al-Attili¹, Z. Li¹, F. Liu¹, K. Oda², N. Higashitarumizu³, Y. Ishikawa³, O. M. Querin⁴, F. Gardès¹, R. W. Kelsall⁴, and S. Saito¹, ¹University of Southampton, ²Hitachi, Ltd., ³The University of Tokyo, ⁴University of Leeds

Thursday, March 2
Room B (203+204), 2F

8:30-9:45 Session 5B - Modeling: Multi Physics Simulation

Chairs: A. Schenk, ETH Zurich
M. Natarajan, GLOBALFOUNDRIES Inc.

5B-1 8:30-8:55

Transient Characterization of Graphene NEMS Switch ESD Protection Structures, Qi Chen¹, Cheng Li¹, Jimmy Ng², Fei Lu¹, Chenkun Wang¹, Feilong Zhang¹, Rui Ma³, Ya-Hong Xie², and Albert Wang¹, ¹University of California, Riverside, ²University of California, Los Angeles, ³Intel

5B-2 8:55-9:20 (Invited)

Reliability Modeling of RF MEMS Switches and Phase Shifters for Microwave and Millimeter Wave Applications, Shibani K. Koul and Sukomal Dey, Indian Institute of Technology

5B-3 9:20-9:45 (Invited)

Multi-Scale and Multi-Domain Simulation of Electrical Power System, Shimeng Huang¹, Xiao Li¹, Tinghao Yeh², Shanghsun Mao², Takayuki Sekisue³, Vel Ambalavanar¹, and Sameer Kher¹, ¹ANSYS Inc., ²ANSYS Taiwan, ³ANSYS Japan

Thursday, March 2
Main Hall, 3F

10:25-12:05 Session 6M - Material: Advanced BEOL Materials

Chairs: S. Kim, Yeungnam University
P. R. Berger, Ohio State University

6M-1 10:25-10:50 (Invited)

Nano-Structure-Controlled Very Low Resistivity Cu Wires Formed by High Purity Electrolyte and Optimized Additives, Jin Onuki¹, Kunihiro Tamahashi¹, Takashi Inami¹, Takatoshi Nagano¹, Yasushi Sasajima¹, and Shuji Ikeda², ¹Ibaraki University, ²tei SOLUTIONS Inc.

6M-2 10:50-11:15

Withdrawn

6M-3 11:15-11:40 (Invited)

Advanced Materials and Interconnect Technologies for Next Generation Smart Devices, Rozalia Beica, Dow Electronic Materials

6M-4 11:40-12:05 (Invited)

Proximity Gettering Technology for Advanced CMOS Image Sensors Using C₃H₅ Carbon Cluster Ion Implantation Techniques, Kazunari Kurita, Takeshi Kadono, Ryosuke Okuyama, Ayumi Masada, Ryou Hirose, Yoshihiro Koga, and Hidehiko Okuda, SUMCO Corporation

Thursday, March 2
Room A (201+202), 2F

10:25-12:05 Session 6A - Device: FET Reliability

Chairs: G. Xiao, National University of Singapore
Y.-C. King, National Tsing Hua University

6A-1 10:25-10:50 (Invited)

New Visions for IC Yield Detractor Detection, Bill Nehrer, Kelvin Doong, and Dennis Ciplickas, PDF Solutions

6A-2 10:50-11:15

Comparative Study on RTN Amplitude in Planar and FinFET Devices, Zexuan Zhang¹, Zhe Zhang¹, Shaofeng Guo¹, Runsheng Wang¹, Xingsheng Wang², Binjie Cheng², Asen Asenov^{2,3}, and Ru Huang¹, ¹Peking University, ²Synopsys, Inc., ³University of Glasgow

6A-3 11:15-11:40 (Invited)

A BTI Analysis Tool (BAT) to Simulate p-MOSFET Ageing under Diverse Experimental Conditions, Souvik Mahapatra, Narendra Parihar, Subrat Mishra, Beryl Fernandez, and Ankush Chaudhary, Indian Institute of Technology Bombay

6A-4 11:40-12:05

Accurate Mapping of Oxide Traps in Highly-Stable Black Phosphorus FETs, Yu. Yu. Illarionov^{1,2}, G. Rzepa¹, M. Waltl¹, T. Knobloch¹, J.-S. Kim³, D. Akinwande³, and T. Grasser¹, ¹Technische Universität Wien, ²loffe Physical-Technical Institute, ³The University of Texas at Austin

Thursday, March 2
Room B (203+204), 2F

10:25-12:05 Session 6B - Modeling: Reliability & Modeling

Chairs: S. Huang, Peking University
M. Miura-Mattausch, Hiroshima University

6B-1 10:25-10:50 (Invited)

ESD Performance Enhancement Methodologies for CMOS Power Transistors, Mahadeva Iyer Natarajan and Jian-Hsing Lee, GLOBALFOUNDRIES Inc.

6B-2 10:50-11:15

Aging Simulation of SiC-MOSFET in DC-AC Converter, Kenshiro Sato, Shinya Sekizaki, Dondee Navarro, Yoshifumi Zoka, Naoto Yorino, Hiroshi Zenitani, Hans Jürgen Mattausch, and Mitiko Miura-Mattausch, Hiroshima University

6B-3 11:15-11:40

Degradation Caused by Negative Bias Temperature Instability Depending on Body Bias on NMOS or PMOS in 65 nm Bulk and Thin-BOX FDSOI Processes, Ryo Kishida and Kazutoshi Kobayashi, Kyoto Institute of Technology

6B-4 11:40-12:05

JFETIDG: A Compact Model for Independent Dual-Gate JFETs, Kejun Xia, Colin C. McAndrew, and Hanyu Sheng, NXP Semiconductors

13:00-14:20 Poster Session in Foyer, 3F

*For Poster Session, please see the detailed information from page 22.

Thursday, March 2

Main Hall, 3F

14:20-16:00 Session 7M - Modeling: Device Characterization

Chairs: P. Su, National Chiao Tung University
D. Navarro, Hiroshima University

7M-1 14:20-14:45 (Invited)

How Non-Ideality Effects Deteriorate the Performance of Tunnel FETs, Andreas Schenk¹, Saurabh Sant¹, Kirsten Moselund², and Heike Riel², ¹ETH Zurich, ²IBM Research-Zurich

7M-2 14:45-15:10

Charge Splitting In-situ Recorder (CSIR) for Monitoring Plasma Damage in FinFET BEOL Processes, Ting-Huan Hsieh, Yi-Pei Tsai, Chrong Jung Lin, and Ya-Chin King, National Tsing Hua University

7M-3 15:10-15:35

Geometric Variation: A Novel Approach to Examine the Surface Roughness and the Line Roughness Effects in Trigate FinFETs, E. R. Hsieh¹, Y. C. Fan², C. H. Liu², Steve S. Chung¹, R. M. Huang³, C. T. Tsai³, and T. R. Yew³, ¹National Chiao Tung University, ²National Taiwan Normal University, ³UMC

7M-4 15:35-16:00

A Novel Method to Characterize DRAM Process Variation by the Analyzing Stochastic Properties of Retention Time Distribution, Min Hee Cho, Namho Jeon, Moonyoung Jeong, Sungsam Lee, Satoru Yamada, and Hyeongsun Hong, Samsung Electronics Co., Ltd.

Thursday, March 2
Room A (201+202), 2F

14:20-16:00 Session 7A - Device: Non-conventional Material-based FET Technologies

Chairs: K. Xia, NXP Semiconductors
H. Lv, Chinese Academy of Sciences

7A-1 14:20-14:45

Analysis of Subthreshold Swing and Internal Voltage Amplification for Hysteresis-Free Negative Capacitance FinFETs, Pin-Chieh Chiu and Vita Pi-Ho Hu, National Central University

7A-2 14:45-15:10

Design Space Exploration Considering Back-Gate Biasing Effects for Negative-Capacitance Transition-Metal-Dichalcogenide (TMD) Field-Effect Transistors, Wei-Xiang You and Pin Su, National Chiao Tung University

7A-3 15:10-15:35

A Simple Way to Grow Large-Area Single-Layer MoS₂ Film by Chemical Vapor Deposition, Yan-Cong Qiao, Zhen Yang, Hai-Ming Zhao, Xue-Feng Wang, Lu-Qi Tao, Yi Yang, and Tian-Ling Ren, Tsinghua University

7A-4 15:35-16:00

High-Mobility and H₂-Anneal Tolerant InGaSiO/InGaZnO/InGaSiO Double Hetero Channel Thin Film Transistor for Si-LSI Compatible Process, Nobuyoshi Saito, Kentaro Miura, Tomomasa Ueda, Tsutomu Tezuka, and Keiji Ikeda, Toshiba Corporation

Thursday, March 2
Room B (203+204), 2F

14:20-16:00 Session 7B - Process: Process Innovation in MEMS and Sensors

Chairs: S. Tanaka, Tohoku University
M. Miura, Hitachi High-Technologies Corp.

7B-1 14:20-14:45 (Invited)

Growing Market of MEMS and Technology Development in Process and Tools Specialized to MEMS, Hiroshi Yanazawa and Kohji Homma, MEMS CORE Co., Ltd.

7B-2 14:45-15:10

Development of MEMS Vibrating Sensor with Phase-Shifted Optical Pulse Interferometry, Yusaku Ohe¹, Hitoshi Kimura¹, Norio Inou¹, Yoshiharu Hirayama², and Minoru Yoshida², ¹Tokyo Institute of Technology, ²Hakusan Corporation

7B-3 15:10-15:35

Microstructuring Polydimethylsiloxane Elastomer Film with 3D Printed Mold for Low Cost and High Sensitivity Flexible Capacitive Pressure Sensor, Bengang Zhuo, Sujie Chen, and Xiaojun Guo, Shanghai Jiao Tong University

7B-4 15:35-16:00

Effective Performance of a Tiny-Chamber Plasma Etcher in Scallop Reduction, Sommawan Khumpuang^{1,2}, Hiroyuki Tanaka^{1,2}, and Shiro Hara^{1,2}, ¹National Institute of Advanced Industrial Science and Technology (AIST), ²Minimal Fab

Thursday, March 2

Main Hall, 3F

16:15-17:55 Session 8M - Device: Memory Technology

Chairs: M. Saitoh, Toshiba Corporation
K. Tateiwa, TowerJazz Panasonic Semiconductor Co., Ltd.

8M-1 16:15-16:40

Exploiting NbO_x Metal-Insulator-Transition Device as Oscillation Neuron for Neuro-Inspired Computing, Ligang Gao, Pai-Yu Chen, and Shimeng Yu, Arizona State University

8M-2 16:40-17:05

Ohmic Contact Formation Between Ge₂Sb₂Te₅ Phase Change Material and Vertically Aligned Carbon Nanotubes, Panni Wang, Suwen Li, Yihan Chen, Lining Zhang, and Mansun Chan, Hong Kong University of Science and Technology

8M-3 17:05-17:30

Impact of Current Distribution on RRAM Array with High and Low I_{ON}/I_{OFF} Devices, Mohammed Zackriya V.^{1,2}, Albert Chin¹, and Harish M. Kittur², ¹National Chiao Tung University, ²VIT University

8M-4 17:30-17:55

3D Time-Contingent Physical Unclonable Function Array on 16nm FinFET Dielectric RRAM, Yi-Hung Chang¹, Po Shao Yeh¹, Yue-Der Chih², Jonathan Chang², Ya-Chin King¹, and Chrong Jung Lin¹, ¹National Tsing Hua University, ²Taiwan Semiconductor Manufacturing Company

Thursday, March 2
Room A (201+202), 2F

16:15-17:55 Session 8A - Process: Process Innovation on Ge Surface and Interface

Chairs: Y. Akasaka, TEL
O. Nakatsuka, Nagoya University

8A-1 16:15-16:40

Surface Preparation and Wet Cleaning for Germanium Surface, Masayuki Otsuji¹, Yukifumi Yoshida¹, Hiroaki Takahashi¹, Farid Sebaai², Kurt Wostyn², Frank Holsteyns², Masanobu Sato¹, and Hajime Shirakawa¹, ¹Screen Semiconductor Solutions Co., Ltd, ²imec vzw

8A-2 16:40-17:05

Oxidation Mechanism and Surface Passivation of Germanium by Ozone, Xiaolei Wang¹, Jinjuan Xiang¹, Chao Zhao^{1,2}, Tianchun Ye^{1,2}, and Wenwu Wang^{1,2}, ¹Chinese Academy of Sciences, ²University of Chinese Academy of Sciences

8A-3 17:05-17:30

The Impact of Atomic Layer Depositions on High Quality Ge/GeO₂ Interfaces Fabricated by Rapid Thermal Annealing in O₂ Ambient, Laura Žurauskaitė, Per-Erik Hellström, and Mikael Östling, KTH Royal Institute of Technology

8A-4 17:30-17:55

Experimental Investigation on Growth Mechanism of GeO_x Layer Formed by Plasma Post Oxidation Based on Angle Resolved X-Ray Photoelectron Spectroscopy, Zhiqian Zhao¹, Xiaolei Wang², Jing Zhang¹, Chao Zhao^{2,3}, Tianchun Ye^{2,3}, and Wenwu Wang^{2,3}, ¹North China University of Technology, ²Chinese Academy of Sciences, ³University of Chinese Academy of Sciences

17:55-18:25 Authors Interview in Main Hall, 3F

Wednesday, March 1 18:25-19:05

Thursday, March 2 13:00-14:20

Foyer, 3F

Poster Session

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UV-Annealing-Enhanced Stability in High-Performance Printed InO_x Transistors, William J. Scheideler and Vivek Subramanian, University of California Berkeley

P-2

Random-Telegraph-Noise by Resonant Tunnelling at Low Temperatures, Z. Li¹, M. Sot¹, F. Liu¹, M. K. Husain¹, I. Zeimpekis¹, H. Yoshimoto², K. Tani², Y. Sasago², D. Hisamoto², J. D. Fletcher³, M. Kataoka³, Y. Tsuchiya¹, and S. Saito¹, ¹University of Southampton, ²Hitachi, Ltd., ³National Physical Laboratory

P-3

Fabrication of E-Mode InGaN/AlGaN/GaN HEMT Using FIB Based Lithography, Shubhankar Majumdar^{1,3}, Chitrakant Sahu², and Dhrub Biswas³, ¹National Institute of Technology Raipur, ²Malaviya National Institute of Technology Jaipur, ³Indian Institute of Technology Kharagpur

P-4

Endurance Characterization of the Cu-Doped HfO₂ Based Selection Device with One Transistor-One Selector Structure, Qing Luo, Xiaoxin Xu, Hangbing Lv, Tiancheng Gong, Shibing Long, Qi Liu, Ling Li, and Ming Liu, Chinese Academy of Sciences

P-5

Investigation on Direct-Gap GeSn Alloys for High-Performance Tunneling Field-Effect Transistor Applications, Lei Liu¹, Renrong Liang¹, Guilei Wang², Henry H. Radamson², Jing Wang¹, and Jun Xu¹, ¹Tsinghua University, ²University of Chinese Academy of Sciences

P-6

Online Training on RRAM Based Neuromorphic Network: Experimental Demonstration and Operation Scheme Optimization, Peng Yao¹, Huaqiang Wu¹, Bin Gao¹, Ning Deng¹, Shimeng Yu², and He Qian¹, ¹Tsinghua University, ²Arizona State University

P-7

Uniformity Improvements of Low Current 1T1R RRAM Arrays through Optimized Verification Strategy, Shan Wang, Xinyi Li, Huaqiang Wu, Bin Gao, Ning Deng, Dong Wu, and He Qian, Tsinghua University

P-8

Electroluminescence Characteristics of Rare Earth Doped Silicon Based Light Emitting Device, Fumihiro Hattori¹, Hideyuki Iwata¹, Toshihiro Matsuda¹, and Takashi Ohzone², ¹Toyama Prefectural University, ²Dawn Enterprise Co., Ltd

P-9

High Photoresponsivity Germanium Nanodot PhotoMOSFETs for Monolithically- Integrated Si Optical Interconnects, Ming-Hao Kuo¹, Morris M. Lee², and Pei-Wen Li^{1,2}, ¹National Central University, ²National Chiao Tung University

P-10

The Impact of Oxygen Insertion Technology on SRAM Yield Performance, A. Marshall¹, S. Nimmalapudi¹, W. K. Loh², J. Krick³, L. Hutter⁴, H. Takeuchi⁵, R. Stephenson⁵, R. J. Mears⁵, and S. Ikeda⁶, ¹The University of Texas at Dallas, ²Consultant, ³Logix Consulting, Inc., ⁴Lou Hutter Consulting, ⁵Atomera Inc., ⁶tei SOLUTIONS Inc.

P-11

Transport Properties in Silicon Nanowire Transistors with Atomically Flat Interfaces, F. Liu¹, M. K. Husain¹, Z. Li¹, M. S. H. Sotito¹, D. Burt¹, J. D. Fletcher², M. Kataoka², Y. Tsuchiya¹, and S. Saito¹, ¹University of Southampton, ²National Physical Laboratory

P-12

InAs MOS-HEMT Power Detector for 1.0 THz on Quartz Glass, Eiji Kume¹, Hiroyuki Ishii², Hiroyuki Hattori², Wen-Hsin Chang², Mutsuo Ogura¹, Haruichi Kanaya³, Tanemasa Asano³, and Tatsuro Maeda², ¹IRspec Corporation, ²National Institute of Advanced Industrial Science and Technology (AIST), ³Kyushu University

P-13

Analysis and Modeling of Capacitances in Halo-Implanted MOSFETs, Chetan Gupta¹, Harshit Agarwal³, Sagnik Dey², Chenming Hu³, and Yogesh S. Chauhan¹, ¹Indian Institute of Technology Kanpur, ²Texas Instruments Inc., ³University of California Berkeley

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Design and Performance of Thin-Film μ TEG Modules for Wearable Device Applications, Tsuyoshi Kondo, Nana Chiwaki, and Satoshi Sugahara, Tokyo Institute of Technology

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Analysis of Spin Accumulation in a Si Channel Using CoFe/MgO/ Si Spin Injectors, Taiju Akushichi, Daiki Kitagata, Yusuke Shuto, and Satoshi Sugahara, Tokyo Institute of Technology

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SER Scaling and Trends in Planar Submicron Technology Nodes, Krishna Mohan Chavali, GLOBALFOUNDRIES Inc.

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Fully Packaged Compliant CMOS Electronic Systems for IoT and IoE Applications, G. A. Torres Sevilla, M. D. Cordero, J. M. Nassar, A. T. Kutbee, and M. M. Hussain, King Abdulla University of Science and Technology

P-18

A Metal Micro-Casting Method for Through-Silicon Via (TSV) Fabrication, Jiebin Gu, Bingjie Liu, Heng Yang, and Xinxin Li, Shanghai Institute of Microsystem and Information Technology

P-19

Acoustic Emission Wave Sensor with Thermally Controllable Force-Enhancement Mechanism for Acoustic Emission Source Detection and Biomedical Application, Guo-Hua Feng and Wei-Ming Chen, National Chung Cheng University

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Electroactive Polymer Actuated Gripper Enhanced with Iron Oxide Nanoparticles and Water Supply Mechanism for Millimeter-Sized Fish Roe Manipulation, Guo-Hua Feng and Shih-Chieh Yen, National Chung Cheng University

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Low Temperature Hermetic Sealing by Aluminum Thermocompression Bonding Using Tin Intermediate Layer, Shiro Satoh, Hideyuki Fukushi, Masayoshi Esashi, and Shuji Tanaka, Tohoku University

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Low-Carrier Density Sputtered-MoS₂ Film by H₂S Annealing for Normally-Off Accumulation-Mode FET, Jun'ichi Shimizu¹, Takumi Ohashi¹, Kentaro Matsuura¹, Iriya Muneta¹, Kuniyuki Kakushima¹, Kazuo Tsutsui¹, Nobuyuki Ikarashi², and Hitoshi Wakabayashi¹, ¹Tokyo Institute of Technology, ²Nagoya University

P-23

Impact of Ferroelectric Domain Switching in Nonvolatile Charge-Trapping Memory, Chia-Chi Fan¹, Yu-Chien Chiu¹, Chien Liu¹, Guan-Lin Liou², Wen-Wei Lai¹, Yi-Ru Chen¹, Chun-Hu Cheng², and Chun-Yen Chang^{1,3}, ¹National Chiao Tung University, ²National Taiwan Normal University, ³Academia Sinica

P-24

An In-Line MOSFET Process with Photomask Fabrication Process in a Minimal Fab, Norio Umeyama^{1,2}, Sommawan Khumpuang^{1,2}, and Shiro Hara^{1,2}, ¹National Institute of Advanced Industrial Science and Technology (AIST), ²Minimal Fab

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Development of a Half-Inch Wafer for Minimal Fab Process, Norio Umeyama^{1,2}, Atsushi Yamazaki³, Takaaki Sakai³, Sommawan Khumpuang^{1,2}, and Shiro Hara^{1,2}, ¹National Institute of Advanced Industrial Science and Technology (AIST), ²Minimal Fab, ³Fujikoshi Machinery

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Helium Ion Microscopy (HIM) for Imaging Fine Line Features Patterned Organic Film with Less Damage, Shinichi Ogawa¹, Tomoya Ohashi², Shigeki Oyama², and Yuki Usui², ¹National Institute of Advanced Industrial Science and Technology (AIST), ²Nissan Chemical Industries, Ltd.

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Supercritical Fluid Deposition of Conformal Oxide Films: 3-Dimensionally-Stacked $\text{RuO}_2/\text{TiO}_2/\text{RuO}_2$ Structures for MIM Capacitors, Yu Zhao, Yusuke Shimoyama, Takeshi Momose, and Yukihiro Shimogaki, The University of Tokyo

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Crystallinity Improvement Using Migration-Enhancement Methods for Sputtered- MoS_2 Films, Shin Hirano, Jun'ichi Shimizu, Kentaro Matsuura, Takumi Ohashi, Iriya Muneta, Kuniyuki Kakushima, Kazuo Tsutsui, and Hitoshi Wakabayashi, Tokyo Institute of Technology

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Low Power Transparent Resistive Switching Device with Memristive Behavior, Amitesh Kumar, Mangal Das, Rohit Singh, Pankaj Sharma, Abhinav Kranti, and Shaibal Mukherjee, Indian Institute of Technology Indore

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Photoresist Development for Wafer-Level Packaging Process, Makiko Irie, Toshiaki Tachi, and Atushi Sawano, Tokyo Ohka Kogyo Co., Ltd.

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Second-Harmonic Susceptibility Enhancement in Gallium Nitride Nanopillars, Kangwei Wang, Haoliang Qian, Zhaowei Liu, and Paul K. L. Yu, University of California, San Diego

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Defect Formation in SiO_2 Formed by Thermal Oxidation of SiC , Kenta Chokawa, Masaaki Araidai, and Kenji Shiraishi, Nagoya University

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Current Enhanced Solid Phase Precipitation (CE-SPP) for Direct Deposition of Multilayer Graphene on SiO_2 from a Cu Capped Co-C Layer, Hiroyasu Ichikawa and Kazuyoshi Ueno, ¹Shibaura Institute of Technology

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Enhanced Photoresponse of InGaZnO TFT to Ultraviolet Illumination by Using a High- k Dielectric, Libin Liu, Renrong Liang, Jing Wang, and Jun Xu, Tsinghua University

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Development of *in-situ* Sb-Doped $\text{Ge}_{1-x}\text{Sn}_x$ Epitaxial Layers for Source/Drain Stressor of Strained Ge Transistors, Jihee Jeon, Akihiro Suzuki, Kouta Takahashi, Osamu Nakatsuka, and Shigeaki Zaima, Nagoya University

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Novel *in-situ* Passivation of MoCl_5 Doped Multilayer Graphene with MoO_x for Low-Resistance Interconnects, K. Kawamoto, Y. Saito, M. Kenmoku, and K. Ueno, Shibaura Institute of Technology

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Thickness-Independent Behavior of Coercive Field in HfO₂-Based Ferroelectrics, Shinji Migita¹, Hiroyuki Ota¹, Hiroyuki Yamada¹, Akihito Sawa¹, and Akira Toriumi², ¹National Institute of Advanced Industrial Science and Technology (AIST), ²The University of Tokyo

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Crystallinity Study of Si Single Crystal Stripe on Bended Glass Substrate Fabricated by Micro-Chevron Laser Beam Scanning Method, Wenchang Yeh and Seigo Moriyama, Shimane University

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Physics Based System Simulation for Robot Electro-Mechanical Control Design, T. K. Maiti¹, L. Chen¹, M. Miura-Mattausch¹, S. K. Koul², and H. J. Mattausch¹, ¹Hiroshima University, ²Indian Institute of Technology Delhi

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Accurate Modeling of MOSFET Aging Based on Trap-Density Increase for Predicting Circuit-Performance Aging, Lei Chen, Hidenori Miyamoto, Tapas Kumar Maiti, Dondee Navarro, Takahiro Iizuka, Hans Jürgen Mattausch, and Mitiko Miura-Mattausch, Hiroshima University

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Modeling and Analysis of Depletion-Mode NMOS Transistor as Transmitter/Receiver RF Switch, Runtao Ning, Tianjiao Liu, and Z. John Shen, Illinois Institute of Technology

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An Analytical Charge-Sheet Drain Current Model for Monolayer Transition Metal Dichalcogenide Negative Capacitance Field-Effect Transistors, Renrong Liang, Chunsheng Jiang, Jing Wang, Jun Xu, and Tian-Ling Ren, Tsinghua University

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A Simple Test Method for Electromigration Reliability of Solder/Cu Pillar Bumps Using Flat Cables, Naoki Azuma¹, Misaki Owada¹, Takumi Abe¹, Tsutomu Nakada², Makoto Kubota², and Kazuyoshi Ueno^{1,3}, ¹Shibaura Institute of Technology, ²EBARA Corporation, ³Research Center for Green Innovation

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Perumal Ratnam, SanDisk / Western Digital
Sadayuki Yoshitomi, Toshiba
Lining Zhang, Hong Kong Univ. of Sci. and Tech.
Kenji Okada, TowerJazz Panasonic Semiconductor
Mahadeva Iyer Natarajan, GLOBALFOUNDRIES
Pin Su, National Chiao Tung Univ.
Kin Leong Pey, Singapore Univ. of Tech. and Design
Anthony S. Oates, TSMC
Inkook Jang, Samsung
Hisayo Sasaki Momose, Yokohama National Univ.