EDTM2020 - Preliminary Advance Program

As of January 29, 2020

Day 3 - Wednesday, March 18

08:30-10:00 Main Room (Matahari I, II, III)
Plenary Session 3
Chair: Jagadheswaran Rajendran

8:30	9:15	PL-6		Nanocarbon Interconnects - from 1D to 3D	Cary Y. Yang	Santa Clara University
9:15	10:00	PL-7		Industrial LED development: From red to UV and from efficient components to smart devices	David Lacey	Osram Opto Semiconductors

10:00-10:15 Main Room (Matahari I, II, III)
Short Break

10:15-12:20 Room A (Matahari I)
Session 7A Variability Modeling
Chairs: Subhash Rustagi, Paul Lining Zhang

10:15	10:40	7A-1		General Formula to Capture the Impact of Dummy Gates on Layout Dependent Effects Modeling of Multi-finger MOSFETs	Kejun Xia	NXP Semiconductors
10:40	11:05	7A-2		An Accurate Structure Generation and Simulation of LER Affected NWFET	Agam Jain	Indian Institute of Technology Roorkee
11:05	11:30	7A-3		Analysis on Process Variation Effect of 3D NAND Flash Memory Cell Through Machine Learning Model	Jang Kyu Lee	Seoul National University
11:30	11:55	7A-4		Superior Work Function Variability Performance of Horizontally Stacked Nanosheet FETs for Sub-7-nm Technology and Beyond	Akhil Sudarsanan	Indian Institute of Technology Hyderabad

12:20-13:20 Authors' Interview / Lunch Break (Rooms Etoile and Grand BR II)

10:15-12:20 Room B (Matahari III)
Session 7B Advanced Transistors
Chairs: Abhisek Dixit, Yukinori Morita

10:15	10:40	7B-1		Process-induced Vt Variability in Nanoscale FinFETs: Does Vt Extraction Methods Have Any Impact	Mandar S. Bhoir	IIT Gandhinagar
10:40	11:05	7B-2		Impact of LER on Mismatch in Nanosheet Transistors for 5nm-CMOS	Chandan Kumar Jha	IIT DELHI
11:05	11:30	7B-3		Possibility of Ultralow Power Rectenna with Super Steep SS "PN-Body Tied SOI FET" and High Impedance Antenna	Ryota Yanagi	Kanazawa Institute of Technology
11:30	11:55	7B-4		Digital Type CMOS-MEMS Cointegrated Pressure Sensor Fabricated Using Cost-Effective Minimal-Fab Process	Yongxun Liu	National Institute of Advanced Industrial Science and Technology (AIST)

12:20-13:20 Authors' Interview / Lunch Break (Rooms Etoile and Grand BR II)

10:15-12:20 Room C (Grand Ballroom I)
Session 7C Materials Processing
Chairs: Sanjiv Sambandan, Sanghun Jeon

10:15	10:40	7C-1	Invited	High Volume Semiconductor Manufacturing Using Nanoimprint Lithography	Yukio Takabayashi	CANON Inc.
10:40	11:05	7C-2	Invited	COTS Semiconductor Components for the New Space Industry	Harshad Bokil	Ispace
11:05	11:30	7C-3		Bi-Objective Indirect Optimization of Robotic Transportation Task Assignment Based on Auction Mechanism	Souleymane Moussa Goumeye	Lineact Cesi
11:30	11:55	7C-4	Invited	Switching and Charge Trapping in HfO2-based Ferroelectric FETs: An Overview and Potential Applications	Halid Mulaosmanovic	NaMLab gGmbH
11:55	12:20	7C-5		Ferroelectricity Enhancement in Hf0.5Zr0.5O2 Capacitors by Incorporating Ta2O5 Dielectric Seed Layers	Venkateswarlu Gaddam	Korea Advanced Institute of Science and Technology

12:20-13:20 Authors' Interview / Lunch Break (Rooms Etoile and Grand BR II)

10:15-12:20 Room D (Grand Ballroom III)
Session 7D 2D Materials and Devices
Chairs: Suprem Das, Nava Kanta Bhat

10:15	10:40	7D-1	Invited	Metals at the Atomic Limit	Joshua Robinson	The Pennsylvania State University
10:40	11:05	7D-2		Synthesis of MoS2(1-x)Te2x by Sputtering and the Change in the Physical Properties and Structure Depending on the Chalcogen Composition	Yusuke Hibino	Meiji University
11:05	11:30	7D-3	Invited	Inter-layer Charge and Energy Transfer in Layered Heterojunction Devices	Kausik Majumdar	Indian Institute of Science Bangalore India
11:30	11:55	7D-4	Invited	Electric-double-layer MoS2 Transistors and Their Neuromorphic Device Applications	Jie Jiang	Central South University

12:20-13:20 Authors' Interview / Lunch Break (Rooms Etoile and Grand BR II)

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13:20-15:00 Room A (Matahari I)
Session 8A Neural Network and NVM 2
Chairs: Wai Yie Leong, Chetan Arora

13:20	13:45	8A-1		Neural Network Based Design Optimization of 14-Nm Node Fully-Depleted SOI FET for SoC and 3DIC Applications	Hyeok Yun	POSTECH
13:45	14:10	8A-2		Graphene Muscle with Artificial Intelligence	Ning-Qin Deng	Tsinghua University
14:10	14:35	8A-3		Methodology to Predict Random Telegraph Noise Induced Threshold Voltage Shift Using Machine Learning	Eunseok Oh	Seoul National University
14:35	15:00	8A-4		Development of Non-Volatile Tunnel-FET Memory as a Synaptic Device for Low-Power Spiking Neural Networks	Hisashi Kino	Tohoku University

15:00-15:20 Authors' Interview / Coffee Break

13:20-15:00 Room B (Matahari III)
Session 8B Manufacturing and Characterization
Chairs: Bernard Lim, Keizo Hiraga

13:20	13:45	8B-1	Invited	Metrology and Inspection: Challenges and Solutions for Emerging Technology Nodes	Arun Srivatsa	Applied Materials
13:45	14:10	8B-2		Physical Model for Rapid Thermal Annealing (RTA) Induced Mechanical Stress	Tingyou Lin	Vanguard International Semiconductor Corporation
14:10	14:35	8B-3		Residual Stress Analysis and Structural Parameters Optimization of Corrugated Diaphragms Applied to MEMS Device	Chuying Tang	Wuhan University
14:35	15:00	8B-4		Emerging memory for IoT	Mohd Azizi Chik	UNIMAP & Silterra Malaysia Sdn Bhd

15:00-15:20 Authors' Interview / Coffee Break

13:20-15:00 Room C (Grand Ballroom I)
Session 8C Emerging Memory for IoT
Chairs: Sachin Sonkusale, Milan Pesic

13:20	13:45	8C-1	Invited	Ferroelectric-HfO2 Devices Technology and Manufacturing for Memory and Logic Applications	Shinji Migita	National Institute of Advanced Industrial Science and Technology (AIST)
13:45	14:10	8C-2		Fabrication and Characterization of Ferroelectric HfZrO-based Synaptic Transistors with Multi-state Plasticity	Tianqi Lu	Tsinghua University
14:10	14:35	8C-3		A Novel Capacitor-based Stateful Logic Operation Scheme for In-memory Computing in 1T1R RRAM Array	Wen Sheng Shen	Peking University
14:35	15:00	8C-4		A Novel Bi-Functional Memory-PUF Module Utilizing Adjustable Switching Window of RRAM	Bohan Lin	Tsinghua University

15:00-15:20 Authors' Interview / Coffee Break

13:20-15:00 Room D (Grand Ballroom III)
Session 8D Focus Session 3: Packaging and Heterogeneous Integration
Chairs: Piyush Gupta, Takafumi Fukushima

13:20	13:45	8D-1	Invited	Laser-Assisted Bonding (LAB), Its Bonding Materials, and Their Applications	Kwang-Seong Choi	Electronics and Telecommunications Research Institute
13:45	14:10	8D-2	Invited	System-level Power Integrity Optimization Based on High-Density Capacitors for Enabling HPC/AI Applications	Sungwook Moon	Samsung Electronics Co. Ltd.
14:10	14:35	8D-3	Invited	Multilithic 3D and Heterogeneous Integration Using Capillary Self-Assembly	Takafumi Fukushima	Tohoku University
14:35	15:00	8D-4	Invited	Surface Planarization of Polymeric Dielectrics for FOWLP Applications	Sungdong Kim	Seoul National University of Science and Technology

15:00-15:20 Authors' Interview / Coffee Break

15:20-19:20 Room A (Matahari I)
JSAP (JST / CREST)

15:20-17:00 Room B (Matahari III)
Session 9B RF Device Modeling
Chairs: Harshit Agarwal, Jean-Pierre Raskin

15:20	15:45	9B-1	Invited	SOI Devices and Substrates Towards RF and Millimeter Wave ICs	Jean-Pierre Raskin	Université Catholique de Louvain
15:45	16:10	9B-2		Modeling and Design of SiC-based High-Frequency Photoconductive Switches	Shaloo Rakheja	University of Illinois at Urbana-Champaign
16:10	16:35	9B-3		Geometrical Dimension Impact for Performance of CMOS Based Compatible Circular Shape Aluminum Nitride (AlN) Piezoelectric Micromachined Ultrasonic	Muhammad Naim Haron	Universiti Sains Malaysia
16:35	17:00	9B-4		Non-Quasi-Static Effect on Ge-Body pTFET for Different Source Materials	Sayani Ghosh	Jadavpur University

17:00-17:20 Authors' Interview / Coffee Break

15:20-17:20 Room D (Grand Ballroom III)
Heterogeneous HRI Road Map Group WS