EDTM2020 - Preliminary Advance Program

As of January 29, 2020

Poster Presentations

Session Chairs: P. Susthitha Menon and MK Radhakrishnan

P-1	Top-gate Self-aligned InGaZnO TFTs with Copper Light Shield Layer	Sun Sheng	Peking University
P-2	Charging Reduction Method for Auger Analysis on Bond Pad	Hemalatha Somu	Infineon Technologies Sdn. Bhd.
P-3	2D MoWSe2 Material Photoluminescence Characterization Based on MOS Device	Xinghua Wang	NIIDT
P-4	Stacked Ge Nanosheets GAAFETs Fabricated by 2D Ge/Si Multilayer Epitaxy, Wet Selective Etching, and New Method of Dislocation Removal	Guang Li Luo	Taiwan Semiconductor Research Institute
P-5	High Frequency Monolithic Inductor with Air-Gaps	Clarissa Prawoto	HKUST
P-6	Monolithic CMOS-BAW Oscillator for Mass Sensing Applications	Eloi Marigo	Silterra Malaysia Sdn. Bhd.
P-7	Novel Hybrid MTJ-CMOS Based Programmable Gain Amplifier for Portable Applications	Shivam Verma	IIT BHU, Varanasi
P-8	A 1.8 V 8-Bit Pipelined ADC with Integrated Folded Cascode Op-Amp in CMOS 180 nm	Norhamizah Idros	Universiti Sains Malaysia
P-9	Design of a High Accuracy and Real-Time Indoor Positioning System Based on Coding Point Identification and Its FPGA Implementation	Guanting Huo	Peking University Shenzhen
P-10	Low-Temperature Fully Photolithographic In-Si-O Thin-Film Transistors	Guangyu Yao	University of Cambridge
P-11	Process Optimization for Improving the Threshold Voltage Distribution of 3300V IGBT Platform	Kui Pu	MaxPower Semiconductor Inc.
P-12	A New Unity Gain Nine-Level Active Neutral Point Clamped (9L-ANPC) Multilevel Inverter Topology	Marif Daula Siddique	University of Malaya
P-13	New Approach for Estimating Three Parameters in PV Cell Models Based on Odd Polynomial Regression	Ahmed Abdolkhalig	The University of Tobruk
P-14	Proposed Process Flow for Potential Well Based FDSOI MOSFET at 20 nm Gate Length	Chandan Jaiswal	Indian Institute of Technology Kanpur
P-15	Analytical Study of WO3-based Memristive System for Neuromorphic Applications	Sanjay Kumar	IIT Indore
P-16	Analytical Modeling to Study the Effect of Cap Layer Thickness in ZnO/MgZnO/ZnO Heterostructure for HEMT Applications	Pawan Kumar	IIT Indore
P-17	Centroid and Inversion Charge Model for Long Channel Strained-Silicon GAA MOSFET with Quantum Effect	Nurul Ezaila Alias	Universiti Teknologi Malaysia
P-18	Carrier Density and Quantum Capacitance Model for Doped Graphene	L Chandrasekar	IIITDM Kancheepuram
P-19	Extensive Study on Effect of Pinhole Induced Electric Field in Si CS-TOPCon Solar Cell	Manish Verma	NIT
P-20	Assessment of Analog/RF Performances for 10 nm Tri-metal Gate FinFET	Nikhil G p	SRM Institute of Science and Technology
P-21	Corrections to WKB Approximation for Accurate Calculation of Gate Current in HKMG MOS Transistors	Apoorva Ojha	Maxim Integrated
P-22	The "Extrinsic" Compact Model of the MOSFET Drain Current Based on a New Interpolation Expression for the Transition Between Linear and Saturation	Valentin Turin	Orel State University
P-23	Resistive Approach for Extraction of Gate to Source bias-Dependent Source/Drain Parasitic Resistance, Mobility and Virtual Gate Length of GaN HEMT	Pragyey Kaushik	IIT Delhi
P-24	Beta-Ga2O3 MOSFET Device Optimization via TCAD	Minghao He	National University of Singapore, Singapore & Southern University of
P-25	Impact of Source/Drain Underlap on the Ballistic Performance of Silicon and Germanium-Tin Nanowire p-MOSFETs	Dibakar Yadav	Indian Institute of Technology, Madras
P-26	An Investigation of Transmission Line Modeling Test Structure in TCAD	Duy Nguyen	RMIT University
P-27	Device Electrostatics and High Temperature Operation of Oxygen Terminated Boron Doped Diamond MOS Capacitor and MOSFET	Pullaiah Yerragudi	IIT Hyderabad
P-28	Reduction of Harmonic Distortion of 14-Nm InAs Quantum Well n-MOSFET for High DC to AC Conversion Efficiency and High Voltage Gain	Sumedha Dasgupta	Future Institute of Technology
P-29	Variation of the Efficiency of GaN Junctionless FinFET Based Boost Converter with Subthreshold Swing as a Unified Device Parameter	Sudipta Mukherjee	Indian Institute of Technology, Bombay
P-30	Analysis and Compact Modeling of Thermal Noise in Halo Implanted MOSFETs	Ravi Goel	IIT Kanpur

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P-31	Investigation of Standard and Enclosed Gate n-MOSFET Degradation Due to Total Ionizing Dose Using BSIM-BULK	Jay Hind Verma	Indian Institute of Technology Kanpur
P-32	Geometrical Influence on Self Heating in Nanowire and Nanosheet FETs Using TCAD Simulations	Min Jae Kang	Imperial College London
P-33	Performance Comparison of Ge/Si Hetero-Junction Vertical Tunnel FET with and Without Gate-Drain Underlapped Structure with Application to Digital Inverter	Manas Tripathy	IIT (BHU), Varanasi
P-34	Ferroelectric Gate Heterojunction TFET on Selective Buried Oxide (SELBOX) Substrate for Distortionless and Low Power Applications	Ashish Singh	IIT (BHU), Varanasi
P-35	Determining ZnO Nanofilm Effect on Bimetallic SPR Biosensing Signal Using Taguchi Method	P. Susthitha Menon	Universiti Kebangsaan Malaysia & Institute of Microengineering and
P-36	Study of Thin Film Tin Oxide for Reliability as Gas Sensing Material	Ravi Shankar	STMicroelectronics Pte Ltd
P-37	Abnormal Positive Bias Stress Instability for Amorphous In-Ga-Zn-O Thin-Film Transistors with Room Temperature Atomic-Layer-Deposited Al2O3 Dielectric	Yan Shao	Fudan University
P-38	Improvement in Electrical Properties of Al/La2O3/ZrO2/ Gate Stack Deposited on LaON Passivated GaAs Substrate	Viral Barhate	K B C North Maharashtra University Jalgaon Maharashtra India
P-39	Adhesion Study on Different Surface Treatment by Button Shear Test	Wei Lee Lim	Infineon Technologies Kulim Sdn Bhd
P-40	Research on Failure Mechanism and Influence Factors of Single Event Burnout in SiC VDMOSFET	Qiumei Li	Guilin University of Electronic Technology
P-41	Studies on Correlation Between Diluted NH4OH Concentration of Pre-GOX Clean SC1 and GOX Breakdown Induced by Silicon Surface Oxides	Wan Tatt Wai	Infineon Technologies Kulim
P-42	A Cycle-by-Cycle HCD and BTI Compact Model to Calculate FinFET Based RO Ageing Using SPICE	Uma Sharma	IIT Bombay
P-43	ESD Device Layout Design Guidelines by 3D TCAD Simulation	Cheng Li	University of California, Riverside
P-44	Analysis of Extraction Methods for Threshold Voltage Shift in NBTI Degradation with Ultra-Fast Measurements	Yu-Hsing Cheng	ON Semiconductor
P-45	Modeling and Simulation of Low-Cost Composite Fiber-to-Chip Edge Coupler for Photonics and MEMS Packaging Applications	Ziji Wang	Southeast University
P-46	In-Hole Diodes for on-Chip Thermal Sensing	Cheng Li	University of California, Riverside
P-47	Enhanced WLCSP Reliability for RF Applications	Zhuojie Wu	Globalfoundries
P-48	Silver and Epoxy Binder-Based Printed Electrodes and the Effect of Silver	Hyun Jin Nam	Seoul National University of Science&Technology
P-49	Manufacturing WIP Management Systems with Automated Dispatching Decision: SilTerra Case Study	Mohd Azizi Chik	UNIMAP & Silterra Malaysia Sdn Bhd
P-50	Semiconductor Manufacturing Equipment: Challenges and Solutions to Enable Customer Yield Ramp	Roman Mostovoy	Applied Materials
P-51	Low Cost 2D-SnS2 Nanosheets Based UV-A-Visible Band Photodetector	Sanjeev Yadav	Indian Institute of Technology (BHU) Varanasi
P-52	Visible Light Response in Defect Engineered Wrinkle Network Nanostructured ZnO	Kamal Rudra	Indian Institute of Science
P-53	Electroluminescence of Si Based MOS Device with Ternary Rare Earth Doped Oxide	Takumi Tomita	Toyama Prefectural University
P-54	CVD-grown Graphene-on-Au Characterization and Sensing Using Kretschmann-based SPR	Nur Akmar Jamil	Universiti Kebangsaan Malaysia
P-55	Ultralow Power Neuromorphic Accelerator for Deep Learning Using Ni/HfO2/TiN Resistive Random Access Memory	Hoang-Hiep Le	National Cheng Kung University