edtm 2021
Electron Devices Technology and Manufacturing Conference

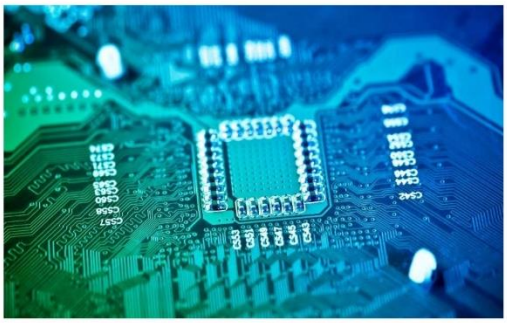
5th IEEE Electron Devices Technology and Manufacturing (EDTM) Conference 2021

EDTM 2021 PROGRAM

Chengdu, China

Chengdu Century City New International Convention and Exhibition Center

April 8–11, 2021



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https://ewh.ieee.org/conf/edtm/2021/

Welcome Message from Chairs

The General and TPC Chairs cordially welcome you to the **2021 IEEE Electron Devices Technology and Manufacturing (EDTM) Conference**, to be held in Chengdu, China, during April 8-11, 2021. Sponsored by IEEE *Electron Devices Society* (EDS), EDTM is a premier conference providing a unique forum for discussions on a broad range of device/manufacturing-related topics. EDTM rotates among the hot-hubs of semiconductor manufacturing in Asia. The 5th EDTM is coming to China in 2021 for the first time.

Come to EDTM2021 to learn from renowned researchers and engineers from around the globe through a rich list of technical sessions, interactive sessions, tutorials and short courses, and industrial exhibits. Share your knowledge and latest results with peers, and enjoy networking by meeting old friends and making new friends. Return invigorated with new ideas and enthusiasm to make new impacts.

EDTM2021 **highlights:**

Keynotes:

EDTM2021 features plenary keynotes from globally recognized scholars and researchers from both the academia and the industry, including Dr. Haijun Zhao, co-CEO of Semiconductor Manufacturing International Corporation (SMIC), talking about alternative foundry innovation strategies; Professor Xiang Zhang, President of University of Hong Kong, describing photonics enabling future hi-resolution cameras ; Teruo Hirayama, Executive Chief Engineer of Sony Corporation, reviewing technical innovations for image sensors; Professor Arokia Nathan from University of Cambridge, discussing about thin-film transistors for advanced analog signal processing; Prof. Ru Huang, Vice President of Peking University, offering a review on advances in ferroelectric-based devices; and Dr. Jeff Xu, Director of HiSilicon Research, looking into future semiconductor technology driven by ubiquitous computing.

Banquet Speech:

As the EDTM tradition, EDTM2021 will be have a Banquet during the Closing ceremony. The featured Plenary Speech will be given by Professor Ilesanmi Adesida. Being Provost of Nazabaryev University, Kazakhstan, and former Provost and Vice Chancellor of University of Illinois, Urbana-Champaign (UIUC), USA, Dr. Adesida will share his experiences in developing and administrating large research universities in developed and developing countries.

Tutorials and Short Courses:

There are two parallel tutorial tracks and four concurrent short course sessions on April 8 to kick-off EDTM2021. Total twelve lectures will be given by renowned experts include leading scholars, such as Professor Zhenan Bao of Stanford University, Professor Kang L. Wang of UCLA and Professor Philip Wong of Stanford University, to highlight a few.

Heterogeneous Integration Roadmap Workshop:

Heterogeneous integration (HI) is a promising avenue to future micro/nano-electronics at the system level and is expected to play an important role in the future scaling of electroncis. Come to this heterogeneous integration

roadmap (HIR) workshop to hear from the experts' opinions on the challenges and opportunities of the pursuit of next generation microelectronics technologies and system products.

Technical Sessions and Invited Talks:

The technical sessions include about 200 contributed papers accepted upon rigorous peer reviews, which will be presented in 36 technical oral sessions and one interactive session. In addition to the contributed papers, EDTM2021 also features an exciting list of about 90 invited talks by renowned scholars, researchers and engineers from around the world. For a better experience, the Interactive (poster) sessions will be integrated with the industrial exhibitions.

Beyond EDTM Technical Sessions:

As usual, EDTM2021 will hold the signature **Reception** in the evening of April 9. In addition, a special "**Business & Exhibition Night**" cocktail reception will be held in the evening of April 10. These two reception events offer relaxed settings for EDTM2021 attendees to network and meet friends and colleagues.

The **IEEE Chapters and Women-in-Engineering (CWiE) Summit**, will be held during EDTM2021, which will provide a forum for local IEEE volunteers and women students and professionals to meet together and share their experiences and ideas on education, research and career activities in area of microelectronics, and offer valuable mentorship opportunities.

To facilitate the desires of students and young engineers to develop successful professional careers in microelectronics, a **Young Engineers' Networking** event will be held on April 8, right after the Short Courses. This unique event will offer a relaxed forum for Young people to meet with famous "old" guys to chat on career planning and opportunities, and to get professional advices from the well-established experts.

What does Chengdu offer?

Chengdu is trendy, artistic, scenic and tech-savvy. It offers endless attractions and opportunities for visitors including cute grand pandas, hot Sichuan food, laid-back tea houses, brain-burning Mahjong games, snow-capped mountains and rapid waters, and ancient ruins and modern high rises, as well as classical temples.

On behalf of EDTM2021, we would like to extend to all of you a warm welcome to participate in the 2021 IEEE EDTM Conference. We look forward to seeing you in Chengdu or virtually during April 8-11, 2021!

Albert Wang

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EDTM 2021 Agenda

Day1 April 8th Tutorials &Short Courses					
Session Time	**Room A (ShuFeng Hall)**	**Room B (ShuShan Hall)**	**Room C (ShuYun Hall)**	**Room D (ShuJin Hall)**	**Activity**
09:00-12:30	Tutorial 1 TTUA1	Tutorial 2 TTUA2	HIR Workshop WTUA4		Registration 3rd floor Convention center
12:30-13:50	Lunch Break				
13:50-17:20	Short Course 1 STUP1	Short Course 2 STUP2	Short Course 3 STUP3	Short Course 4 STUP4	
17:30-19:30	**Young Engineers' Networking Event (ShuJin Hall)**				

Day2 April 9th					
Session Time	**Main Room (TianFu Ballroom）**				**Activity**
9:00-9:30	**Opening Ceremony (Award Presentations & IEEE Fellow Recognition)**				Registration 3rd floor Convention center
9:30-10:15	Plenary 1: Dr. Haijun Zhao, SMIC, China				
10:15-11:00	Plenary 2: Prof. Xiang Zhang, University of Hong Kong, China				
11:00-11:45	Plenary 3: Teruo Hirayama, Sony Corp., Japan				
	Room A (ShuFeng Hall)	**Room B (ShuShan Hall)**	**Room C (ShuYun Hall)**	**Room D (ShuJin Hall)**	
12:00-13:30	Lunch Break				
13:30-15:10	Session 1 WE1P1	Session 2 WE1P2	Session 3 WE1P3	Session 4 WE1P4	Poster & Exhibition Setting
15:10-15:30	Authors Interview/Coffee Break				
15:30-17:10	Session 5 WE2P1	Session 6 WE2P2	Session 7 WE2P3	Session 8 WE2P4	Exhibition
18:30-20:30	**Welcome Reception**, jointly with Poster I/Exhibition				Poster I (WTHPE) &Exhibition

EDTM 2021 Agenda

Day3 April 10th					
Session Time	**Main Room (TianFu Ballroom)**				**Activity**
9:00-9:45	Plenary 4: Prof. Arokia Nathan, University of Cambridge, UK				Registration 3rd floor Convention center
9:45-10:30	Plenary 5: Prof. Ru Huang, Peking University, China				
10:30-11:15	Plenary 6: Dr. Jeff Xu, HiSilicon Research, China				
11:15-11:30	Coffee Break				
	Room A (ShuFeng Hall)	**Room B (ShuShan Hall)**	**Room C (ShuYun Hall)**	**Room D (ShuJin Hall)**	
11:30-12:30	Session 9 TH1A1	Session 10 TH1A2	Session 11 TH1A3	Session 12 TH1A4	Exhibition Session
12:30-13:50	Lunch Break				
13:50-15:30	Session 13 TH2P1	Session 14 TH2P2	Session 15 TH2P3	Session 16 TH2P4	
15:30-15:50	Authors Interview/Coffee Break				
15:50-17:30	Session 17 TH3P1	Session 18 TH3P2	Session 19 TH3P3	Session 20 TH3P4	
18:30-20:30	**Business & Exhibition Night**, jointly with Poster II/Exhibition				Poster II (WTHPE)

Day4 April 11th					
Session Time	**Room A (ShuFeng Hall)**	**Room B (ShuShan Hall)**	**Room C (ShuYun Hall)**	**Room D (ShuJin Hall)**	**Activity**
9:00-10:40	Session 21 FR1A1	Session 22 FR1A2	Session 23 FR1A3	Session 24 FR1A4	Registration 3rd floor Convention center
10:40-11:00	Author Interview/Coffee Break				
11:00-12:40	Session 25 FR2A1	Session 26 FR2A2	Session 27 FR2A3	Session 28 FR2A4	
12:40-14:00	Lunch Break				
14:00-15:40	Session 29 FR3P1	Session 30 FR3P2	Session 31 FR3P3	Session 32 FR3P4	
15:40-16:00	Authors Interview/Coffee Break				
16:00-17:40	Session 33 FR4P1	Session 34 FR4P2	Session 35 FR4P3	Session 36 FR4P4	
18:30-21:00	**Closing Banquet (Award Presentations)** **Plenary Speaker:** Professor Ilesanmi Adesida Nazabaryev University, Kazakhstan & UIUC, USA				

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Best Paper Award Finalists

FR1A4-3: Synaptic Plasticity in Novel Non-Volatile FET with Amorphous Gate Insulator Enabled by Oxygen Vacancy Related Dipoles

Guoqing Zhang[1] , Yue Peng[1], Wenwu Xiao[1, 2], Fenning Liu[1] , Yan Liu[1] , Genquan Han[1], Yue Hao[1]; [1]Xidian University, China, [2]Xi'an UniIC Semiconductors, China

FR3P1-4: Formation Mechanism of a Rounded SiGe-Etch-Front in an Isotropic Dry SiGe Etch Process for Gate-All-Around (GAA)-FETs

Yu Zhao, Taku Iwase, Makoto Satake, Hirotaka Hamamura; Hitachi, Ltd., Japan

FR4P1-5: Forming Low-Resistivity Tungsten Contacts and Avoiding Fluorine Diffusion by Flash Lamp Annealing (FLA)

Shogo Shigemasu, Hideaki Tanimura, Hikaru Kawarazaki, Shinichi Kato; SCREEN Semiconductor Solutions Co. Ltd., Japan

FR2A1-3: White Noise Characterization of N-MOSFETs for Physics-Based Cryogenic Device Modeling

K. Ohmori, S. Amakawa; Device Lab Inc., Japan

FR1A2-3: GaN Super-Heterojunction Schottky Barrier Diode with over 10 kV Blocking Voltage

Sang-Woo Han , Jianan Song ,Rongming Chu; Pennsylvania State University, USA

FR2A3-2: Development of Integrated Device Simulator for Quantum Bit Design: Self-Consistent Calculation for Quantum Transport and Qubit Operation

Hidehiro Asai, Shota Iizuka, Tsutomu Ikegami, Junichi Hattori, Koichi Fukuda, Hiroshi Oka, Kimihiko Kato, Hiroyuki Ota, Takahiro Mori; National Institute of Advanced Industrial Science and Technology (AIST), Japan

TH3P3-4: On the Critical Role of Ferroelectric Thickness for Negative Capacitance Transistor Optimization

Om Prakash[1], Aniket Gupta[1,2], Girish Pahwa[3], Yogesh S. Chauhan[4], Hussam Amrouch[5]; [1]Karlsruhe Institute of Technology, Germany, [2]National Institute of Technology Uttarakhand, India, [3]University of California, Berkeley, USA, [4] Indian Institute of Technology Kanpur, India, [5] University of Stuttgart, Germany

FR2A4-3: ESD Co-Design of mm-Wave RF Switch in 22nm SOI

Feilong Zhang, Cheng Li, Mengfu Di, Zijin Pan, Han Wang, Albert Wang; University of California, Riverside, USA

TH2P4-3: Growth Behavior and Mechanism of Tin Whisker on Isolated SnAg Solder Under Compressive Stress

Shuhui Chen , Xundi Zhang , Lingyue Tan ,Anmin Hu , Huiqin Ling , Ming Li, Tao Hang; Shanghai Jiao Tong University, China

WE2P4-5: Cryogenic Operation of 3D Flash Memory for New Applications and Bit Cost Scaling with 6-Bit per Cell (HLC) and Beyond

Yuta Aiba, Hitomi Tanaka, Takashi Maeda, Keiichi Sawa, Fumie Kikushima, Masayuki Miura, Toshio Fujisawa, Mie Matsuo; Kioxia Corporation, Japan

TH2P1-4: A Flexible Electroencephalography Electronic Skin Based on Graphene

Ge Deng[1,2],Yan-cong Qiao[1] ,Ning-qin Deng[1] ,Xiao-shi Li[1] ,Qi Wu[1] ,Ying-fen Zeng[1,2], Si-fan Yang[2], Tian-Ling Ren[1]; [1]Tsinghua University, China [2]Graduate School at Shenzhen, Tsinghua University,China

WE2P1-5: A Novel Piston-Like Piezoelectric Micromachined Ultrasonic Transducer Based on Mass Loading Effect

Lei Wang， Jie Zhou, Wei Zhu, Zhipeng Wu, Wenjuan Liu, Chengliang Sun; Institute of Technological Sciences, China

TH2P2-4: A Sensitive Vertical Standing Graphene/Silicon Schottky Photodetector to Angle Changes

Ning-Qin Deng[1,4] , Zhen-Yi Ju[1], Ge Deng[1], Hou-Fang Liu[1], Xiang-Shun Geng[1] , Xiu-Feng Jia[1] , Jun Ren[1] , Tian-Zhong Yang[2] , Dan Xie[1] , Yi Yang[1] , He Tian[1], Tian-Ling Ren[1,3]; [1]Tsinghua University, China, [2]Chinese Academy of Sciences, China, [3]Center for Flexible Electronics Technology, Tsinghua University, Beijing, China, [4]National Institute of Metrology (NIM), Beijing, China

WE2P2-4: A Design of Horizontal Perovskite Nanowire LED for Better Light Extraction

Qianpeng Zhang[1,2], Yuanjing Lin[3], Xiaofei Sun[1] , Bryan Cao[1], Haoning Tang,[4], Zhiyong Fan[1,2]; [1] The Hong Kong University of Science and Technology, China, [2]HKUST-Shenzhen Research Institute, China, [3]Southern University

TH2P3-4: Universal Non-Volatile Resistive Switching Behavior in 2D Metal Dichalcogenides Featuring Unique Conductive-Point Random Access Memory Effect

Xiaohan Wu[1] , Ruijing Ge[1] , Yuqian Gu[1] , Emmanuel Okogbue[2] , Jianping Shi[3] , Abhay Shivayogimath[3] , Peter Bøggild[4] , Timothy J. Booth[4] , Yanfeng Zhang[3] , Yeonwoong Jung[2] , Jack C. Lee[1], Deji Akinwande[1] ; [1]University of Texas at Austin, Austin, USA, [2]University of Central Florida, USA, [3]Peking University, China, [4]Technical University of Denmark,Denmark

WE2P3-4: A Compact Model for Transition Metal Dichalcogenide Field Effect Transistors with Effects of Interface Traps

Yifei Xu1 , Weisheng Li1 , Dongxu Fan, Yi Shi, Hao Qiu , Xinran Wang; Nanjing University, China

TH1A3-1: A BEOL Compatible, 2-Terminals, Ferroelectric Analog Non-Volatile Memory

Laura Bégon-Lours; IBM Zurich Research Laboratory, Switzerland

Best Student Paper Award Finalists

FR1A4-4: Selecting and Optimizing Threshold Switching Materials and Devices for Stochastic Neuron

Kuan Wang, Qing Hu, Qi Lin, Dayou Zhang, Yuhui He, Hao Tong, Xiang Shui Miao; Huazhong University of Science and Technology, China

FR4P1-4: Optimization of Tilted Profile in Ultra-High Aspect Ratio Etch Process for 3D NAND Flash Memory

Jinqing He[1,2,3], Zhiliang Xia[1,2,3], Meng Wang[3] , Guangxuan Zhang[3] , Haiqing Dou[3] , Zongliang Huo[1,2,3]; [1] University of Chinese Academy of Sciences, China, [2]Institute of Microelectronics of the Chinese Academy of Sciences, China,[3]Yangtze Memory Technologies Company, Ltd.,China

FR3P1-5: Optimization of Bump Defect at High-Concentration In-Situ Phosphorus Doped Polysilicon/TEOS Oxide Interface for 3D NAND Flash Memory Application

Dongxue Zhao[1,2,3], Zhiliang Xia[1,2,3], Linchun Wu[3] , Tao Yang[1,2,3], Dongyu Fan[1,2,3], Yuancheng Yang[3] , Lei Liu[3] , Wenxi Zhou[3] , Zongliang Huo[1,2,3]; [1]Institute of Microelectronics of the Chinese Academy of Sciences, China, [2]University of Chinese Academy of Sciences, China, [3]Yangtze Memory Technologies Company, Ltd., China

TH3P1-3: Subthreshold Swing in Silicon Gate-All-Around Nanowire MOSFET at Cryogenic Temperature

Shohei Sekiguchi, Min-Ju Ahn , Takuya Saraya , Masaharu Kobayashi, Toshiro Hiramoto; University of Tokyo, Japan

FR1A1-3: Top-Gate Short Channel Amorphous Indium-Gallium-Zinc-Oxide Thin Film Transistors with Sub-1.2 nm Equivalent Oxide Thickness

Kaizhen Han, Subhranu Samanta, Chen Sun, Jishen Zhang, Zijie Zheng, Xiao Gong; National University of Singapore, Singapore

FR1A2-2: Channel Mobility Properties of β-Ga_2O_3 MOSFETs on Si Substrate Fabricated by Ion-Cutting Process

Yibo Wang,[1], Wenhui Xu,[2], Genquan Han,[1] Tiangui You,[2] Haodong Hu,[1] Yan Liu,[1] Hao Huang,[2] Xin Ou,[2] Xiaohua Ma,[1] Yue Hao[1]; [1]Xidian University, China, [2]Chinese Academy of Sciences, China

TH3P3-2: Revisiting the Definition of Ferroelectric Negative Capacitance Based on Gibbs Free Energy

Yuanyuan Zhang[1,2], Xueli Ma[1,2], Xiaolei Wang[1,2], Jinjuan Xiang[1,2], Wenwu Wang[1,2]; [1]Institute of Microelectronics, Chinese Academy of Sciences, China, [2]University of Chinese Academy of Sciences, China

TH3P3-5: Modelling and Design of FTJs as High Reading-Impedance Synaptic Devices

R. Fontanini, M. Massarotto, R. Specogna, F. Driussi, M. Loghi, D. Esseni ; University of Udine, Italy

WE1P2-2: Hot-Carrier-Induced Reliability Concerns for Lateral DMOS Transistors with Split-STI Structures

Li Lu[1], Ran Ye[1], Siyang Liu[1], Zhibo Yin[1], Yuanchang Sang[1], Weifeng Sun[1], Wei Su[2], Feng Lin[2], Shulang Ma[2], Yuwei Liu[2]; [1]Southeast University,China, [2]CSMC Technologies Corporation, China

WE1P2-4: Nonlinear Weight Quantification for Mitigating Read Disturb Effect on Multilevel RRAM-Based Neural Network

Lindong Wu, Zongwei Wang , Zhizhen Yu, Yabo Qin, Qingyu Chen, Yimao Cai , Ru Huang; Peking University, China

WE1P3-5: Low Temperature Packaging for Ion-Sensitive Organic Field Effect Transistor

Yixiao Tang, Wei Tang, Yukun Huang, Yawen Song, Bang Ouyang, Xiaojun Guo; Shanghai Jiao Tong University, China

TH3P4-3: Statistical Feature Extraction and Hybrid Feature Selection for Material Removal Rate Prediction in Chemical Mechanical Planarization Process

Wenlan Jiang[1], Chunpu Lv[1] , Bing Yang[2] , Fuquan Zhang[2] , Ying Gao[2] , Tao Zhang[1] , Huangang Wang[1]; [1]Tsinghua University, China, [2]Semiconductor Technology Innovation Center (Beijing) Crop, China

WE1P4-4: Three-Orders Improvement of Endurance in Hafina Based MFS Capacitor Through CF_4 Plasma Pre-Treatment

Shuxian Lv[1, 2], Yan Wang[1, 2], Zhaomeng Gao[1, 2], Zhiwei Dang[1, 2], Pengfei Jiang[1, 2], Peng Yuan[1,2], Qing Luo[1, 2], Shengjie Zhao[1] and Hangbing Lv[1, 2]; [1]Institute of Microelectronics of Chinese Academy of Sciences, China; [2]University of Chinese Academy of Sciences, China

WE2P1-4: Double-Deck Metal Solenoids 3D Integrated in Silicon Wafer for Kinetic Energy Harvester

Nianying Wang[1, 2, 3], Ruofeng Han[1, 3], Changnan Chen[1, 3], Jiebin Gu[1, 3], and Xinxin Li[1, 2, 3]; [1]Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, China, [2]ShanghaiTech University, China, [3]University of Chinese Academy of Sciences, China

TH2P2-2:β-Ga_2O_3 Micro-Flake FET SBPD with Record Detectivity of 3.87×10^{17} Jones for Weak Light Detection

Shunjie Yu[1] , Mengfan Ding[1] , Wenxiang Mu[2] , Zhitai Jia[2] , Xiaohu Hou[1] , Zhongfang Zhang[1] , Pengju Tan[1] , Xiaolong Zhao[1],Guangwei Xu[1] , Shibing Long[1]; [1]University of Science and Technology of China, China; [2]Shandong University, China

TH2P2-3: Large Area and Flexible Organic Active Matrix Image Sensor Array Fabricated by Solution Coating Processes at Low Temperature

Xiao Hou[1], Wei Tang[1], Sujie Chen[1], Jianghu Liang[2], Hanyang Xu[1], Bang Ouyang[1], Ming Li[1], Yawen Song[1], Chun-chao Chen[2], Patrick Too[3], Xiaoqing Wei[4], Libo Jin[4], Gang Qi[5], Xiaojun Guo1; [1]School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University, China, [2]School of Material Science and Engineering, Shanghai Jiao Tong University, China, [3]FlexEnable, UK, [4]iRay Technology, China, [5]Tianma Microelectronics, China

FR4P2-5: Semi-Disposable Self-Adhesive Sensor System for Wearable Electrocardiogram Detection

Fangran Bian, Sujie Chen, Ming Li, Yishen Pei, Xiaojun Guo; Shanghai Jiao Tong University, China

TH2P3-5:A Study of Materials Impacts on Graphene Electrostatic Discharge Switches

Cheng Li, Mengfu Di, Zijin Pan, Albert Wang; University of California, Riverside, USA

TH1A3-2:A Novel Leaky-FeFET Based True Random Number Generator with Ultralow Hardware Cost for Neuromorphic Application

Tianyi Liu[1] , Jin Luo[1] , Xinming Wei[1] ,Qianqian Huang[1,2] , Ru Huang[1,2] ; [1] Peking University, China, [2]National Key Laboratory of Science and Technology on Micro/Nano Fabrication, China

FR3P3-4: Artificial Neuron with Spike Frequency Adaptation Based on Mott Memristor

Qiumeng Wei[1] , Jianshi Tang[1,2] , Xinyi Li[1] , Yanan Zhong[1] , Bin Gao[1,2], He Qian[1,2], Huaqiang Wu[1,2]; [1] Institute of Microelectronics, Tsinghua University, China, [2]Beijing Innovation Center for Future Chips (ICFC), Tsinghua University, China

Best Interactive Paper Award Finalists

WTHPE-007: Seed layer dependent bottom pinned magnetic tunnel junctions

Weibin Chen[1,2], Shaohua Yan[2,3], Yaodi Yang[2] , Zhiqiang Cao[2,3], Yixuan Lin[1] Zitong Zhou[2,3], Shishen Yan[1], Qunwen leng[2,3,4]; [1]Shandong University, China,[2]Qingdao Research Institute, Beihang University, China, [3]School of Integrated Circuit Science and Engineering, Beihang University, China, [4]Goertek Inc, China

WTHPE-012: Development of HSQ replacement gate process for silicon nanowire MOS devices

Kun Tu[1,2], Xiaoqiao Dong[2], Baotong Zhang[2], Ru Huang[2], Ming Li[2], Peimin Lu[1]; [1]Fuzhou University, China, [2]Peking University, China

WTHPE-018: WS_2 pMISFETs by Sputtering and Sulfur-Vapor Annealing with TiN/HfO_2-Top-Gate-Stack, TiN Contact and Ultra-Thin Body and Box

Takuya Hamada, Masaya Hamada, Satoshi Igarashi, Taiga Horiguchi, Iriya Muneta, Kuniyuki Kakushima, Kazuo Tsutsui, Tetsuya Tatsumi, Shigetaka Tomiya; Hitoshi Wakabayashi Tokyo Institute of Technology, Japan

WTHPE-029: Vertical Field-Plated NiO/Ga_2O_3 Heterojunction Power Diodes

Hehe Gong[1], Xinxin Yu[1,2], Yang Xu[1], Jianjun Zhou[2], Fangfang Ren[1], Shulin Gu[1], Rong Zhang[1], Jiandong Ye[1]; [1]Nanjing University, China, [2]Nanjing Electronic Devices Institute, China

WTHPE-039: A first-principles study of the interface property in oxide-based RRAM

Nianduan Lu[1], Shang Ma[12], Jiezhi Chen[3], Qian Zhou[2], Ling Li[1], Ming Liu[1]; [1]Institute of Microelectronics of Chinese Academy of Sciences, China,[2] Beihang Univ., China, [3]Shandong Univ., China

WTHPE-040: Ag/HfO_2-based Threshold Switching Memristor as an Oscillatory Neuron

Qilin Hua[1], Chunsheng Jiang[2], Weiguo Hu[1]; [1]Chinese Academy of Sciences, China, [2]China Academy of Engineering Physics, China

WTHPE-051: HTRB & THB Reliability Improvement Using Capping Layer in Power Discrete Trench Devices

David Goh, W. J. Chen, F. Tahir, Shin Phay Lee, V. C. Ngwan; STMicroelectronics Pte Ltd, Singapore

WTHPE-055: Error Correction Scheme for Reliable RRAM-Based In-Memory Computing

Yixuan Hu, Kaili Cheng, Zuodong Zhang, Runsheng Wang, Yuan Wang, Ru Huang; Peking University, China

WTHPE-065: Crosstalk of octagonal TSV array arrangement based on differential signal

Jiang Han[1], Ziyu Liu[2], Ziyuan Zhu[1], Lin Chen[1], Qingqing Sun[1]; [1]Southwest University, China; [2]Fudan University, China

WTHPE-071: Core-Shell Dual-Gate Nanowire Synaptic Transistor with Short/Long-Term Plasticity

Md. Hasan Raza Ansari[1], Daehwan Kim[1], Seongjae Cho[1], Jong-Ho Lee[2], Byung-Gook Park[2]; [1]Gachon University, South Korea, [2]Seoul National University, South Korea

WTHPE-080: Visible Light Sensitivity Enhancement of CMOS Image Sensor with Pseudo High Refractive Index Film Integrated by Directed Self-Assembly Process

I. Oshiyama, T. Shigetoshi, I. Mita, N. Sumitani, T. Oinoue, S. Saito, T. Okawa, Y. Ebiko, K. Yokochi, Y. Kitano, Y. Hagimoto, T. Hirano, H. Iwamoto; Sony Semiconductor Solutions Corp., Japan

WTHPE-089: Fabrication and Research of MSM UV Detectors with Different Electrode Materials

Jun Liao, Cheng Wu, Rui Zhang, Yong Li, Tao Li; Shaoyang University, China

WTHPE-090: Design for a TE Mode Magneto-optical Circulator Based on Asymmetric Silicon Slot Waveguides

Yucong Yang[1], Shuyuan Liu[1], Wei Yan[1], Yan Zhang[2], Jun Qin[1], Longjiang Deng[1], Lei Bi[1]; [1]University of Electronic Science and Technology of China, China, [2]Chongqing United Microelectronics Center, China

WTHPE-099: Circuit Design and Experimental Verification of Low-voltage Organic Field-effect Transistor-based Common Source Amplifier

Li'ang Deng, Wei Tang, Lei Han, Yukun Huang, Xiaojun Guo; Shanghai Jiao Tong University, China

WTHPE-103: Nanoscale Inverters Enabled by a Facile Dry-Transfer Technique Capable of Fast Prototyping of Emerging Two-Dimensional Electronic Devices

Yachun Liang, Jiankai Zhu, Fei Xiao, Bo Xu, Ting Wen, Song Wu, Jing Li, Juan Xia, Zenghui Wang; University of Electronic Science and Technology of China, China

WTHPE-117: Optoelectronic Synaptic Devices Based on the Heterostructure of Silicon Nanomembrane and P3HT

Peiwen Huang[1], Lei Yin[1], Yayao Li[1], Yue Wang[1], Deren Yang[1,2], Xiaodong Pi[1,2]; [1]State Key Laboratory of Silicon Materials & School of Materials Science and Engineering, Zhejiang University, China,[2]Institute of Advanced Semiconductors, Hangzhou Innovation Center, Zhejiang University, China

WTHPE-102: Lateral p−n Homojunction formed by Local Doping for High-Performance Photodetector

Jiacheng Sun[1,2], Junying Zhang[2], Yuyan Wang[1,2]; [1]Tsinghua University, China,[2]Beihang University, China

Plenary Keynote 1

Haijun Zhao, Co-CEO, SMIC., PR China

"Creating Values through Innovations on Mature Nodes of Technologies of Integrated Circuits"

Abstract: IC manufacturing has followed Moore's Law in the past fifty years, with a new fab for each new node every one and half years to two years, resulting in a big challenge to IC IDM players. IC foundry manufacturing is a good solution to buffering the hard landing of the quick retirement of each fab after its peak period of two years. This talk explains the benefits of Moore's Law and industry's difficulty in following the fast moving and never ending of market needs, discusses the patterns of product evolution in various application sectors, and gives examples of making optimal uses of fabs from standard logic to embedded applications by continuous development of derivatives of the first set of technology per Moore's Law. It concludes that IC foundry manufacturing can plan and operate a fab by Moore's Law and More-Than Moore practices through innovations within a mature technology and make successful business by extending the fab lifetime to meet the needs of markets at different phases.

Biography

Dr. Haijun Zhao joined SMIC in 2010 as a Vice President for 12-inch operations and became COO and Executive Vice President in 2013. In July 2013, Dr. Zhao was appointed as General Manager of Semiconductor Manufacturing North China (Beijing) Corporation, a joint venture company established in Beijing and a SMIC subsidiary. In May 2017, Dr. Zhao was appointed as CEO, and later, in October, Co-CEO of SMIC. Dr. Zhao received his BS and Ph.D. degrees in electronic engineering from Tsinghua University, and MBA degree from the University of Chicago. Before joining SMIC, he had 16 years of overseas experience in well-known research institutes and manufacturing corporations in semiconductor field.

Plenary Keynote 2

Professor Xiang Zhang, President and Vice-Chancellor
The University of Hong Kong, Hong Kong SAR, PR China

"How to build a camera with highest resolution: a photonics perspective"

Abstract: Compared with electronics that is already at nanoscale today, photonic circuits remain rather bulky due to optical diffraction limit. This Keynote will discuss physics in scaling down of photonics that is important for both optical sciences and modern information technology. The talk will discuss a new optical cavity design using indefinite medium that exhibits an anomalous scaling law than conventional cavities, which was confirmed experimentally. The talk will further present nanoscale waveguide and laser circuits using hybrid plasmons that can be multiplexed into a single waveguide-an effort towards integrated photonics at nano-scale. The talk will also discuss non-Hermitian optics that is capable to sort color simultaneously at nano-scale for potential ultrahigh resolution camera.

Biography

Professor Xiang Zhang is currently the President and Vice-Chancellor of the University of Hong Kong (HKU). Prior to joining HKU in July 2018, he was the Ernest S. Kuh Endowed Chair Professor at the University of California, Berkeley, Director of the Nano-scale Science and Engineering Center (SINAM), and Director of the Materials Science Division at the Lawrence Berkeley National Laboratory. Professor Zhang received his PhD from UC Berkeley (1996), MS from the University of Minnesota and MS/BS from Nanjing University. He was an Assistant Professor at Pennsylvania State University (1996-1999), and Associate Professor and Full Professor at UCLA (1999-2004) prior to joining Berkeley's faculty in 2004. In 2008, Professor Zhang's research was selected by *Time Magazine* as one of the "Top Ten Scientific Discoveries of the Year" and "50 Best Inventions of the Year", *Discover Magazine*'s "Top 100 Science Stories" in 2007, and *R&D Magazine*'s top 25 Most Innovative Products of 2006. His research has been frequently featured in international media, including *BBC, CNN and the Wall Street Journal*. In 2019, his research team's work on 'Casimir effect' at UC Berkeley was selected as one of the Top 10 Breakthroughs for 2019 by *Physics World*.

Plenary Keynote 3

Teruo Hirayama, Executive Chief Engineer, Sony Corp., Japan

“The power of image sensors for innovation”

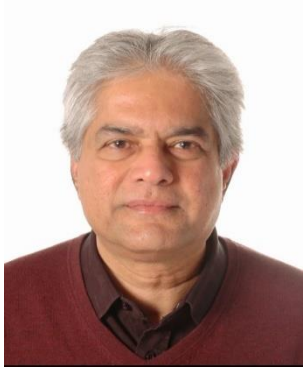
Abstract: CCD image sensor created a consumer video camera market in the early 80s. Then, digital still cameras that incorporated it replaced film cameras because they don’t need post-production process such as development, printing, and enlargement. Therefore, the film camera market shrank drastically. Around 2000, CMOS image sensor was incorporated into cellular phones due to digital output and low power consumption. However, CCD was yet used in video and still cameras because its image quality was superior to that of CMOS image sensor. Accordingly, back illuminated CMOS image sensor was developed. Its image quality exceeded that of CCD. So, it rapidly replaced CCD in video and still cameras. While back illuminated CMOS image sensor contributed to spread of smartphones that need cameras of high image quality. As smartphones spread, the markets of video and still cameras have been shrinking, but that of smartphones is growing. Thus, most of image sensors in these markets are back illuminated CMOS image sensor nowadays. On the other hand, image sensors are pioneering new markets for automobiles, medical care, agriculture, and so on by taking advantage of information of photons, such as wavelength, polarization, and time of flight, which human eyes cannot use. Furthermore, highly efficient image sensors are required for autonomic systems such as face recognition, automatic driving, and inspection in factories. This talk will present technological challenges of image sensors for replacing other devices and creating markets, then show the directions of advances of image sensors.

Biography

Teruo Hirayama joined Sony Corporation in 1981. He worked on SRAM and CMOS LSI in the research division of the semiconductor group, and then developed embedded memory technologies. He also developed stacked wide band DRAM on a LOGIC chip to solve issues of embedded DRAM in a LOGIC chip. Subsequently he joined the image sensor division in 2002 where he developed back-illuminated CMOS image sensor and stacked CMOS image sensor, which were launched into the market in 2009 and 2012, respectively. He played key role in development of CMOS image sensor technologies in Sony. He had managed the development of semiconductor devices as a senior general manager in the semiconductor technology development division since 2010. He was Senior Vice President in June 2013 and was appointed as president of the device and material R&D group in April 2014, where he was

responsible for R&D of displays, batteries, materials, and semiconductor devices. He is now Executive Chief Engineer in Sony Corporation.

Plenary Keynote 4



Prof. Arokia Nathan
University of Cambridge, UK

"Thin Film Transistor Architectures for Advanced Analog Signal Processing"

Abstract: Thin film semiconductor materials, such as oxides and organics, are becoming key for the future flexible electronics because of their potentially wide band gap, hence high transparency and low OFF current, compared with the ubiquitous silicon counterparts. These material systems can be processed at low temperature and at low fabrication cost, which makes them amenable for integration on a wide range of substrate materials including plastic and paper.

This presentation will review the new generation of applications using selected oxides and organics ranging from large area flexible electronics to the newly emerging Internet of Things. While the thin film transistor continues to evolve, producing devices with higher mobility, steeper sub-threshold slope and lower threshold voltage, practical analog signal processing circuits are constrained by issues related to non-uniformity, electrically- and illumination-induced instability, and temperature dependence. We will discuss the critical design considerations of displays, sensors and sensor interfaces, along with advanced signal processing architectures, to show how device-circuit interactions should be handled and how compensation methods can be implemented. In particular, the quest for low power becomes highly compelling in newly emerging application areas related to wearable devices in the Internet of Things. We will discuss thin-film transistor operation near the OFF state, driven by the pivotal requirement of low supply voltage and ultralow power. The operation of the wearable device is challenged by limited battery lifetime even if augmented with energy harvesting. One of the key requirements for design of flexible electronics for these emerging applications is physically-based circuit models, which requires good knowledge of the underlying transport mechanisms in the thin film transistor, and in particular, the associated density of states and field-effect mobility. The major developments in thin film transistor modeling for computer-aided design of circuits and systems will be reviewed, along with simple and compact analytical description of the current-voltage characteristics of thin film transistors in the above-threshold and sub-threshold regions for expedient circuit simulations.

Biography

Arokia Nathan (S'84–M'87–SM'99–F'10) is a leading pioneer in the development and application of thin film transistor technologies to flexible electronics, display and sensor

systems. Following his PhD in Electrical Engineering, University of Alberta, Canada in 1988, he joined LSI Logic USA and subsequently the Institute of Quantum Electronics, ETH Zürich, Switzerland, before joining the Electrical and Computer Engineering Department, University of Waterloo, Canada. In 2006, he joined the London Centre for Nanotechnology, University College London as the Sumitomo Chair of Nanotechnology. He moved to Cambridge University in 2011 as the Chair of Photonic Systems and Displays, and he is currently a Bye-Fellow and Tutor at Darwin College. He has over 600 publications including 4 books, and more that 110 patents and four spin-off companies. He is a Fellow of IEEE, an IEEE/EDS Distinguished Lecturer, a Chartered Engineer (UK), Fellow of the Institution of Engineering and Technology (UK), and winner of the 2020 IEEE EDS JJ Ebers Award.

Plenary Keynote 5

Prof. Ru Huang
Vice President, Peking University, China

"Ferroelectric-based device: revived as a low-power technology booster for diverse applications"

Abstract: Thanks to the discovery of hafnium-based ferroelectric oxides, the ferroelectric-based device has revived and attracted extensive attentions from both material and device communities recently, due to its fully CMOS compatibility and highly scalability. This talk will give a broad overview as well as insights on the various kinds of hafnium oxide based ferroelectric devices for diverse applications, including ultralow-power logics, memory, and neuromorphic computing. For low-power logic applications, ferroelectric negative-capacitance FET (NCFET) with steep-slope can break the fundamental limitation of subthreshold swing in conventional MOSFETs, while the negative-capacitance effect in ferroelectric film has aroused scientific controversy. This talk will discuss the current different understandings of negative-capacitance effect, and re-assess the possibility of NCFET as a steep-slope device for high-speed and low-voltage operation. Besides, the nonvolatile polarization feature in the ferroelectric can be used to store information in various ways as memory devices with lower write energy. This talk will present the technical challenges and state of the art of ferroelectric memories, and provide some prospects for their future development, focusing on ferroelectric random access memory (FeRAM), ferroelectric field-effect transistor (FeFET)and ferroelectric tunnel junction (FTJ). The reliability issues of hafnium-based ferroelectric FET and capacitance will also be discussed, especially the mechanisms of breakdown during endurance and/or retention. Moreover, by exploiting the inherent physics of ferroelectric polarization switching, this talk will present that the ferroelectric-based devices can be utilized for the hardware implementation of artificial neurons and synapses, providing an ultralow hardware-cost and high energy-efficient solution for neuromorphic computing systems.

Biography

Prof. Ru Huang is currently a professor and Vice-president, Peking University. She is an elected academician of Chinese Academy of Science, an elected member of IEEE Fellow and TWAS Fellow. Her research interests include nano-scaled CMOS devices, ultra-low-power new devices, new device for neuromorphic computing, emerging memory technology and device variability/reliability. She has authored or coauthored five books, 5 book chapters and more than 300 papers, including more than 100 papers in IEDM (39 IEDM papers from 2007 to 2020), VLSI Technology Symposium, IEEE EDL and IEEE T-ED, and gave more than 50 keynote/invited talks at international conferences. She is the holder of more than 200 granted patents (49 U.S.

patents). Prof. Huang is an Associate Editor-in-Chief of journal of “Science China: Information Sciences”. She is the winner of National Technology Invention Award, National Award of Science and Technology Progress and many other awards. Prof. Ru Huang has been the leader of many major national projects, as well as a couple of international collaborative projects.

Plenary Keynote 6

Dr. Jeff Xu
Director of HiSilicon Research

"Ubiquitous Computing Drives Future Semiconductor Technology"

Abstract : After 55 years unprecedented journey of Moore's Law, the semiconductor industry faces conventional transistor scaling physical limits and von Neumann architecture bottleneck. Though tremendous efforts have been directed towards improving logic scaling PPA (performance, power and area) including device architecture innovations, EUV introduction, and DTCO (Design Technology Co-Optimization), etc., performance/power gain diminishes and cost per transistor reverses conventional Moore's Law trend. On the other hand, performance of HPC (high performance computing) is limited by insufficient memory bandwidth, aka, memory wall. This paper reviews post Moore's Law era technology/function scaling options to meet demands of ever increasing chip performance from ubiquitous computing for the next two decades. The technology options include but not limited to the development of monolithic 3D memory to break the memory wall, integration of BEOL compatible low power logic for function scaling, introduction of in-memory devices to enable non-von Neumann architecture and gain system-level performance, and the adoption of 2D/CNT channel materials for logic and memory applications.

Biography

Dr. Jeff Xu is the Director of HiSilicon Research. He has 24 years of experiences in the field of semiconductor technology research and development. Jeff started his semiconductor career at Intel after completing his postdoctoral research at the University of Michigan. He joined TSMC corporate R&D in Hsinchu after 10 years tenure at Intel. Before joining HiSilicon, Jeff worked at Qualcomm in San Diego. Jeff holds nearly one hundred patents in the fields of semiconductor logic and memory devices and process technologies.

Plenary Speaker: Closing Banquet

Prof. Ilesanmi Adesida
Provost, Nazabaryev University, Kazakhstan

"The Development of an International Research University in the Big Steppe of Kazakhstan"

Abstract: Many of us present at this conference are associated with or work in world-class universities. The prevailing environment or ambience of excellence is taken for granted and the commanding ingredients responsible for such conditions are not completely obvious or transparent to the average faculty working to advance himself or herself professionally. Only a few universities under fifty years of existence have attained world-class status as measured through academic excellence, research excellence, and engagement with industry and society at large. In this talk, we will look at the individual and aggregate conditions needed to attain world class status. We will also discuss the establishment and growth of a ten-year old institution, Nazarbayev University in Kazakhstan, as a case study.

Biography

Prior to his present appointment at Nazarbayev University in Kazakhstan, Professor Adesida served as the Provost and Vice Chancellor for Academic Affairs at the University of Illinois at Urbana-Champaign (UIUC). He also served as the Dean of the College of Engineering and the Director of the Micro and Nanotechnology Laboratory at the same institution. As Nazarbayev University's Provost, Professor Adesida oversees NU's entire academic and research program, including creating innovative educational initiatives, awarding of research grants as well as overseeing the creation and implementation of quality assurance programs.

During his tenure at Illinois, he was instrumental in creating many innovative programs including the iFoundry for Engineering Education, the Applied Research Institute, the Advanced Digital Systems Center (in Singapore) and the novel engineering-based Carle-Illinois College of Medicine. His awards include the Oakley-Kunde Award for Excellence in Undergraduate Education, TMS John Bardeen Award for outstanding contributions to electronic materials and being named an outstanding graduate of the EECS Department at the University of California, Berkeley in 2009. He was awarded the Distinguished Service Award by IEEE Electron Device Society of which he served as President previously. He served as the Chair of the Engineering Advisory Board of the National Science Foundation, a member of the Hong Kong PhD Fellowship Program Committee, a member of International Expert Panel for the National Research Foundation of Singapore, and a member of the Advisory Committee of the Carnegie Foundation African Diaspora Fellowship Program. He is very much interested in issues of science, technology, engineering, and mathematics education, higher education, innovation and entrepreneurship, and their relevance to national development. He is very active in the Asian Universities Alliance; and he is a member of the United States' National Academy of Engineering (NAE).

Tutorial 1 (TTUA1)

“Flexible electronics + Display”

Thursday, April 8, 2021

09:00–12:30 ShuFeng Hall

Moderator: Tianling Ren, Jianbin Xu

TTUA1-1: 9:00 am

Skin-Inspired Organic Electronics

Zhenan Bao, Stanford University, California, USA

TTUA1-2: 10:10 am

2D material based flexible and wearable electronics

Jong-Hyun Ahn, Yonsei University, Seoul, Korea

TTUA1-3: 11:20 am

A Metal-Oxide Transistor Technology for Flexible Electronics

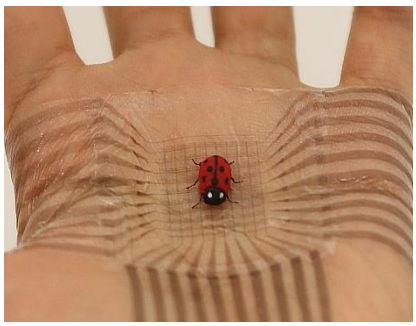
Man Wong, Hong Kong University of Science and Technology, Hong Kong, China

Tutorial TTUA1-1

Zhenan Bao, Director of Stanford Wearable Electronics Initiative (eWEAR), Stanford University, USA

"Skin-Inspired Organic Electronics"

Abstract: Skin is the body's largest organ, and is responsible for the transduction of a vast amount of information. This conformable, stretchable, self-healable and biodegradable material simultaneously collects signals from external stimuli that translate into information such as pressure, pain, and temperature. The development of electronic materials, inspired by the complexity of this organ is a tremendous, unrealized materials challenge. However, the advent of organic-based electronic materials may offer a potential solution to this longstanding problem. Over the past decade, we have developed materials design concepts to add skin-like functions to organic electronic materials without compromising their electronic properties. These new materials and new devices enabled arrange of new applications in medical devices, robotics and wearable electronics. In this talk, I will discuss several projects related to engineering conductive materials and developing fabrication methods to allow electronics with effective electrical interfaces with biological systems, through tuning their electrical as well as mechanical properties. The end result is a soft electrical interface that has both low interfacial impedance as well as match mechanical properties with biological tissue. Several new concepts, such as "morphing electronics" and "genetically targeted chemical assembly - GTCA" will be presented.



Images of stretchable electronic skin. Image credit: Amir Foudeh, Sihong Liu of Bao Group, Stanford University

Biography

Zhenan Bao is Department Chair and K.K. Lee Professor of Chemical Engineering, and by courtesy, a Professor of Chemistry and a Professor of Material Science and Engineering at

Stanford University. Bao founded the Stanford Wearable Electronics Initiate (eWEAR) in 2016 and serves as the faculty director.

Prior to joining Stanford in 2004, she was a Distinguished Member of Technical Staff in Bell Labs, Lucent Technologies from 1995-2004. She received her Ph.D in Chemistry from the University of Chicago in 1995. She has over 550 refereed publications and over 65 US patents with a Google Scholar H-Index >160.

Bao is a member of the National Academy of Engineering and the National Academy of Inventors. She is a Fellow of MRS, ACS, AAAS, SPIE, ACS PMSE and ACS POLY.

Bao was selected as Nature's Ten people who mattered in 2015 as a "Master of Materials" for her work on artificial electronic skin. She was awarded the inaugural ACS Central Science Disruptor and Innovator Prize in 2020, the Gibbs Medal by the Chicago session of ACS in 2020, the Wilhelm Exner Medal by Austrian Federal Minister of Science 2018, ACS Award on Applied Polymer Science 2017, the L'Oréal-UNESCO For Women in Science Award in the Physical Sciences 2017, the AICHE Andreas Acrivos Award for Professional Progress in Chemical Engineering in 2014, ACS Carl Marvel Creative Polymer Chemistry Award in 2013, ACS Cope Scholar Award in 2011, the Royal Society of Chemistry Beilby Medal and Prize in 2009, the IUPAC Creativity in Applied Polymer Science Prize in 2008.

Bao is a co-founder and on the Board of Directors for C3 Nano and PyrAmes, both are silicon-valley venture funded start-ups. She serves as an advising Partner for Fusion Venture Capital.

Tutorial TTUA1-2

Jong-Hyun Ahn, School of Electrical and Electronic Engineering, Yonsei University, Korea

"2D material based flexible and wearable electronics"

Abstract : Rapid advances in synthesis of graphene and 2D materials, and fabrication methods for functional devices enable sophisticated types of functionality and their application to various emerging electronics, such as flexible, wearable and optoelectronic applications,that cannot be addressed with conventional materials. In this talk, I present that two-dimensional semiconductor/semi-metal materials can play critical roles in this context, through demonstrations of complex, mechanically assembled electronic and optoelectronic devices for flexible and wearable applications. Specifically, the mechanics of graphene and MoS_2 can yield various devices in distinct, engineered wearable geometries that cannot be easily reproduced with conventional materials and/or conventional device layouts. Examples of devices include touch, tactile sensors, wearable OLED display, and brain signal sensing devices.

Biography

Jong-Hyun Ahn received Ph.D degree at POSTECH, Korea in 2001. He joined SKKU as an assistant professor in 2008 after the postdoctoral experience in the University of Illinois at Urbana-Champaign for several years and moved to Yonsei University in 2013. He holds Underwood distinguished professor at Yonsei University, Korea. He has worked as a president of Korean Graphene Society and a director of the Center for strain engineered electronic devices, supported by National Research Foundation of Korea. He also works as an associate editor of NPG Asia Materials. His research includes fundamental and applied aspects of nanomaterials and fabrication for flexible and wearable electronic devices, and recent interest focuses on 2D material based wearable electronics with an emphasis on bio-applications. Jong-Hyun Ahn has authored more than 200 papers (H-index 73, Citation # > 40,000), and is an inventor of more than 60 patents and has received numerous scientific awards, including the Korean National academy award (2018), the National Young Scientist Award (2011) and the IEEE George Smith Award (2009).

Tutorial TTUA1-3

Man Wong, Hong Kong University of Science and Technology, Hong Kong, China

"A Metal-Oxide Transistor Technology for Flexible Electronics"

Abstract: The realization of electronic systems on a flexible substrate is a recognized fertile ground of research and development, with established applications in displays and extending to future ones in biomedical sensing, etc. Depending on the requirements, further constraints are imposed on the substrate, such as transparency, stretchability, bio-compatibility, and bio-degradability. As active electronic elements, transistors are indispensable in the realization of a non-trivial flexible electronic system. Much has been accomplished and more needs to be done in resolving issues regarding the compatibility of a transistor technology with polymer-based flexible substrates. Following a broad overview of possible transistor technologies for the construction of flexible electronics, focus will be placed on a thin-film transistor technology based on metal-oxide semiconductors as one that fits the purpose. This assessment will be justified on grounds of high optical transparency of wide band-gap semiconductors, good electrical performance of the transistors, substrate-compatible low-temperature processing, and good stability against mechanical deformation. Techniques of realizing metal-oxide thin-film transistors on a polyimide-based flexible substrate will be discussed, in terms of material engineering, device architectural design, and process optimization. Issues and challenges in the design of flexible circuits will be covered and examples of flexible electronic systems currently under development will be introduced.

Biography

Man Wong was born in Beijing, China. From 1979 to 1984, he studied at the Massachusetts Institute of Technology, USA, where he obtained his BS and MS degrees in Electrical Engineering. From 1985 to 1988, he was at the Center for Integrated Systems at Stanford University, USA, where he worked on tungsten-gate MOS technology and obtained his PhD degree, also in Electrical Engineering. From 1988 to 1992, he was with the Semiconductor Process and Design Center of Texas Instruments, USA and worked on the modeling and development of integrated-circuit metallization systems and dry/vapor surface-conditioning processes. He is with the Department of Electronic and Computer Engineering at The Hong Kong University of Science and Technology, Hong Kong. His research interests include micro-fabrication technology, device structure and material; physics and technology of thin-film transistor; organic light-emitting diode display technology; modeling and implementation of integrated micro-systems; and thin-film solar cell device and process technology. He is a member of Tau Beta Pi, Eta Kappa Nu and Sigma Xi.

Tutorial 2 (TTUA2)

"Future Communication and Computing"

Thursday, April 8, 2021

09:00–12:30 ShuShan Hall

Moderator: Qiming Shao, Yimao Cai

TTUA2-1: 9:00 am

6G: Towards a More Connected and Sustainable World

Mohamed-Slim Alouini, King Abdullah University of Science and Technology, Saudi Arabia

TTUA2-2: 10:10 am

Topological Spintronics for Low Energy Dissipation

Kang L. Wang, University of California, Los Angeles, USA

TTUA2-3: 11:20 am

In- and Near-Memory Computing Using 2D/3D Resistive Memories

Philip Wong, Stanford University, California, USA

Tutorial TTUA2-1

Mohamed-Slim Alouini, King Abdullah University of Science and Technology, Saudi Arabia

"6G: Towards a More Connected and Sustainable World"

Abstract: The role of Internet and Communication Technology (ICT) in bringing about a revolution in almost all aspects of human life needs no introduction. It is indeed a well-known fact that the transmission of the information at a rapid pace has transformed all spheres of human life such as economy, education, and health to name a few. In this context, and as the standardization of the fifth generation (5G) of wireless communication systems (WCSs) has been completed, and 5G networks are in their early stage of deployment, the research visioning and planning of the sixth generation (6G) of WCSs are being initiated. 6G is expected to be the next focus in wireless communication and networking and aim to provide new superior communication services to meet the future hyper-connectivity demands in the 2030s. In addition, keeping in mind that urbanized populations have been the major beneficiary of the advances offered by the previous generations of WCSs and motivated by the recently adopted unitednations sustainability development goals intended to be achieved by the year 2030, 6G networks are anticipated to democratize the benefits of ICT. Indeed these advantages are still not experienced by almost 4 billion people in the world who are still "unconnected or under-connected" and who suffer as such from the "digital divide", a term coined in order to emphasize the lack of ICT infrastructure in many parts of the world. Given this background, this talk aims to (i) provide an envisioned picture of 6G, (ii) serve as a research guideline in the beyond 5G era, and (iii) go over the recently proposed solutions to provide high-speed connectivity in under-covered areas in order to serve and contribute to the development of far-flung regions.

The role of Internet and Communication Technology (ICT) in bringing about a revolution in almost all aspects of human life needs no introduction. It is indeed a well-known fact that the transmission of the information at a rapid pace has transformed all spheres of human life suchas economy, education, and health to name a few. In this context, and as the standardization of the fifth generation (5G) of wireless communication systems (WCSs) has been completed, and 5G networks are in their early stage of deployment, the research visioning and planning of the sixth generation (6G) of WCSs are being initiated. 6G is expected to be the next focus in wireless communication and networking and aim to provide new superior communication services to meet the future hyper-connectivity demands in the 2030s. In addition, keeping in mind that urbanized populations have been the major beneficiary of the advances offered by the previous generations of

WCSs and motivated by the recently adopted united nation sustainability development goals intended to be achieved by the year 2030, 6G networks are anticipated to democratize the benefits of ICT and to bring global connectivity in a sustainable fashion in order to contribute to developing tomorrow's digitally inclusive and green world. In this context, this talk aims to (i) provide an envisioned picture of 6G, (ii) serve as a research guideline in the beyond 5G era, and (iii) go over some of the recently proposed green technologies to offer high-speed connectivity not only in urban environments but also in under-covered areas in order to serve and contribute to the development of far-flung regions.

Biography

Mohamed-Slim Alouini was born in Tunis, Tunisia. He received the Ph.D. degree in Electrical Engineering from the California Institute of Technology (Caltech), Pasadena, CA, USA, in 1998. He served as a faculty member in the University of Minnesota, Minneapolis, MN, USA, then in the Texas A&M University at Qatar, Education City, Doha, Qatar before joining King Abdullah University of Science and Technology (KAUST), Thuwal, Makkah Province, Saudi Arabia as a Professor of Electrical Engineering in 2009.

Tutorial TTUA2-2

Kang L. Wang, University of California, Los Angeles, USA

"Topological Spintronics for Low Energy Dissipation"

Abstract : Spintronics provides an energy-efficient high-speed nonvolatile approach for next-generation memory and logic applications to complement CMOS technology, for example, magnetoresistance random-access memory (MRAM) [1, 2]. First, we will briefly show the recent progress on spintronic devices based on spin-transfer torque, spin-orbit torque and voltage-controlled magnetic anisotropy for energy efficient applications. Firstly, we describe the use of spin-momentum locking in topological surface states to realize a high spin-orbit torque (SOT) efficiency [3], showing the SOT of an order of magnitude larger than conventional heavy metals at room temperature [4]. By tuning the Fermi level of topological insulators (TIs), it was found that the topological surface states give rise to an observed giant SOT value beyond that from bulk. Then, the magnetic tunnel junction device was integrated with the TIs, where the 100% tunneling magnetoresistance (TMR) ratio and the ultralow switching current density of 10^5 Acm^{-2} were achieved at the same time, indicating the great potential of TI-based SOT-MRAM.

Second, to further reduce the energy and improve the speed of SOT devices, we use the ferrimagnetic GdFeCo [5], where the SOT effective field is proportional to $1/M_s$ and thus is significantly enhanced near the magnetic compensation point ($M_s = 0$) [6]. To demonstrate the speed performance, a photoconductive Auston switch in a ferrimagnetic GdFeCo device was used and a train of 1-ps electric pulses were generated by a THz optical source. Efficient switching of the magnetization states between the up and down states, from which an over 50 GHz magnetic resonance frequency indicates tens of picosecond switching speed. Furthermore, by carefully tuning the magnetic anisotropy and interfacial Dzyaloshinskii–Moriya interaction (DMI) in BiSbTe/GdFeCo, a topologically-protected magnetic skyrmion phase was observed, where the antiferromagnetically-coupled skyrmion lattices were detected by the element-resolved scanning transmission X-ray microscope (STXM) for Gd and Fe elements [7].

For SOT devices with perpendicular magnetic anisotropy, breaking the inversion symmetry is needed to achieve deterministic SOT switching. Often, an external in-plane field is used for this purpose. We will discuss the use of different kinds of symmetry breaking methods to achieve deterministic switching. We report the use of magnetization gradient in ferrimagnetic GdFeCo layers to create SOT-induced spin textures, where the chiral symmetry is broken by DMI, leading to the deterministic SOT switching [8].

Lastly, voltage-controlled magnetic anisotropy (VCMA) can further reduce the energy of spintronic devices from 100 fJ/bit to below 1 fJ/bit [9]. The integration of SOT with VCMA may further improve the performance. However, two major challenges need to be resolved for realizing high density integration in order to achieve high marketing-level applications: a high TMR (on off ratio) >1000% ratio is needed; and a large VCMA coefficient of >1000 (fJ V^{-1} m^{-1}) will greatly improve the scaling of device density. Recent work in 2-dimentional (2D) magnetic materials has demonstrated a TMR of over 10000% at 4 K [10], where increasing the working temperature to room temperature will be a significant step for practical applications. Likewise, the integrating SOT with VCMA will give further improvement of performance.

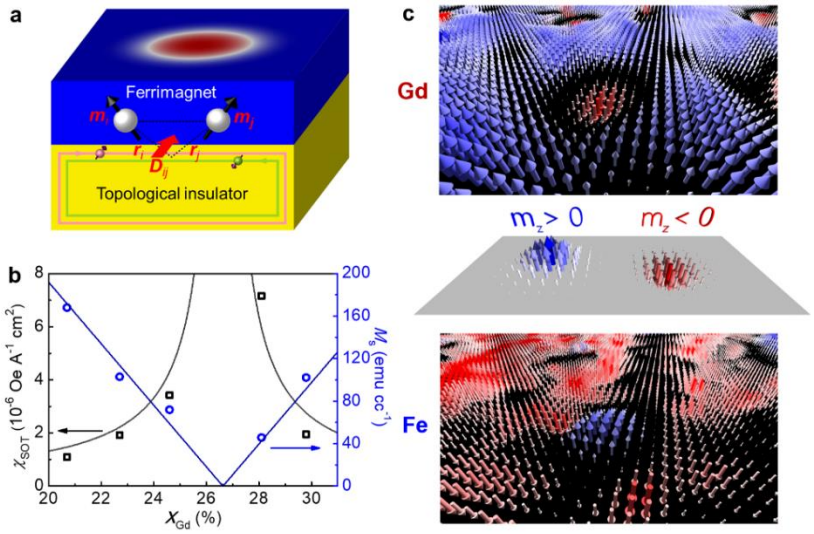


Figure 1. a, Schematic of a topological insulator/ferrimagnet heterostructure, i.e., $(BiSb)_2Te_3/Gd_x(FeCo)_{1-x}$. b, SOT effective field χ_{SOT} and saturation magnetization M_s as a function of the Gd concentration. c, Antiferromagnetically-coupled skyrmion lattices for Gd and Fe elements measured by scanning transmission X-ray microscopy (STXM).

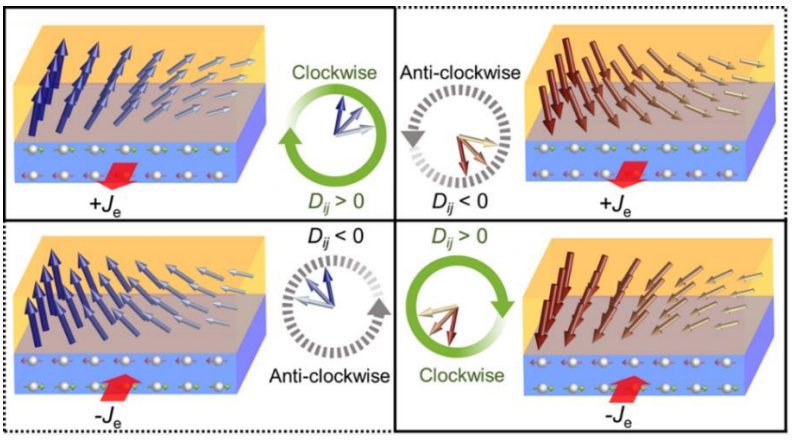


Figure 2. Schematic of chiral symmetry breaking showing that different chirality direction (clockwise or anticlockwise) gives rise to deterministic spin-orbit torque (SOT) switching. For the system with a magnetization gradient, SOT exerts the non-collinear spin textures, where the DMI breaks the chiral symmetry and thus leads to the deterministic SOT switching.

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[3] L. Liu, C.-F. Pai, Y. Li, H. W. Tseng, D. C. Ralph and R. A. Buhrman, Science 336 (6081), 555-558 (2012).
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Biography

Dr. Kang L. Wang is currently a Distinguished Professor and the Raytheon Chair Professor in Physical Science and Electronics at the University of California, Los Angeles (UCLA). He is affiliated with the Departments of ECE, MSE, and Physics/Astronomy. He received his M.S. and Ph.D. degrees from the Massachusetts Institute of Technology and his B.S. degree from National Cheng Kung University (Taiwan). He is a Guggenheim Fellow, Fellows of American Physical Society and IEEE, and a Laureate of Industrial Technology Research Institute of Taiwan. He is an Academician of Academia Sinica. His awards include the IUPAP Magnetism Award and Néel Medal, the IEEE J.J. Ebers Award for electron devices, SRC Technical Excellence Award, the Pan Wen-Yuan Award, Chinese American History Makers Award, and others. He served as the editor-in-chief of IEEE TNANO, editor of Artech House, editors for J of Spins and Science Advances, and other publications. His research areas include topological insulators – condensed matters and physics; spintronics/magnetics and nonvolatile electronics; quantum information and computing; nanoscale physics and materials; molecular beam epitaxy.

Tutorial TTUA2-3

H.-S. Philip Wong, Professor of Electrical Engineering, Stanford University, USA

"In- and Near-Memory Computing Using 2D/3D Resistive Memories"

Abstract: The growing demands of ubiquitous artificial intelligence (AI) applications call for new energy-efficient hardware solutions that can offer sustainable benefits with technology, architecture, and system advancements. As illustrated in Figure 1, we envision that 3D integrated systems with tight integration of logic and memory, through end-to-end technology-system co-optimization, will be the key enabler going forward [1]. Particularly, high-density, on-chip non-volatile memories (NVMs) play an important role [2], enabling three major features: (1) high-capacity, high-bandwidth on-chip data storage, (2) near-memory computing capabilities with domain-specific accelerators on chip, (3) in-memory computing capabilities utilizing unique device properties. In this tutorial, we will discuss on the essential characteristics of in-memory and near-memory computing using 2D and 3D vertical resistive RAM (RRAM).

We start with a high-level overview and discussion of both application and technology trends towards energy-efficient AI hardware. Then, at device level, we will focus on the RRAM technologies and provide backgrounds from device physics and operations to 3D structures and integration. At circuit and architecture level, we will dive into the basic ideas, designs, and system analysis of leveraging RRAM for near-memory and in-memory computing, using various case studies.

The new design space created by the logic-memory integration with RRAMs and other NVMs on chip can provide new insights and augment domain-specific accelerator optimizations where computations need to be close to memories [3]. Utilizing the device-level and circuit-level properties allows us to move neural network computations into RRAMs [4], and further support brain-inspired learning models with native compute kernels in 3D structures [5].

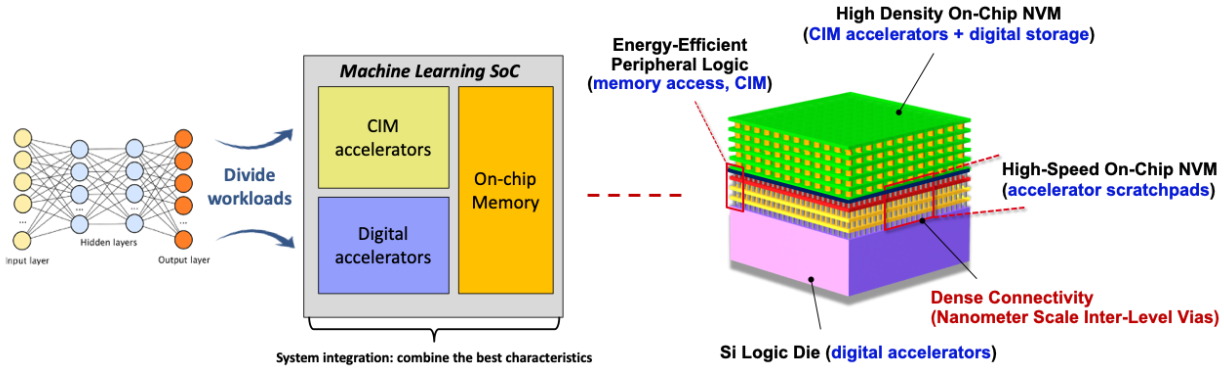

Figure 1. End-to-end technology-system co-optimization with on-chip NVM (e.g., RRAM) for energy-efficient machine intelligence.

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[1] M.M. Aly, et al., "The N3XT approach to energy-efficient abundant-data computing," Proc. IEEE, 2018
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[4] W. Wan et al., "A 74 TMACS/W CMOS-RRAM neurosynaptic core with dynamically reconfigurable dataflow and in-situ transposable weights for probabilistic graphical models," ISSCC, 2020
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H.-S. Philip Wong

Biography

H.-S. Philip Wong is the Willard R. and Inez Kerr Bell Professor in the School of Engineering at Stanford University. He joined Stanford University as Professor of Electrical Engineering in September, 2004. From 1988 to 2004, he was with the IBM T.J. Watson Research Center. From 2018 to 2020, he was on leave from Stanford and was the Vice President of Corporate Research at TSMC, the largest semiconductor foundry in the world. Since 2020, he has been the Chief Scientist of TSMC. He is a Fellow of the IEEE and received the IEEE Electron Devices Society J.J. Ebers Award for "pioneering contributions to the scaling of silicon devices and technology." He has held leadership positions at major multi-university research centers of the National Science Foundation and the Semiconductor Research Corporation. He is the founding Faculty Co-Director of the Stanford SystemX Alliance – an industrial affiliate program focused on building systems, and the faculty director of the Stanford Non-Volatile Memory Technology Research Initiative (NMTRI).

Heterogeneous Integration Roadmap (HIR) Workshop

(WTUA4)

9:00 am – 12:30 pm

Thursday, April 8, 2021

On-site participation: ShuYun Hall

The Heterogeneous Integration Roadmap (HIR) is a roadmap to the future of electronics identifying technology requirements and potential solutions. The primary objective is to stimulate pre-competitive collaboration between industry, academia and government to accelerate progress. The roadmap offers professionals, industry, academia and research institutes a comprehensive, strategic forecast of technology over the next 15 years. The HIR also delivers a 25-year projection for heterogeneous integration of Emerging Research Devices and Emerging Research Materials with longer research-and-development timelines. The HIR is sponsored by three IEEE Societies (Electronics Packaging Society, Electron Devices Societry & Photonics Society) together with SEMI and ASME EPPD.

This HIR workshop @EDTM2021 will feature seven selected topics from the HIR chapters including an overview presentation. The purposes for the HIR workshop at EDTM are to feature interest & stimulate collaboration for the HIR stakeholders around the world.

HIR Workshop Organizing Committee

Chair: William Chen, Co-Chairs: Subramanian Iyer, WR Bottoms, Ravi Mahajan

Agenda

09:00 am – 09:05 am	Welcome EDTM & HIR
09:05 am – 09:30 am	HIR Overview: William Chen, WR Bottoms & Ravi Mahajun
09:30am – 09:55 am	Automotive Electronics: Urmi Ray & Rich Rice
09:55 am – 10:20 am	SiP & Module: R. Aschenbrenner, Klaus Pressel, Erik Jung
10:20 am – 10:45 am	MEMS & Sensor Integration: Shafi Saiyed & MaryAnn Mahar
10:45 am – 11:10 am	Simulation & Co-Design: Christopher Bailey & Xuejun Fan
11:10 am – 11:35 am	Reliability: Abhijit Dasgupta, Richard Rao, Shubhana Sahasrabudha
11:35 am – 12:00 pm	Integrated Power Electronics: Patrick McCluskey & Douglas Hopkins
12 :00 pm – 12:30 pm	Panel Session: Moderators: Subramanian Iyer & William Chen

Workshop Speakers & Panelists from HIR Techncial Working Groups:

HIR Overview Chapter: William (Bill) Chen (ASE) & WR (Bill) Bottoms (HIR & 3MTS, Chairman)


Automotive Technical Working Group: Chair & Co-Chair Urmi Ray (Consultant) & Rich Rice (ASE SVP Business Development)


SiP & Module Technical Working Group: Chair & Co-Chairs Rolf Aschenbrenneer (IZM), Klaus Pressel (Infineon), Erik Jung (IZM)



MEMS & Sensor Integration Technical Working Group: Chair & Co-Chair Shafi Saiyed (Analog Devices) & MaryAnn Maher (CEO, Soft MEMS)


Simulation Technical Working Group: Chair & Co-Chair Christopher Bailey (Greenwich University), Xuejun Fan (Lamar Uniuversity)


Reliability Technical Working Group: Chair & Co-Chairs Abhijit Dasgupta (U Maryland), Richard Rao (Inphi), Shubhana Sahasrabudha (Intel)



Integrated Power Electronics Technical Working Group: Chair & Co-Chair Patrick McCluskey (U Maryland) Douglas Hopkins (NC State)


Panel Session Moderators:

Subramanian Iyer (UCLA) & William Chen (HIR & ASE)


Short Course 1 (STUP1)

"Advanced Memories and Emerging Applications"

Thursday, April 8, 2021

13:50–17:20 ShuFeng Hall

Moderator: Qi Xiang, Navakanta Bhat

STUP1-1: 2:00 pm

Computing-in-memory design for general neural networks inference

Shaodi Wang, Founder/CEO of WITINMEM, Beijing, China

STUP1-2: 3:10 pm

Emerging Device Technologies for Neuromorphic Computing and Machine Learning

Damien Querlioz, Université Paris-Saclay, CNRS, France

STUP1-3: 4:20 pm

RRAM Based Computing-In-Memory

Qi Xiang, CTO of Xiamen Industrial Technology Research Institute Co., LTD, China

Short Course STUP1-1

Shaodi Wang, Beijing Zhicun (WITIN) Technology Co. Ltd, China

"Computing-in-memory design for general neural networks inference"

Abstract : Neural Networks (NNs) have been widely employed in modern artificial intelligence (AI) systems due to their unprecedented capability in classification, recognition and detection. However, the massive data communication between the processing units and the memory has been proven to be the main bottleneck to improve the efficiency of NNs based hardware. Furthermore, the significant power demand for massive addition and multiplication limits its adoption at the edge devices. In addition, the cost is another major concern for an edge device. Therefore, an edge neural processing chip with simultaneous low power, high performance, low cost is in urgent need for the fast-growing AI-and-IoT (AIoT) market. In this talk, we will introduce an ultra-low-power neural processing SoC chip in 40nm with computing-in-memory technology. We have designed, fabricated, and tested this chip based on 40nm eFlash technology. It solves the data processing and communication bottlenecks in NNs with computing-in-memory technology. Furthermore. It combines classic digital solution together with the analog computing-in-memory macro to achieve 12-bit high-precession computing. To enable a sub-mW system in AIoT applications, a Risc-V micro-processor with DSP instruction was designed with dynamic-voltage-and-frequency-scaling (DVFS) to adapt with various low-power and real-time computing tasks. The chip supports multiple NNs including DNN, TDNN, and RNN for different applications, e.g., smart voice, and health monitoring.

Biography

Shaodi received his B.S. degree from Peking University in 2011.and the Ph.D. degree in electrical engineering from UCLA in 2017. He founded WITINMEM Co. Ltd in 2017, and currently serves as the CEO of WITINMEM and is dedicated to developing chips with computing-in-memory technology. Shaodi published 20+ journal and conference papers and applied over 50 patents. He also served as reviewers and TPC in several IEEE and ACM journals and conferences.

Short Course STUP1-2

Damien Querlioz, Université Paris-Saclay, CNRS, France

"Emerging Device Technologies for Neuromorphic Computing and Machine Learning"

Abstract: In recent years, Artificial Intelligence (AI) has progressed to an astonishing level through the development of algorithms known as deep neural networks. Nevertheless, AI has to face a challenge: its considerable energy consumption, orders of magnitudes higher than the brain on similar tasks. Neuromorphic computing aims at designing electronic systems whose operating principles are to some extent inspired by the brain, to reduce the energy consumption of AI. In this tutorial, we will elucidate why the brain is more energy-efficient than current AI. This will teach us fundamental lessons on the design of neuromorphic systems, which should avoid the von Neumann bottleneck by closely associating computational units (artificial neurons) and memory units (artificial synapses). We will see that one of the biggest challenges, however, is the inadequacy of established memory technologies. We will then study how resistive memories, phase change, and spin torque memories, which naturally resemble synapses, can by contrast provide a solution. We will see that neuromorphic systems are sometimes less demanding in terms of device properties than conventional systems, which can allow using devices in a more optimal fashion. We will study the two main applications of neuromorphic hardware (inference and learning hardware), and show that they feature very different device requirements. We will also compare two visions for neuromorphic computing: the AI approach, which can bring immediate applications, and the longer-term neuroscience-inspired approach. We will see that both approaches do not call for the same electron device work. Finally, we will study recent developments that use the physics of conductive bridge and spin-torque devices, directly for computing, as well on 3-D integrated neuromorphic devices.

Biography

Damien Querlioz is a CNRS Researcher at the Centre de Nanosciences et de Nanotechnologies of Université Paris-Saclay. His research focuses on novel usages of emerging non-volatile memory and other nanodevices, in particular relying on inspirations from biology and machine learning. He received his predoctoral education at Ecole Normale Supérieure, Paris and his PhD from Université Paris-Sud in 2009. Before his appointment at CNRS, he was a Postdoctoral Scholar at Stanford University and at the Commissariat a l'Energie Atomique. Damien Querlioz is the coordinator of the interdisciplinary INTEGNANO

research group, with colleagues working on all aspects nanodevice physics and technology, from materials to systems. He is a member of the bureau of the French Biocomp research network, and a management committee member of the European MEMOCIS COST action. He has coauthored one book, nine book chapters, more than 100 journal articles and conference proceedings, and given more than 50 invited talks at national and international workshops and conferences. In 2016, he was the recipient of an ERC Starting Grant to develop the concept of natively intelligent memory. In 2017, he received the CNRS Bronze medal. He has also been a co-recipient of the 2017 IEEE Guillemin-Cauer Best Paper Award and of the 2018 IEEE Biomedical Circuits and Systems Best Paper Award.

Short Course STUP1-3

Qi Xiang, Xiamen Industrial Technology Research Institute Co., Ltd., China

"RRAM Based Computing-In-Memory"

Abstract: Artificial intelligence (AI) technologies, running state-of-the-art deep learning (DL) algorithms, demand significantly high computing power and energy efficiency. Computing power and energy efficiency for conventional computing hardware based on von Neumann architecture are limited by the so called "memory wall" problem due to physical separation of processing and memory units. Computing-In-Memory (CIM) based on emerging non-volatile memory devices, such as resistive random access memory (RRAM), is an emerging paradigm for hardware acceleration of AI workloads, and has potential to significantly increase computing power and energy efficiency for a DL accelerator. In this short course, we will focus on RRAM based CIM technology. We will first introduce the principles of RRAM based CIM technology. We will talk about the performance requirement of analog RRAM (or memristor) device. RRAM cell material system selection and process integration with an advanced logic CMOS process flow will be discussed. Modeling of analog RRAM device will be addressed. Co-design and co-optimization of device, circuit, architecture, and algorithm for AI accelerator chips will be discussed. We will summarize key challenges in CIM chip design and manufacturing with regards to the device non-idealities, analog-to-digital conversion, and process variations. State-of-the-art CIM-based prototype AI chips will be surveyed.

Biography

Dr. Qi Xiang is currently the Chief Technology Officer (CTO) of Xiamen Industrial Technology Research Institute Co., LTD (XITRI). Prior to joining XITRI, Dr. Xiang worked at Xilinx, GlobalFoundres, Altera (now Intel), and AMD in various engineering and management positions, including Director of Foundry Engineering at Xilinx, Director of DTCO and Fellow at GlobalFoundries, Senior Manager and Principal Engineer of Technology Development at Altera, and Manager of New Materials & Integration at AMD. He has more than 20 years of experience in semiconductor technology development and product manufacturing, from IDM, to design house, to foundry, and from process R&D, to foundry interface, to foundry design enablement. Dr. Xiang holds more than 200 US patents, and authored more than 70 technical papers. He served as a technical program committee member for various technical conferences, including IEDM, ICSICT, ICSI, DesignCon. He also served as a working group

member for ITRS and IRDS. He obtained BS, MS, and Ph.D. degrees in EE from Xi'an Jiaotong University. He worked as a post doctoral fellow in University of California, Los Angeles (UCLA) and Tsinghua University, Beijing, China.

Short Course 2 (STUP2)

"Quantum Computing Technologies"

Thursday, April 8, 2021

13:50–17:20 ShuShan Hall

Moderator: Qiang Zhou, Jong-Hyun Ahn

STUP2-1: 2:00 pm

Cryo-CMOS for Quantum Computing

Edoardo Charbon, EPFL, Switzerland

STUP2-2: 3:10 pm

Understanding quantum computing by quantum algorithms

Lvzhou Li, Sun Yat-sen University, China

STUP2-3: 4:20 pm

Quantum computing using superconducting quantum coherence devices

Yuxi Liu, Tsinghua University, China

Short Course STUP2-1

Edoardo Charbon, EPFL, Switzerland

"Cryo-CMOS for Quantum Computing"

Abstract : Quantum computing holds the promise to solve intractable problems using processors that exploit quantum physics concepts, such as superposition and entanglement. The core of a quantum processor is generally an array of qubits that need to be controlled and read out by a classical processor. This processor operates on the qubits with nanosecond latency, several millions of times per second, with tight constraints on noise and power. This is due to the extremely weak signals involved in the process that require highly sensitive circuits and systems, along with very precise timing capability. We advocate the use of CMOS technologies to achieve these goals, whereas the circuits will be operated at deep-cryogenic temperatures. We believe that these circuits, collectively known as cryo-CMOS control, will make future qubit arrays scalable, enabling a faster growth in qubit count. In the lecture, the challenges of designing and operating complex circuits and systems at 4K and below will be outlined, along with preliminary results achieved in the control and read-out of qubits by ad hoc integrated circuits that were optimized to operate at low power in these conditions. The talk will conclude with a perspective on the field and its trends.

Biography

Edoardo Charbon (SM'00 F'17) received the Diploma from ETH Zurich, the M.S. from the University of California at San Diego, and the Ph.D. from the University of California at Berkeley in 1988, 1991, and 1995, respectively, all in electrical engineering and EECS. He has consulted with numerous organizations, including Bosch, X-Fab, Texas Instruments, Maxim, Sony, Agilent, and the Carlyle Group. He was with Cadence Design Systems from 1995 to 2000, where he was the Architect of the company's initiative on information hiding for intellectual property protection. In 2000, he joined Canesta Inc., as the Chief Architect, where he led the development of wireless 3-D CMOS image sensors. Since 2002 he has been a member of the faculty of EPFL. From 2008 to 2016 he was with Delft University of Technology's as full professor and Chair of VLSI design. He has been the driving force behind the creation of deep-submicron CMOS SPAD technology, which is mass-produced since 2015 and is present in telemeters, proximity sensors, and medical diagnostics tools. His interests span from 3-D vision, LiDAR, FLIM, FCS, NIROT to super-resolution microscopy, time-resolved Raman spectroscopy, and cryo-CMOS circuits and systems for quantum computing. He has authored

or co-authored over 350 papers and two books, and he holds 23 patents. Dr. Charbon is a distinguished visiting scholar of the W. M. Keck Institute for Space at Caltech, a fellow of the Kavli Institute of Nanoscience Delft, a distinguished lecturer of the IEEE Photonics Society, and a fellow of the IEEE.

Short Course STUP2-2

Lvzhou Li, Sun Yat-sen University, China

"Understanding quantum computing by quantum algorithms"

Abstract: The fundamental reason why quantum computing attracts so much attention is that it has powerful parallel computing ability, which can efficiently solve some problems that are quite difficult for classical computers. For example, Shor's algorithm can solve the factorization problem in polynomial time, which thus poses a great threat to RSA cryptography. However, the parallel computing power of quantum computation is not directly available since the ingenious algorithm design centered on the target problem is required. This talk will introduce the basic principles, development history and typical ones of quantum algorithms so that the audience can have some basic understanding of how quantum computing can speed up problem solving.

Biography

Lvzhou Li is a professor at Institute of Quantum Computing and Computer Science Theory, School of Computer Science and Engineering, Sun Yat-Sen University. He obtained Ph.D in Computer Science from Sun Yat-sen University in 2009. His researches focus on quantum computing models, algorithms, and complexity. He has published more than 60 papers and one monograph. He is a distinguished member and distinguished lecturer of China Computer Federation (CCF).

Short Course STUP2-3

Yuxi Liu, Institute of Microelectronics, Tsinghua University, China

"Quantum computing using superconducting quantum coherence devices"

Abstract : There are various model systems, which may be used to realize quantum information processing. In the past 20 years, significant progress has been made in superconducting quantum circuits, which provide a platform to manipulate microwave photons and implement quantum information processing. This talk will introduce several superconducting quantum coherence devices, and show you how to design basic model for quantum computing using these coherence devices. The recent progress of the superconducting quantum computing is also summarized. Finally, I will present our recent research results on developing superconducting quantum circuit models for quantum computing and simulations.

References

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[4] Y. J. Zhao, X.W. Xu, H. Wang, Y. X. Liu, and W. M. Liu, Phys. Rev. A 102, 053722 (2020)

Biography

Yu-xi Liu is a Professor at the Institute of Microelectronics, Department of Micro- and Nano-oelectronics, Tsinghua University of China. He received his Ph.D. degree from the Department of Physics, Peking University in 1998. From 1998 to 2000, he was a Postdoctoral Researcher at the Institute of Theoretical Physics, the Chinese Academy of Sciences, China. From 2000 to 2002, he was a JSPS Postdoctoral fellow at the Graduate University for Advanced Studies (SOKENDAI), Japan. From 2002 to 2009, he was a research scientist in the Institute of Physical and Chemical Research (RIKEN), Japan. Since 2009, he has been a full Professor at Tsinghua University. He is an expert of superconducting quantum devices and solid-state quantum computing theories. His research interests include superconducting quantum devices and quantum information processing, hybridization of superconducting quantum devices with photonic/phononic devices, quantum control theory, and quantum artificial intelligence. He has made several contributions to superconducting quantum coherence devices and quantum computing, and published about 140 journal papers, including Nature Photonics (3), Phys. Rep. (2), Phys. Rev. Lett. (13), Phys. Rev. A/B/E/Research/Applied (105), and other journals.

Short Course 3 (STUP3)

"Advanced Processing and Manufacturing"

Thursday, April 8, 2021

13:50–17:20 ShuYun Hall

Moderator: Wei-Min Gao, Udayan Ganguly

STUP3-1: 2:00 pm

Layer transfer technology of post-Si materials for monolithic 3D integration

Tatsuro Maeda, National Institute of Advanced Industrial Science and Technology, Japan

STUP3-2: 3:10 pm

Device/Process Technology Challenges for CMOS System Evolution

Digh Hisamoto, Hitachi, Japan

STUP3-3: 4:20 pm

EUV lithography and its applications to logic and memory devices

Wei-Min Gao, ASML China

Short Course STUP3-1

Tatsuro Maeda, National Institute of Advanced Industrial Science and Technology, Japan

"Layer transfer technology of post-Si materials for monolithic 3D integration"

Abstract: Monolithic 3D integration has emerged as a promising technological solution for high density, high performance, and multi-functional integrated circuits. To enhance the performance and expand the functionality of current Si-based semiconducting platforms, the layer transfer technology of post-Si materials, such as Ge and III-V semiconductors onto Si substrates has attracted a lot of attention. Key challenges are how to maintain the material quality of transferred layers from donor wafer, and how to fabricate high-performance devices under low-thermal budget processes on Si. In this talk, we discuss the layer transfer technology for integrating Ge and III-V devices and their applicability for building the emerging monolithic 3D devices.

Biography

Dr. Tatsuro Maeda is Research Manager at National Institute of Industrial Science and Technology (AIST), Ibaraki, Japan. He received Ph. D. degree in material science from Tokyo Institute of Technology in Japan in 1996. In 1996, he joined the Electron Device Division, Electrotechnical Laboratory, Ibaraki, Japan where he has been engaged in the research on the fabrication and the characterization of ultrasmall SOI-MOSFETs, nano-scale Si-based devices, and single electron transistors for future CMOS components. In 2001, he joined AIST as a senior researcher. Now he belongs to Device Technology Research Institute at AIST. His current research interests include heterogeneous integration of post-silicon devices such as SiGe, Ge, and III-V materials onto Si LSI to expand the functionality of current Si CMOS technology. He has authored or co-authored over 100+ publications and patents related to nanoelectronics research fields.

Short Course STUP3-2

Digh Hisamoto, Research & Development Group, Hitachi, Ltd., Japan

"Device/Process Technology Challenges for CMOS System Evolution"

Abstract: Triggered by the introduction of FinFET, the evolution of device structure has been actively considered. By considering the history of CMOS device developments so far, here, we will discuss the direction of device evolution and explore the features required for future devices. Due to the system / architecture requirements, the input method functionality plays an important role in determining the device structure. Based on these, we will review the current challenges of device and process technologies.

Biography

Digh Hisamoto received the B.S., M.S. degrees in reaction chemistry and Ph.D. degree in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1984, 1986, and 2003, respectively.

In 1986, he joined Central Research Laboratory, Hitachi, Ltd., Tokyo, where he has been working on ULSI device physics and process technologies. He developed scaled CMOS devices and memory devices including DELTA (fully depleted lean-channel transistor), the original model of the FinFET. From 1997 to 1998, he was a Visiting Industrial Fellow at the University of California, Berkeley, where he created the first FinFET.

Since 2000, he has developed embedded non-volatile Flash memories using split-gate MONOS charge-trapped technology. Currently, he has expanded the research interests into RF devices, tunnel FETs, wide bandgap semiconductor power devices, quantum sensing devices, and quantum computing devices.

He has served as a committee member of International Conference on Solid State Devices and Materials (SSDM), International Electron Devices Meeting (IEDM) and VLSI Symposia. And also, he served as Director of Japan Applied Physics (JSAP) and assigned to Visiting Professor of School of Engineering, Tokyo Institute of Technology.

Dr. Hisamoto is Fellow of IEEE and JSAP. Currently, he is Technology Advisor, Research and Development Group, Hitachi, Ltd.

Short Course STUP3-3

Wei-Min Gao, ASML, China

"EUV lithography and its applications to logic and memory devices"

Abstract : This course will cover the basic theory of EUV lithography, the history and present status of EUV lithography; It will explain the applications of EUV lithography to both advanced logic and memory processes in high volume manufactory; it will also discuss the extension of 0.33NA EUV (low k1 EUV) and the future high NA EUV lithography.

Biography

Weimin Gao received his bachelor's degree from Zhejiang University, China and obtained Ph.D. in physics from KU Leuven, Belgium. He joined ASML in 2018 as a technical director in its Technology Development Center. Prior to joining ASML, he served as the Synopsys assignee at imec for over 10 years. Dr. Gao is an expert in advanced optical lithography with more than 19 years of R&D experience. He has participated in the lithographic development of multiple generations of advanced CMOS technology. His technical expertise covers a wide range of lithographic fields including the process development, advanced imaging, RETs, modeling, OPC, reticle, DTCO, and metrology. For the past 10 years, his research activities has focused on the development of EUV lithography and he is currently working on EUV extension and enabling technologies including high-NA EUV lithography. Dr. Gao has over 100 publications in various international journals and conferences and has given invited presentations at many international conferences.

Short Course 4 (STUP4)

“Ultra/Wide Bandgap Power Electronics”

Thursday, April 8, 2021

13:50–17:20 ShuJin Hall

Moderator: Mengyuan Hua, Shaibal Mukherjee

STUP4-1: 2:00 pm

Integration with GaN-on-Si Power HEMT platform

Kevin J. Chen, Hong Kong University of Science and Technology, Hong Kong, China

STUP4-2: 3:10 pm

Energy efficient power switches with Gallium Nitride technology

Srabanti Chowdhury, Stanford University, California, USA

STUP4-3: 4:20 pm

Element Technology for Next Generation High- to Ultra-High Voltage SiC Power Device

Yoshiyuki Yonezawa, AIST, Japan

Short Course STUP4-1

Kevin J. Chen, Hong Kong University of Science and Technology, Hong Kong, China

"Integration with GaN-on-Si Power HEMT platform"

Abstract: Group-III/nitride semiconductors have exhibited strong capability and flexibility informing large-area heterojunctions (e.g. AlGaN/GaN) with high quality and high uniformity Using epitaxial growth techniques. These heterojunctions yield polarization-induced highmobility 2DEG channel that forms the basis of GaN HEMT, which is currently the dominant technology platform for commercial applications, such as high-frequency power amplifiers for wireless base-stations and power switching devices for compact power conversions. The GaN HEMT structure is planar in nature, with the inherent benefit of high-density integration that can be utilized to increase functionality, optimize performance and improve reliability. An immediate beneficiary of such an integration is the GaN power switching components currently being commercialized using advanced 6- or 8-inch GaN-on-Si power HEMT technology. The parasitic inductances from the interconnection bonding wires and PCB traces often create the bottleneck in exploiting the full potential of GaN power devices switching at high frequencies, since they could induce voltage spikes/oscillations that may lead to various reliability issues. Large gate voltage spikes could degrade the gate junction, as the gate drive voltage window of the commercial p-GaN gate power HEMTs is much narrower than Si and SiC MOSFETs. The GaN power transistors also have a relatively low VTH and are likely to suffer false turn-on. By monolithically integrating gate driving circuits with the power switch, parasitic inductance between gate driver and the power device can be greatly reduced to obtain cleaner gate driving signals and more robust switching characteristics. Furthermore, the integration of core power components with peripheral devices enables incorporation of functionality/reliability enhancement blocks, such as on-chip protection and sensing modules. The development of GaN power integration technology based on a commercially available pGaN gate HEMT platform will be reviewed and discussed. An integrated gate driving IC will be presented as an example of practical implementation. By adopting a bootstrap unit, the integrated gate driver enables rail-to-rail driving capability and ultrafast switching with clean waveforms and enhanced gate reliability. From power IC design point of view, the unique dynamic V_{TH} of the voltage-driven p-GaN power transistors and the corresponding SPICE model will be introduced, and its impact on the GaN power IC design. The prospects for future GaN power IC development will also be discussed, including multi-functional GaN power devices, GaN CMOS technology.

Biography

Prof. Kevin J. Chen received his B.S. degree from Peking University, China in 1988, and PhD degree from University of Maryland, College Park, USA in 1993. He has obtained industry experience by conducting R&D work on III-V high-speed device technologies in NTT LSI Laboratories, Japan and Agilent Technologies, USA. Prof. Chen joined Hong Kong University of Science and Technology (HKUST) in 2000, where he is currently a professor in the Department of Electronic and Computer Engineering. Prof. Chen has more than 600 publications in international journals and conference proceedings. He has been granted 12 US patents on GaN electron device technologies. His research is currently focused on developing wide-bandgap semiconductor device technologies for high-power and high-frequency applications. He is a Fellow of IEEE. He is a guest editor for the 2013 special issue of IEEE Transactions on Electron Device on “GaN Electronic Devices”. He is currently an editor for IEEE Transactions on Electron Devices and has served as an editor for IEEE Transactions on Microwave Theory and Techniques and Japanese Journal of Applied Physics.

Short Course STUP4-2

Srabanti Chowdhury, Stanford University, USA

"Energy efficient power switches with Gallium Nitride technology"

Abstract : GaN technology is an ever-expanding topic of research and development, proving its potential to solve several challenges in power conversion that cannot be addressed by Si. For instance, medium voltage (650-900V) devices using the HEMT configuration have been able to reduce form factor at the system level by driving circuits at higher frequencies (100KhZ-1Mhz) and eliminating heat sinks or reducing cooling requirements. This alone sparked the interest in GaN research to save space, energy and ultimately cost of power conversion. However, in power conversion the demand of high current from a single chip for a rated voltage is a standard need. Particularly when the market is favorable towards electrification of cars and other means of transportations, GaN must expand its scope to provide high power solutions with higher power density compared to Si, and even SiC. Vertical devices have been the choice of power device engineers for economic use of the material and maximum use of its physical properties (which allow highest possible blocking field, field mobility, etc.). GaN vertical devices, therefore, carry all the advantages offered by vertical geometry and are being explored increasingly with emphasis on material and device needs.
An overview of the recent achievements in vertical Gallium Nitride (GaN)-based power electronic devices will be presented with particular reference to a current aperture vertical electron transistor (CAVET), MOSFETs an oxide, GaN interlayer FET (OGFET), Static Induction Transistor (SIT), and high voltage diodes. We have done systematic study of several types of vertical devices and compared their performances. Lateral HEMTs will be discussed and their current issues will be elaborated with specific examples.
Prevalent opinion suggests GaN HEMTS are suitable for 650V, while vertical devices are more suited for 1.2kV and up. In this tutorial I would build discuss the device performance for both topologies and allude to the overall (most likely system-level, but also device-level) cost that is an important metric for the successful commercialization of power deices. Finally, there will be some discussion of device fundamentals that include the role of avalanche breakdown, and likelihood of impact ionization of carriers in GaN power devices.

Biography

Srabanti Chowdhury (George and Ida Mary Hoover faculty fellow'19, Gabilan fellow '19) is an associate professor of Electrical Engineering (EE), and Center Fellow, by courtesy, at the

Precourt Institute for Energy at Stanford University. Her research focuses on wideband gap (WBG) materials and device engineering for energy efficient and compact system architecture for power electronics, and RF applications. Besides Gallium Nitride, her group is exploring Diamond for various electronic applications. She received her B.Tech in India in Radiophysics and Electronics (Univ. of Calcutta) and her M.S and PhD in Electrical Engineering from University of California, Santa Barbara. She received the DARPA Young Faculty Award, NSF CAREER and AFOSR Young Investigator Program (YIP) in 2015. In 2016 she received the Young Scientist award at the International Symposium on Compound Semiconductors (ISCS). She is a senior member of IEEE and an invitee by the NAE to the 2019 symposium on Frontiers of Engineering. She received the Alfred P. Sloan fellowship in Physics in 2020. To date, her work has produced over 5 book chapters, 85 journal papers, 100 conference presentations, and 26 issued patents. She leads the WBG-Lab and affiliated with System-X alliance at Stanford University.

Short Course STUP4-3

Yoshiyuki Yonezawa, National Institute of Advanced Industrial Science and Technology (AIST), Japan

"Element Technology for Next Generation High- to Ultra-High Voltage SiC Power Device"

Abstract: In order to achieve the goal of zero greenhouse gas emissions and to meet the expected explosive increase in electricity demand associated with ICT and the electrification of vehicles, it will be necessary to introduce and control a large amount of renewable energy, as well as to conserve energy in consumption. Under such circumstances, the role of power electronics and power device are becoming increasingly important in the energy value chain from power transmission and distribution to energy consumption.

The evolution of power electronics has been supported by improvements in Si-IGBTs. However, since the theoretical limit of Si has been reached, expectations for SiC devices are increasing. Since SiC has a breakdown electrical field ten times higher than Si a blocking voltage one order of magnitude higher with SiC compared to Si is expected using the same structure.

In this short course, the current status of SiC power devices and issues such as forward degradation and countermeasures are introduced. Furthermore, efforts to develop next-generation SiC superjunction MOSFET and ultra-high voltage SiC-IGBT elemental technologies aiming at lower loss and higher breakdown voltage will be reported.

Biography

Yoshiyuki Yonezawa received his Ph.D. degree from Tokyo Institute of Technology, based on his work in SiC power devices and solution growth of SiC crystal. From 1989 to 2013, he was an engineer at Fuji Electric Co., Ltd., where he was engaged in research and development in solid state laser system, hard disk media, dielectric thin films for DC/DC converter, and SiC power devices, and led the SiC group. He was a visiting scholar at Stanford University from 1996 to 1998. He joined National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, Japan, in 2013 at Advanced Power Electronics Research Center. He is currently a principal research manager and his research involves SiC high voltage SJ-MOSFET, ultra-high-voltage IGBTs and related fundamental technologies.

Technical Sessions

Friday, April 9, 2021

13:30–15:10 ShuFeng Hall

Invited Session WE1P1: Materials Growth and Applications

Chair: Genquan Han, Xidian University
Co-Chair: Daniel Herr, University of North Carolina, Greensboro

WE1P1-1 13:30

Pushing the Limit of Lithography for Patterning Two-Dimensional Lattices in III-V Semiconductor Quantum Wells (Invited talk)

N.A. Franchina Vergel[1], C. Post[2], F. Vaurette[1], Y. Lambert[1], D. Yarekha[1], C. Coinon[1], G. Fleury[3], T.S. Kulmala[4], T. Xu[5], L. Desplanque[1], X. Wallart[1], D. Vanmaekelbergh[2], C. Delerue[1], B. Grandidier[1]; [1]Univ. Lille, France,[2]Utrecht University, The Netherlands, [3]Univ. Bordeaux, France,[4]Heidelberg Instruments, Switzerland,[5]Shanghai University, China

WE1P1-2 13:50

Graphene Synthesis: From Single Crystalline Wafer to Edge Specific Nano-Ribbon (Invited talk)

Zengfeng Di, Tianru Wu, Haomin, Wang, Qingkai Yu, Xiaoming Xie; Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, China

WE1P1-3 14:10

Artificial Heterostructures Enabled by Remote Epitaxy (Invited talk)

Jeehwan Kim; Massachusetts Institute of Technology, USA

WE1P1-4 14:30

Non-Volatile FETs with Amorphous (Al_2O_3, HfO_2, ZrO_2, Etc.) Gate Insulators (Invited talk)

Yan Liu, Yue Peng, Genquan Han; Xidian University, China

WE1P1-5 14:50

Silicon Nanocrystals: Fabrication, Physical Properties and Applications (Invited talk)

Ilya Sychugov; KTH Royal Institute of Technology, Sweden

Friday, April 9, 2021

13:30–15:10 ShuShan Hall

Session WE1P2: Hot carrier relaibility and Neuromorphic reliability

Chair: Runsheng Wang, Peking University
Co-Chair: Yuan Zhang, Amazon

WE1P2-1 13:30

Hot Carrier Degradation in Classical and Emerging Logic and Power Electronic Devices: Rethinking Reliability for Next-Generation Electronics (Invited talk)

Muhammad Ashraful Alam, Bikram Kishore Mahajan, Yen-Pu Chen; Purdue University, USA

WE1P2-2 13:50

Hot-Carrier-Induced Reliability Concerns for Lateral DMOS Transistors with Split-STI Structures

Li Lu[1], Ran Ye[1], Siyang Liu[1], Zhibo Yin[1], Yuanchang Sang[1], Weifeng Sun[1], Wei Su[2], Feng Lin[2], Shulang Ma[2], Yuwei Liu[2]; [1]Southeast University,China, [2]CSMC Technologies Corporation, China

WE1P2-3 14:10

Identifying Relaxation and Random Telegraph Noises in Filamentary Analog RRAM for Neuromorphic Computing

Qi Hu[1], Bin Gao[1], Jianshi Tang[1], Zhenqi Hao[1], Peng Yao[1], Yudeng Lin[1], Yue Xi[1], Meiran Zhao[1], Jiezhi Chen[2], He Qian[1],Huaqiang Wu[1]; [1]Tsinghua University, China, [2]Shandong University, China

WE1P2-4 14:30

Nonlinear Weight Quantification for Mitigating Read Disturb Effect on Multilevel RRAM-Based Neural Network

Lindong Wu, Zongwei Wang , Zhizhen Yu, Yabo Qin, Qingyu Chen, Yimao Cai , Ru Huang; Peking University, China

WE1P2-5 14:50

Predicted static fatigue lifetime of silica optical interconnects: application of Boltzmann-Arrhenius-Zhurkov (BAZ) model (Invited talk)

Ephraim Suhir; Portland State University, USA

Friday, April 9, 2021

13:30–15:10 ShuYun Hall

Session WE1P3: Heterogeneous Integration

Chair: Yifan Guo, ASE
Co-Chair: Jian Cai, Tsinghua University

WE1P3-1 13:30

Heterogeneous Integration for Silicon Photonic Systems: Challenges and Approaches (Invited talk)

John M. Dallesasse, John A. Carlson, Manaav Ganjoo, Leah Espenhahn; University of Illinois at Urbana-Champaign, USA

WE1P3-2 13:50

Effect of Leveler on Electrical Resistance and Microstructural of Electroplated Copper After Heat Treatment

Lingyue Tan, Silin Han, Shuhui Chen, Chu Liang, Yunwen Wu, Huiqin Ling, Ming Li, Tao Hang; Shanghai Jiao Tong University, China

WE1P3-3 14:10

Heterogenous Integration of InP DHBT and Si CMOS by 30μm Pitch Au-In Microbumps

LiShu Wu[1,2], JiaYun Dai[1], Cheng Wei[1], YueChan Kong[1], TangShen Chen[1], Tong Zhang[2]; [1]Science and Technology on Monolithic Integrated Circuits and Modules Laboratory Nanjing Electronic Devices Institute, China, [2]Southeast University, China

WE1P3-4 14:30

Simulation of fast room-temperature bonding by mechanical interlock structure applied for 3D integration

Ziyu Liu, Yaomin Gong, Lin Chen, Qingqing Sun, David Wei Zhang; Fudan University, China

WE1P3-5 14:50

Low Temperature Packaging for Ion-Sensitive Organic Field Effect Transistor

Yixiao Tang, Wei Tang, Yukun Huang, Yawen Song, Bang Ouyang, Xiaojun Guo; Shanghai Jiao Tong University, China

Friday, April 9, 2021

13:30–15:10 ShuJin Hall

Session WE1P4: New memories and in memory computing

Chair: Hangbing Lv, IMECAS
Co-Chair: Kai Ni, RIT

WE1P4-1 13:30

Ferroelectric field-effect transistors for the next-generation storage (Invited talk)

Cheol Seong Hwang; Seoul National University,Korea

WE1P4-2 13:50

Toward Energy-efficient, Cost-effective, and Variation-aware In-memory Computing for Deep Learning Acceleration (Invited talk)

Tuo-Hung Hou; National Chiao Tung University, China

WE1P4-3 14:10

Design Limits of In-Memory Computing: Beyond the Crossbar (Invited talk)

Gokul Krishnan[1], Jubin Hazra[2], Maximilian Liehr[2], Xiaocong Du[1], Karsten Beckmann[2], Rajiv V. Joshi[3], Nathaniel C. Cady[2], Yu Cao[1]; [1]Arizona State University,USA, [2]State University of New York Polytechnic Institute,USA, [3]IBM T. J. Watson Research Center Yorktown Heights,USA

WE1P4-4 14:30

Three-Orders Improvement of Endurance in Hafina Based MFS Capacitor Through CF_4 Plasma Pre-Treatment

Shuxian Lv[1, 2], Yan Wang[1, 2], Zhaomeng Gao[1, 2], Zhiwei Dang[1, 2], Pengfei Jiang[1, 2], Peng Yuan[1,2], Qing Luo[1, 2], Shengjie Zhao[1], Hangbing Lv[1, 2]; [1]Institute of Microelectronics of Chinese Academy of Sciences, China; [2]University of Chinese Academy of Sciences, China

WE1P4-5 14:50

A RRAM Based Max-Pooling Scheme for Convolutional Neural Network

Yaotian Ling, Zongwei Wang, Yunfan Yang, Zhizhen Yu, Qilin Zheng, Yabo Qin, Yimao Cai, Ru Huang; Peking University, China

Friday, April 9, 2021

15:30–17:10 ShuFeng Hall

Session WE2P1: MEMS and Sensors

Chair: Jiahao Zhao, Tsinghua University
Co-Chair: Evelyn Wang, Massachusetts Institute of Technology

WE2P1-1 15:30

Piezoelectric Micromachined Ultrasonic Transducers for Range-Finding Applications (Invited talk)

David A. Horsley[1,2], Richard J. Przybyla[1], Stefon E. Shelton[1], Fabian T. Goericke[1], Benjamin E. Eovino[1], Michael Alex[1] , John Logan[1]; [1]Chirp Microsystems Corporation,USA, [2]University of California, Davis, USA

WE2P1-2 15:50

Biaxially-Stretchable Kirigami-Patterned Mesh Structures for Motion Artifact-Free Wearable Devices (Invited talk)

Hyo Chan Lee[1], Ezekiel Y. Hsieh[1],SungWoo Nam[1,2]; [1]Department of Mechanical Science and Engineering, University of Illinois at Urbana – Champaign, USA, [2]Department of Materials Science and Engineering, University of Illinois at Urbana – Champaign, USA

WE2P1-3 16:10

Thermal Infrared Detector Sparse Array for NASA Planetary Applications (Invited talk)

M. Bulut Coskun[1], Mina Rais-Zadeh[1,2]; [1]California Institute of Technology,USA, [2]University of Michigan, Ann Arbor, USA

WE2P1-4 16:30

Double-Deck Metal Solenoids 3D Integrated in Silicon Wafer for Kinetic Energy Harvester

Nianying Wang[1,2,3], Ruofeng Han[1,3], Changnan Chen[1,3], Jiebin Gu[1,3], and Xinxin Li[1,2,3]; [1]Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, China, [2]ShanghaiTech University, China, [3]University of Chinese Academy of Sciences, China

WE2P1-5 16:50

A Novel Piston-Like Piezoelectric Micromachined Ultrasonic Transducer Based on Mass Loading Effect

Lei Wang， Jie Zhou, Wei Zhu, Zhipeng Wu, Wenjuan Liu, Chengliang Sun; Institute of Technological Sciences, China

Friday, April 9, 2021

15:30–17:10 ShuShan Hall

Session WE2P2: Photonic Devices

Chair: Lili Wang, Chinese Academy of Sciences
Co-Chair Myungsoo Kim, University of Texas at Austin

WE2P2-1 15:30

Analog Switches Based on Boron Nitride Memristors for Application in 5G and Terahertz Communication Systems (Invited talk)

Myungsoo Kim[1], Emiliano Pallecchi[2], Guillaume Ducournau[2], Henri Happy[2], Deji Akinwande[1]; [1]University of Texas at Austin, USA, [2] University of Lille, France

WE2P2-2 15:50

Photonic Machine Intelligence: Photonic Tensor Core and Nonvolatile Memories (Invited talk)

Volker J. Sorger; George Washington University, USA

WE2P2-3 16:10

Efficient Silicon Photonic Waveguide Switches for Chip-Scale Beam Steering Applications (Invited talk)

Li-Yuan Chiang[1], Chun-Ta Wang[2], Steve Pappert[1], Paul K. L. Yu[1]; [1]University of California San Diego, USA, [2]National Sun Yat-Sen University, China

WE2P2-4 16:30

A Design of Horizontal Perovskite Nanowire LED for Better Light Extraction

Qianpeng Zhang[1,2], Yuanjing Lin[3], Xiaofei Sun[1], Bryan Cao[1], Haoning Tang,[4], Zhiyong Fan[1,2]; [1]The Hong Kong University of Science and Technology, China, [2]HKUST-Shenzhen Research Institute, China, [3]Southern University

WE2P2-5 16:50

Loss Compensation Symmetry for TE Modes of Asymmetrical Optical Coupler with Gain and Loss

Anton Hlushchenko[1,2], Vitalii Shcherbinin[2], Denis Novitsky[3], Vladimir Tuz[1]; [1]Jilin University, China, [2]Institute of Physics and Technology of NASU, Ukraine, [3]NASB, Belarus

Friday, April 9, 2021

15:30–17:10 ShuYun Hall

Session WE2P3: 2D materials and devices I

Chair: Xinran Wang, Nanjing University
Co-Chair: Zenghui Wang, UESTC

WE2P3-1 15:30

All 2D Heterostructure Tunnel Field Effect Transistors (Invited talk)

Kosuke Nagashio; University of Tokyo, Japan

WE2P3-2 15:50

ALD Encapsulation of CVD WS2 for Stable and High-Performance FET Devices (Invited talk)

Xiangyu Wu, Dennis Lin, Daire Cott, Jean-Francois de Marneffe, Benjamin Groven, Stephanie Sergeant, Yuanyuan Shi, Quentin Smets, Surajit Sutar, Inge Asselberghs, Iuliana Radu; IMEC, Belgium

WE2P3-3 16:10

Epitaxial Growth of Single-Crystal Two-Dimensional Materials for Electronic Applications (Invited talk)

Areej Aljarb[1,2], Vincent Tung[1], Lain-Jong Li[1,3]; [1]KAUST Solar Centre, Kingdom of Saudi Arabia, [2]King Abdulaziz University, Kingdom of Saudi Arabia, [3] TSMC Taiwan

WE2P3-4 16:30

A Compact Model for Transition Metal Dichalcogenide Field Effect Transistors with Effects of Interface Traps

Yifei Xu, Weisheng Li, Dongxu Fan, Yi Shi, Hao Qiu, Xinran Wang; National Laboratory of Solid State Microstructures, School of Electronic Science and Engineering and Collaborative Innovation Center of Advanced Microstructures, Nanjing University, Nanjing, China

WE2P3-5 16:50

Reliability of Ultrathin High-k Dielectrics on 2D Semiconductors

Zhihao Yu[1,2] , Hongkai Ning[2], Weisheng Li[2] , Lei Liu[2] , Wanqing Meng[2] , Zhongzhong Luo[2] , Songhua Cai[3] , Taotao Li[2], Peng Wang[3] , Yi Shi[2] , Yong Xu[1] , Xinran Wang[2]; [1]Nanjing University of Posts and Telecommunications, China, [2]School of Electronic Science and Engineering, Nanjing University, China, [3]College of Engineering and Applied Sciences, Nanjing University, China

Friday, April 9, 2021

15:30–17:10 ShuJin Hall

Session WE2P4: Charge based memories

Chair: Shimeng Yu, Georgia Institute of Technology
Co-Chair: Bing Chen, Zhejiang University

WE2P4-1 15:30

The Case for Ferroelectrics in Future Memory Devices (Invited talk)

Thomas Mikolajick[1,2], Uwe Schroeder[1], Stefan Slesazeck[1];[1]NaMLab gGmbH, Germany, [2]IHM, Germany

WE2P4-2 15:50

A Multiscale Statistical Evaluation of DRAM Variable Retention Time (Invited talk)

Plamen Asenov[1] , Salvatore M. Amoroso[1] , Jaehyun Lee[1] , Fabiano Corsetti[4] , Pieter Vancraeyveld[4] , Søren Smidstrup[4] ,Xi-Wei Lin[3] ,Victor Moroz[3]; [1]Synopsys, Scotland, [2]Synopsys, Denmark, [3]Synopsys, USA

WE2P4-3 16:10

3D-NAND cell challenges to enable high density and high performance devices (Invited talk)

Tecla Ghilardi; Micron

WE2P4-4 16:30

Performance Boost of p-MOSFET with Al-Incorporated HfSiOx in DRAM Periphery Transistor Application

Xingsong Su, Kang You, Mengmeng Yang, Juanjuan Huang, Wei Yang, Weiping Bai, Jie Bai, Er-xuan Ping; Changxin Memory Technologies, Inc, China

WE2P4-5 16:50

Cryogenic Operation of 3D Flash Memory for New Applications and Bit Cost Scaling with 6-Bit per Cell (HLC) and Beyond

Yuta Aiba, Hitomi Tanaka, Takashi Maeda, Keiichi Sawa, Fumie Kikushima, Masayuki Miura, Toshio Fujisawa, Mie Matsuo, Tomoya Sanuki; Kioxia Corporation, Japan

Saturday, April 10, 2021

11:30–12:30 ShuFeng Hall

Session TH1A1: Advanced Process Technology III

Chair: Ming Li, Peking University
Co-Chair: Walter Schwarzenbach, SOITEC

TH1A1-1 11:30

Smart Cut SiC Substrates for Manufacturing of High Quality Power Devices (Invited talk)

Walter Schwarzenbach; SOITEC, France

TH1A1-2 11:50

Directed Self-Assembly of Block Copolymers for Microelectronic Manufacturing (Invited talk)

Shisheng Xiong; Fudan University, China

TH1A1-3 12:10

Nanolithography to Beat the Diffraction Limit Using Ultrafast Laser (Invited talk)

Xuanming Duan; Jinan University, China

Saturday, April 10, 2021

11:30–12:30 ShuShan Hall

Session TH1A2: Flexible Devices

Chair: Xiaojun Guo, Shanghai Jiao Tong University
Co-Chair: Sheng Xu, University of California, San Diego

TH1A2-1 11:30

Flexible Semiconductor Device Technologies (Invited talk)

Huilong Zhang, Tzu-Hsuan Chang, Seunghwan Min, Zhenqiang Ma; University of Wisconsin-Madison, USA

TH1A2-2 11:50

Personalized Medicinal Platform (Invited talk)

Muhammad M. Hussain; King Abdullah University of Science and Technology, Saudi Arabia

TH1A2-3 12:10

Low-Voltage Synaptic Transistor Based on Polyvinylpyrrolidone Composite Electrolyte for Humidity Sensing

Wenhui Fu[1], Jiang Dongliang[1] , He Liangchun[1] ,Yang Yaohua[1] , Chen Qi[1] , Zhang Jianhua[2], Li Jun[1]; [1]Shanghai University, China, [2]Ministry of Education, Shanghai University, China

Saturday, April 10, 2021

11:30–12:30 ShuYun Hall

Session TH1A3: Emerging devices for in-memory and neuromorphic computing

Chair: Haifeng Yu, Peking University
Co-Chair: Jianjun Zhang, Chinese Academy of Sciences

TH1A3-1 11:30

A BEOL Compatible, 2-Terminals, Ferroelectric Analog Non-Volatile Memory

Laura Bégon-Lours, Mattia Halter, Diana Dávila Pineda, Youri Popoff, Valeria Bragaglia, Antonio La Porta, Daniel Jubin, Jean Fompeyrine, Bert Jan Offrein; IBM Zurich Research Laboratory, Switzerland

TH1A3-2 11:50

A Novel Leaky-FeFET Based True Random Number Generator with Ultralow Hardware Cost for Neuromorphic Application

Tianyi Liu[1] , Jin Luo[1] , Xinming Wei[1] ,Qianqian Huang[1,2] , Ru Huang[1,2]; [1] Peking University, China, [2]National Key Laboratory of Science and Technology on Micro/Nano Fabrication, China

TH1A3-3 12:10

$Hf_{1-x}Zr_xO_2$ Based Bipolar Selector with High Uniformity and High Selectivity for Large-Scale Integration of Memristor Crossbars

Caidie Cheng[1,2], Keqin Liu[2] , Bingjie Dang[2] , Liying Xu[2] , Zhen Yang[2] , Xiaoqin Yan[1], Yuchao Yang[2], Ru Huang[2]; [1]University of Science and Technology Beijing, China, [2]Peking University, China

Saturday, April 10, 2021

11:30–12:30 ShuJin Hall

Session TH1A4: The Photon Challenge: No Longer Light Manufacturing

Chair: Qi Liu, Institute of Microelectronics, CAS
Co-Chair: Patrick Fay, University of Notre Dame

TH1A4-1 11:30

Silicon Nanophotonic Devices for On-chip Optical Modulation and Switching (Invited talk)

Daoxin Dai , Lijia Song ,Bingchen Pan; Zhejiang University, China

TH1A4-2 11:50

Purcell effect and lasing from quantum dots in a topological photonic crystal nanocavity (Invited talk)

Xin Xie[1,2], Weixuan Zhang[3,4], Xiaowu He[5] , Huiming Hao[5] , Haiqiao Ni[5] , Zhichuan Niu[5] , Xiangdong Zhang[3,4], Xiulai Xu[1,2,6]; [1]Institute of Physics, Chinese Academy of Sciences, China, [2]CAS Center for Excellence in Topological Quantum Computation and School of Physical Sciences, University of Chinese Academy of Sciences, China, [3]School of Physics, Beijing Institute of Technology, China, [4]School of Physics, Beijing Institute of Technology, China, [5]Institute of Semiconductors Chinese Academy of Sciences, China, [6]Songshan Lake Materials Laboratory, China

TH1A4-3 12:10

Manufacturing of State-of-The-Art InP-Based Photonic Integrated Circuits (Invited talk)

Fred Kish; NCSU/Infinera

Saturday, April 10, 2021

13:50–15:30 ShuFeng Hall

Session TH2P1: Bio-MEMS/NEMS

Chair: Xinxin Li, SIMIT-CAS
Co-Chair: Jiahao Zhao, Tsinghua University

TH2P1-1 13:50

Manipulation and Characterization of Human Cardiomyocytes for Drug Screening (Invited talk)

Yu Sun; University of Tronto, Canada

TH2P1-2 14:10

The manufacture and characterization of a novel ultrasonic transducer for medical imaging

Jian-Song Sheng[1], Yunfei Zhao[1], Yancong Qiao, Jiang Ling, Jun Fu, Yi Yang, Tian-Ling Ren; Tsinghua University, China

TH2P1-3 14:30

Shrink Polymer Micro Sensors for Detection of Water Pollutants (Invited talk)

Tianhong Cui; University of Minnesota, USA

TH2P1-4 14:50

A Flexible Electroencephalography Electronic Skin Based on Graphene

Ge Deng[1,2],Yan-cong Qiao[1] ,Ning-qin Deng[1] ,Xiao-shi Li[1] ,Qi Wu[1] ,Ying-fen Zeng[1,2], Si-fan Yang[2], Tian-Ling Ren[1]; [1]Tsinghua University, China [2]Graduate School at Shenzhen, Tsinghua University,China

TH2P1-5 15:10

Surface Modification to Improve the Electrochemical Performance of Neural Microelectrode Arrays

Shuguang Yang, Yujie Yang, Liang Geng, George Adedokum, Dongcheng Xie, Ruichen Liu, Lei Xu; University of Science and Technology of China, China

Saturday, April 10, 2021

13:50–15:30 ShuShan Hall

Session TH2P2: Photodetection and Display Technologies

Chair: Zheng Lou, University of Chinese Academy of Sciences
Co-Chair: Volker Sorger, The George Washington University

TH2P2-1 13:50

Bionic Eye with Perovskite Nanowire Array Retina (Invited talk)

Leilei Gu, Swapnadeep Poddar, Yuanjing Lin, Zhenghao Long, Daquan Zhang, Qianpeng Zhang, Lei Shu, Xiao Qiu, Matthew Kam, Zhiyong Fan; Hong Kong Univ. of Sci. and Tech, China

TH2P2-2 14:10

β-Ga_2O_3 Micro-Flake FET SBPD with Record Detectivity of 3.87×10^{17} Jones for Weak Light Detection

Shunjie Yu[1] , Mengfan Ding[1] , Wenxiang Mu[2] , Zhitai Jia[2] , Xiaohu Hou[1] , Zhongfang Zhang[1] , Pengju Tan[1] , Xiaolong Zhao[1],Guangwei Xu[1] , Shibing Long[1]; [1]University of Science and Technology of China, China; [2]Shandong University, China

TH2P2-3 14:30

Large Area and Flexible Organic Active Matrix Image Sensor Array Fabricated by Solution Coating Processes at Low Temperature

Xiao Hou[1], Wei Tang[1], Sujie Chen[1], Jianghu Liang[2], Hanyang Xu[1], Bang Ouyang[1], Ming Li[1], Yawen Song[1], Chun-chao Chen[2], Patrick Too[3], Xiaoqing Wei[4], Libo Jin[4], Gang Qi[5], Xiaojun Guo1; [1]School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University, China, [2]School of Material Science and Engineering, Shanghai Jiao Tong University, China, [3]FlexEnable, UK, [4]iRay Technology, China, [5]Tianma Microelectronics, China

TH2P2-4 14:50

A Sensitive Vertical Standing Graphene/Silicon Schottky Photodetector to Angle Changes

Ning-Qin Deng[1,4] , Zhen-Yi Ju[1], Ge Deng[1], Hou-Fang Liu[1], Xiang-Shun Geng[1] , Xiu-Feng Jia[1] , Jun Ren[1] , Tian-Zhong Yang[2] , Dan Xie[1] , Yi Yang[1] , He Tian[1], Tian-Ling Ren[1,3]; [1]Tsinghua University, China, [2]Chinese Academy of Sciences, China, [3]Center for Flexible Electronics Technology, Tsinghua University, Beijing, China, [4]National Institute of Metrology (NIM), Beijing, China

TH2P2-5 15:10

Ultra-High-Sensitivity Photodetector from Ultraviolet to Visible Based on Ga-Doped In_2O_3 Nanowire Phototransistor with Top-Gate Structure

Wenhao Ran , Zheng Lou , Guozhen Shen; University of Chinese Academy of Sciences, China

Saturday, April 10, 2021

13:50–15:30 ShuYun Hall

Session TH2P3: 2D materials and devices II

Chair: Yanqing Wu, Peking University
Co-Chair: Fengqiu Wang, Nanjing University

TH2P3-1 13:50

From the Top or Through the Edge: What is the Most Scalable Contact to 2D Semiconductors? (Invited talk)

Aaron D. Franklin; Duke University, USA

TH2P3-2 14:10

Semiconductor Nanostructures for Optoelectronic and Energy Applications (Invited talk)

Hoe Tan; Australian National University, Australia

TH2P3-3 14:30

Small-Hysteresis Flexible Carbon Nanotube Thin-Film Transistors Using Stacked Architecture

Yun Sun[1], Dong-Sheng Zhu[2],Yang Jian[3] ,Chao Zang[1], Dong-Ming Sun[1]; [1]Chinese Academy of Sciences, China, [2]Shenyang Ligong Univ., China, [3]Northeastern Univ. China

TH2P3-4 14:50

Universal Non-Volatile Resistive Switching Behavior in 2D Metal Dichalcogenides Featuring Unique Conductive-Point Random Access Memory Effect

Xiaohan Wu[1] , Ruijing Ge[1] , Yuqian Gu[1] , Emmanuel Okogbue[2] , Jianping Shi[3] , Abhay Shivayogimath[3] , Peter Bøggild[4] , Timothy J. Booth[4] , Yanfeng Zhang[3] , Yeonwoong Jung[2] , Jack C. Lee[1], Deji Akinwande[1] ; [1]University of Texas at Austin, Austin, USA, [2]University of Central Florida, USA, [3]Peking University, China, [4]Technical University of Denmark,Denmark

TH2P3-5 15:10

A Study of Materials Impacts on Graphene Electrostatic Discharge Switches

Cheng Li, Mengfu Di, Zijin Pan, Albert Wang; University of California, Riverside, USA

Saturday, April 10, 2021

13:50–15:30 ShuJin Hall

Session TH2P4: Advanced Packaging

Chair: Ke Xiao, NCAP
Co-Chair: Sarah Ying Zhong, University of South Florida

TH2P4-1 13:50

Modeling for assessing Semiconductor Packages in High-Reliability Applications (Invited talk)

Chris Bailey; University of Greenwich, UK

TH2P4-2 14:10

Fan-Out Wafer and Panel Level Packaging - A Platform for 3D Integration (Invited talk)

Tanja Braun[1] ,Karl-Friedrich Becker[1] ,Michael Töpper[1] ,Rolf Aschenbrenner[1] ,Martin Schneider-Ramelow[2]; [1]Fraunhofer IZM, Germany, [2]Technical University Berlin, Germany

TH2P4-3 14:30

Growth Behavior and Mechanism of Tin Whisker on Isolated SnAg Solder Under Compressive Stress

Shuhui Chen , Xundi Zhang , Lingyue Tan ,Anmin Hu , Huiqin Ling , Ming Li, Tao Hang; Shanghai Jiao Tong University, China

TH2P4-4 14:50

Undercooling and Microstructure Analysis for the Design of Low Melting Point Solder

Li Pu[1] , Yongjun Huo[1] , Xiuchen Zhao[1] , K. N. Tu[2] , Yingxia Liu[1]; [1] Beijing Institute of Technology, China, [2]University of California, Los Angeles, USA

TH2P4-5 15:10

An Epoxy Composite Film for Modified Semi-Addictive Process

Suibin Luo, Junyi Yu, Pengpeng Xu, Jie Liu, Shuhui Yu, Rong Sun, Yougen Hu; Chinese Academy of Sciences, China

Saturday, April 10, 2021

15:50–17:30 ShuFeng Hall

Session TH3P1: Advanced CMOS Technologies

Chair: Toshiro Hiramoto, University of Tokyo
Co-Chair: Jiezhi Chen, Shandong University

TH3P1-1 15:50

Disruptive Technology Elements, and Rapid and Accurate Block-Level Performance Evaluation for 3nm and Beyond (Invited talk)

M.H. Na[1], D. Jang[1], R. Baert[1], S. Sarkar[1], S. Patli[1], O. Zografos[1], B. Chehab[1], A. Spessot[1], G.Sisto[2], P. Schuddinck[1], H. Mertens[1], Y.Oniki[1], G. Hellings[1], E. Dentoni Litta[1], J. Ryckaert[1], N.Horiguchi[1]; [1]imec, Belgium, [2]Cadence Design System, USA

TH3P1-2 16:10

Advanced CMOS Technologies for Ultra-Low Power Logic and AI Applications (Invited talk)

Shinichi Takagi, Kasidit Toprasertpong, Kimihiko Kato, Kei Sumita , Eishin Nako , Ryosho Nakane, Kwang-won Jo, Mitsuru Takenaka; University of Tokyo, Japan

TH3P1-3 16:30

Subthreshold Swing in Silicon Gate-All-Around Nanowire MOSFET at Cryogenic Temperature

Shohei Sekiguchi, Min-Ju Ahn , Takuya Saraya , Masaharu Kobayashi, Toshiro Hiramoto; University of Tokyo, Japan

TH3P1-4 16:50

Sub-3nm Transition-Metal Dichalcogenides FETs: Theoretical Insights into the Impacts of Layer Numbers and Channel Lengths

Fei Wang, Xiaolei Ma, Wei Wei, Pengpeng Sang, Qianwen Wang, Weiqiang Zhang, Yuan Li, Jiezhi Chen; Shandong University, China

TH3P1-5 17:10

Manipulating the Electrical Characteristics of Two-Dimensional Semiconductor Transistors by Gate Engineering

Jingyi Ma[1], Ling Tong[1], Xiaojiao Guo[1], Xinyu Chen[1], Minxing Zhang[1], Chenjian Wu[2], Wenzhong Bao[1]; [1]Fudan University, China, [2]Soochow University, China

Saturday, April 10, 2021

15:50–17:30 ShuShan Hall

Session TH3P2: GaN power devices

Chair: Shibing Long, University of Science and Tecnology of China
Co-Chair: Ray Hueting, University of Twente

TH3P2-1 15:50

150 mm RF GaN Technology for Commercial RF Applications (Invited talk)

B. Green, K. Moore, S. Klingbeil, C. Rampley, P. Renaud, D. Burdeaux, D. Hill, C. Zhu, J. Wan, K. Kim, C. Gaw, T. Arnold, F. Vanaverbeke, J. Finder; NXP Semiconductors, USA

TH3P2-2 16:10

Nearly Ideal Quasi-Vertical GaN Schottky Barrier Diode with 10^{10} High On/Off Ratio and Ultralow Turn on Voltage via Post Anode Annealing

Jiabo Chen, Zhihong liu , Zhaoke Bian, haiyong Wang, Xiaoling Duan, Jing Ning, Jincheng Zhang, Yue Hao; Xidian University, China

TH3P2-3 16:30

A Novel Normally-Off Laterally Coupled p-GaN Gate HEMT

Xing Wei[1,2], Xiaodong Zhang[1,2], Chi Sun[1,2], Wenxin Tang[1,2], Tao He[2] , Xuan Zhang[2], Guohao Yu[2], Liang Song[2] , Wenkui Lin[1,2], Yong Cai[2], Baoshun Zhang[2]; [1]University of Science and Technology of China, China, 2Suzhou Institute of Nano-Tech and Nano-Bionics, China

TH3P2-4 16:50

Reverse Conduction Induced Dynamic Ron Effect in GaN HEMT with p-GaN Gate

Shaoyu Sun[1,2], Ling Xia[3], Wengang Wu[2], Yufeng Jin[1, 2]; [1]Peking University ShenZhen Graduate School, China, [2]Peking University, China, [3]Shenzhen Hai Li Technology Inc., China

TH3P2-5 17:10

3D GaN Power Switching Electronics: A Revival of Interest in ELO (Invited talk)

Jia Wang[1,2], Hiroshi Amano[2], Ya-Hong Xie[1] ; [1]University of California, Los Angeles, USA, [2]Nagoya University, Japan

Saturday, April 10, 2021

15:50–17:30 ShuYun Hall

Session TH3P3: Modeling of Ferroelectronics

Chair: Peng Huang, Peking University
Co-Chair: Rongmei Chen, IMEC

TH3P3-1 15:50

Variability Analysis for Ferroelectric Field-Effect Transistors

Gihun Choe, Shimeng Yu; Georgia Institute of Technology, USA

TH3P3-2 16:10

Revisiting the Definition of Ferroelectric Negative Capacitance Based on Gibbs Free Energy

Yuanyuan Zhang[1,2], Xueli Ma[1,2], Xiaolei Wang[1,2], Jinjuan Xiang[1,2], Wenwu Wang[1,2]; [1]Institute of Microelectronics, Chinese Academy of Sciences, China, [2]University of Chinese Academy of Sciences, China

TH3P3-3 16:30

Ferroelectric Based FETs and Synaptic Devices for Highly Energy Efficient Computational Technologies (Invited talk)

D. Esseni, R. Fontanini, D. Lizzit, M. Massarotto, F. Driussi, M. Loghi; University of Udine, Italy

TH3P3-4 16:50

On the Critical Role of Ferroelectric Thickness for Negative Capacitance Transistor Optimization

Om Prakash[1], Aniket Gupta[1,2], Girish Pahwa[3], Yogesh S. Chauhan[4], Hussam Amrouch[5]; [1]Karlsruhe Institute of Technology, Germany, [2]National Institute of Technology Uttarakhand, India, [3]University of California, Berkeley, USA, [4] Indian Institute of Technology Kanpur, India, [5] University of Stuttgart, Germany

TH3P3-5 17:10

Modelling and Design of FTJs as High Reading-Impedance Synaptic Devices

R. Fontanini, M. Massarotto, R. Specogna, F. Driussi, M. Loghi, D. Esseni ; University of Udine, Italy

Saturday, April 10, 2021

15:50–17:30 ShuJin Hall

Session TH3P4: Yield and Manufacturing

Chair: Weihai Bu, STIC
Co-Chair: Bill Nehrer, Applied Materials

TH3P4-1 15:50

On-Chip Test Acceleration for Advanced Technologies (Invited talk)

Shenzhi Yang, Fan Lan, Weiwei Pan, Ludan Yang, Yongjun Zheng; Semitronix Inc, China

TH3P4-2 16:10

Efficient Yield Analysis and Optimization with Transient Sensitivity Analysis (Invited talk)

Zuochang Ye, Tsinghua University, China

TH3P4-3 16:30

Statistical Feature Extraction and Hybrid Feature Selection for Material Removal Rate Prediction in Chemical Mechanical Planarization Process

Wenlan Jiang[1] , Chunpu Lv[1] , Bing Yang[2] , Fuquan Zhang[2] , Ying Gao[2] , Tao Zhang[1] , Huangang Wang[1]; [1]Tsinghua University, China, [2]Semiconductor Technology Innovation Center (Beijing) Crop, China

TH3P4-4 16:50

Maximizing Output from an Equipment Fleet in a Semiconductor Fab (Invited talk)

Sanjiv Mittal, Haim Albalak, Chris Keith, Willian Nehrer; Applied Materials, USA

TH3P4-5 17:10

Thermal Atomic Layer Etching of Microelectronic Materials (Invited talk)

Steven M. George; University of Colorado, USA

Sunday, April 11, 2021

9:00–10:40 ShuFeng Hall

Session FR1A1: Emerging Devices and Applications

Chair: Xiao Gong, National University of Singapore
Co-Chair: Ran Cheng, Zhejiang University

FR1A1-1 9:00

Physics and Applications of Emerging Ferroelectric Devices (Invited talk)

Masaharu Kobayashi; University of Tokyo, Japan

FR1A1-2 9:20

Dynamics Studies of Polarization Switching in Ferroelectric Hafnium Zirconium Oxide (Invited talk)

X. Lyu[1] , M. Si[1] , P. R. Shrestha[2] , K. P. Cheung[2] ,P. D. Ye[1]; [1]Purdue University, USA, [2]National Institute of Standards and Technology, Gaithersburg, USA

FR1A1-3 9:40

Top-Gate Short Channel Amorphous Indium-Gallium-Zinc-Oxide Thin Film Transistors with Sub-1.2 nm Equivalent Oxide Thickness

Kaizhen Han, Subhranu Samanta, Chen Sun, Jishen Zhang, Zijie Zheng, Xiao Gong; National University of Singapore, Singapore

FR1A1-4 10:00

Tunable Random Number Generators Implemented by Spin-Orbit Torque Driven Stochastic Switching of a Nanomagnet for Probabilistic Spin Logic

Shuai Zhang, Shihao Li, Xuecheng Zou, Jeongmin Hong, Long You; Huazhong University of Science and Technology, China

FR1A1-5 10:20

100 nm T-Gate GaN-On-Si HEMTs Fabricated with CMOS-Compatible Metallization for Microwave and mm-Wave Applications

Hanlin Xie[1,2] , Zhihong Liu[3], Yu Gao[1] , Kenneth E. Lee[1] , Geok Ing Ng[2]; [1]Singapore-MIT Alliance for Research and Technology Centre, Singapore, [2]Nanyang Technological University, Singapore , [3]Xidian University, China

Sunday, April 11, 2021

9:00–10:40 ShuShan Hall

Session FR1A2: Ga_2O_3, GaN power devices and Packaging trends

Chair: Wanjun Chen, University of Science and Tecnology of China
Co-Chair: Wai Tung Ng, University of Toronto

FR1A2-1 9:00

Ga_2O_3 Power Devices and How They Stand up to GaN and SiC (Invited talk)

Huili Grace Xing; Cornell University, USA

FR1A2-2 9:20

Channel Mobility Properties of β-Ga_2O_3 MOSFETs on Si Substrate Fabricated by Ion-Cutting Process

Yibo Wang,[1], Wenhui Xu,[2], Genquan Han,[1] Tiangui You,[2] Haodong Hu,[1] Yan Liu,[1] Hao Huang,[2] Xin Ou,[2] Xiaohua Ma,[1] Yue Hao[1]; [1]Xidian University, China, [2]Chinese Academy of Sciences, China

FR1A2-3 9:40

GaN Super-Heterojunction Schottky Barrier Diode with over 10 kV Blocking Voltage

Sang-Woo Han , Jianan Song ,Rongming Chu; Pennsylvania State University, USA

FR1A2-4 10:00

High Density Packaging Trends Driven by Miniaturization of Home Appliance

Yuquan Su, Jinqing Xu, Chi Zhang, Yasuhiro Koike; GD Midea Air-Conditioning Equipment Co., Ltd., China

FR1A2-5 10:20

Development of High-Frequency Ga_2O_3 Field-Effect Transistors (Invited talk)

Masataka Higashiwaki; NICT, Japan

Sunday, April 11, 2021

9:00–10:40 ShuYun Hall

Session FR1A3: Modeling of Transistors

Chair: Xinsheng Wang, Huazhong University of Science and Technology
Co-Chair: D. Nirmal, Karunya Institute of Technology and Sciences

FR1A3-1 9:00

L-UTSOI: Best In-Class Compact Modeling Solution for FD-SOI Technologies (Invited talk)

Thierry Poiroux[1] , Sébastien Martinie[1] , Olivier Rozeau[1] , Michael Reiha[2] , Julien Arcamone[1]; [1]MINATEC Campus, France, [2]Univ. Grenoble Alpes, France

FR1A3-2 9:20

RF Linearity of SiGe HBT: Physics, Compact Modeling Using Mextram 505 and X-Parameter Based Measurements (Invited talk)

Guofu Niu[1], Yiao Li[1], Xuewei Ding[1], Anni Zhang[1], Huaiyuan Zhang[1] Andries Scholten[2], Marnix Willemsen[2], Ralf Pijper[2], Luuk F. Tiemeijer[2]; [1]Auburn University, USA, [2]NXP Semiconductors, The Netherlands

FR1A3-3 9:40

Evaluating the Impact of STI Recess Profile Control on Advanced FinFET Device Performance

Qingpeng Wang, Yu De Chen, Rui Bao, Cheng Li, Jacky Huang, Joseph Ervin; Lam Research company, China

FR1A3-4 10:00

Multi-Physics Evaluation of Silicon Steep-Slope Cold Source FET

Weizhuo Gan[1,5], Raphaël Prentki[3] , Kun Luo[1] , Jiali Huo[1,5], Weixing Huang[1,5], Qiang Huo[1,5],Jianhui Bu[5] , Ronggen Cao[6] , Ye Lu[2] , Huaxiang Yin[1,5], Hong Guo[3] , Zhenhua Wu[1,5]; [1]Institute of Microelectronics, Chinese Academy of Sciences, China, [2]School of Information Science and Technology, Fudan University, Shanghai, China, [3]McGill University, Canada, [5]University of Chinese Academy of Sciences, China, [6]Department of materials, Fudan University, China

FR1A3-5 10:20

Enhanced On-State Current in Barrier-Free Carbon Heterojunction Tunneling Field-Effect Transistor

Yu Zhu[1], Wenli Zhou[1,2], Li Cheng[1], Qingfeng Gong[1]; [1]Huazhong University of Science and Technology, China [2]Wuhan National Laboratory of Optoelectronics, China

Sunday, April 11, 2021

9:00–10:40 ShuJin Hall

Session FR1A4: Electronic Materials

Chair: Xiaodong Pi, Zhejiang University
Co-Chair: Saptarshi Das, Pennsylvania State University

FR1A4-1 9:00

Tailoring the electromechanical coupling in stretchable inorganic thin-film electronics (Invited talk)

Yuan Lin; University of Electronic Science and Technology of China, China

FR1A4-2 9:20

Dynamics of Negative Capacitance Induced by Ferroelectric Switching in Ferroelectric-Resistor Circuit

Yulong Dong[1], Danyang Chen[1], Ni Zhong[2], Jingquan Liu[1], Chungang Duan[2], Xiuyan Li[1]; [1]Shanghai Jiao Tong University, Shanghai, China, [2]East China Normal University, China

FR1A4-3 9:40

Synaptic Plasticity in Novel Non-Volatile FET with Amorphous Gate Insulator Enabled by Oxygen Vacancy Related Dipoles

Guoqing Zhang[1] , Yue Peng[1], Wenwu Xiao[1, 2], Fenning Liu[1] , Yan Liu[1] , Genquan Han[1], Yue Hao[1]; [1]Xidian University, China, [2]Xi'an UniIC Semiconductors, China

FR1A4-4 10:00

Selecting and Optimizing Threshold Switching Materials and Devices for Stochastic Neuron

Kuan Wang, Qing Hu, Qi Lin, Dayou Zhang, Yuhui He, Hao Tong, Xiangshui Miao; Huazhong University of Science and Technology, China

FR1A4-5 10:20

High-Performance ZnO Thin-Film Transistors Prepared by Atomic Layer Deposition at Low Temperature

Qi Li, Junchen Dong, Dedong Han, Xing Zhang, Yi Wang; Peking University, China

Sunday, April 11, 2021

11:00–12:40 ShuFeng Hall

Session FR2A1: CMOS Characterization Technologies

Chair: Mitani Yuichiro, Tokyo City University
Co-Chair: Zhigang Ji, Shanghai Jiao Tong University

FR2A1-1 11:00

Low Frequency Noise: A Show Stopper for State-Of-The-Art and Future Si, Ge-Based and III-V Technologies (Invited talk)

C. Claeys[1] , A. Oliviera[2] , A. Veloso[3] , L. He[4] , K. Takakura[5] , V. Putcha[3] , H. Amimura[3] , E. Simoen[3]; [1]KU Leuven, Belgium [2]Universidade Tecnológica Federal do Paraná (UTFPR) , Brazil, [3]Imec, Belgium, [4]Xidian University, China, [5]National Institute of Technology (KOKEN), Kumamoto College, Japan

FR2A1-2 11:20

A Review of Recent MOSFET Source and Drain Resistances Extraction Methods Using a Single Test Device (Invited talk)

Adelmo Ortiz-Conde[1], Manuel A. Quevedo-Lopez[2]; [1]Universidad Simón Bolívar,Venezuela,[2]University of Texas at Dallas, USA

FR2A1-3 11:40

White Noise Characterization of N-MOSFETs for Physics-Based Cryogenic Device Modeling

K. Ohmori, S. Amakawa; Device Lab Inc., Japan

FR2A1-4 12:00

MOSFET C-V Characteristics Extraction Based on Ring Oscillator with Addressable DUTs

Zhen Zhou[1] , Junxu Wu[2] , Changfeng Wang[2] , Ganbing Shang[2] , Xiaojin Li[1] , Yabin Sun[1] , Yanling Shi[1]; [1]East China Normal University, China, [2]Shanghai Huali Microelectronics Corporation, China

FR2A1-5 12:20

Performance Trade-Offs in Complementary FET (CFET) Device Architectures for 3nm-Node and Beyond

Xiaoqiao Yang[1] , Yabin Sun[1], Ziyu Liu[2], Yanling Shi[1], Xiaojin Li[1]; [1]East China Normal University, China, [2]Fudan University, China

Sunday, April 11, 2021

11:00–12:40 ShuShan Hall

Session FR2A2: Group IV power devices

Chair: Moufu Kong, University of Electronic Science and Tecnology of China
Co-Chair: Rongming Chu, Penn State University

FR2A2-1 11:00

Phonon Properties of Group IV Materials for Thermoelectric Applications (Invited talk)

Atsushi Ogura[1, 2], Ryo Yokogawa[1, 2]; [1]School of Science and Technology, Meiji University, Japan [2]Meiji Renewable Energy Laboratory, Meiji University, Japan

FR2A2-2 11:20

Progress and Future Challenges of SiC Power MOSFETs (Invited talk)

Tsunenobu Kimoto; Kyoto University, Japan

FR2A2-3 11:40

Novel Ultralow On-Resistance Accumulation-Mode LDMOS with Integrated Diodes

Jie Wei, Zhen Ma, Congcong Li, Kaiwei Dai, Xiaorong Luo, Bo Zhang; University of Electronic Science and Technology of China, China

FR2A2-4 12:00

Process Improvement for Stabilizing the VLD Effective Dose of 4500V Trench-Gated IGBT Platform

Rui Jin[1], Li Li[1], Kui Pu[2], Jun Zeng[2,3], Longlai Xu[2] , Xiaohu Deng[4], Pan Yin[4], Yaohua Wang[1], Wenhong Zhang[2], Mohamed N. Darwish[2,3]; [1]Global Energy Interconnection Research Institute co., Ltd.,China, [2]MaxPower Semiconductor Inc., China, [3] MaxPower Semiconductor Inc., USA,[4]China Resource Microelectronics Limited, China

FR2A2-5 12:20

Accurate TCAD Simulation of Trench-Gate IGBTs and Its Application to Prediction of Carrier Lifetime Requirements for Future Scaled Devices (Invited talk)

M. Watanabe[1] , N. Shigyo[1] , T. Hoshii[1] , K. Furukawa[1] , K. Kakushima[1] , K. Satoh[2] , T. Matsudai[3] , T. Saraya[4] , T. Takakura[4] , I. Muneta[1] , H. Wakabayashi[1] , A. Nakajima[5] , S. Nishizawa[6] , K. Tsutsui[1] , T. Hiramoto[4] , H. Ohashi[1] , H. Iwai1; [1]Tokyo Institute of Technology, Japan, [2]Mitsubishi Electric Corp., Japan, [3]Toshiba Electronic Devices & Storage Corp., Japan, [4]University of Tokyo, Japan, [5]Nat. Inst. Advanced Industrial Science and Technology, Japan,[6]Kyushu University, Japan

Sunday, April 11, 2021

11:00–12:40 ShuYun Hall

Session FR2A3: Modeling of Memory, Quantum, and TFT

Chair: Lang Zeng, Beihang University
Co-Chair: Lining Zhang, Peking University Shenzhen Graduate School

FR2A3-1 11:00

A Compact Model of Analog RRAM Considering Temperature Coefficient for Neural Network Evaluation

Minghong Xu[1], Bin Gao[1], Feng Xu[1], Wei Wu[1], Jianshi Tang[1], Jiezhi Chen[2], He Qian[1]; [1]Tsinghua University, China, [2]Shandong University, China

FR2A3-2 11:20

Development of Integrated Device Simulator for Quantum Bit Design: Self-Consistent Calculation for Quantum Transport and Qubit Operation

Hidehiro Asai, Shota Iizuka, Tsutomu Ikegami, Junichi Hattori, Koichi Fukuda, Hiroshi Oka, Kimihiko Kato, Hiroyuki Ota, Takahiro Mori; National Institute of Advanced Industrial Science and Technology (AIST), Japan

FR2A3-3 11:40

Designing EDA-Compatible Cryogenic CMOS Platform for Quantum Computing Applications

Zewei Wang[1] , Chengwei Cao[2] , Puqing Yang[1,3], Yumeng Yuan[1] , Zhidong Tang[1] , Renhe Chen[1] , Weican Wu[2] , Xin Luo[2] , Ao Guo[2] , Liujiang Yu[4] , Ganbing Shang[4] , Zhaofeng Zhang[3] , Shaojian Hu[2] , Xufeng Kou[1]; [1]ShanghaiTech University, China, [2]Shanghai IC Research and Development Center, China, [3]Chinese Academy of Sciences, China, [4]Huali Microelectronics Corporation (HLMC), China

FR2A3-4 12:00

Compact Modeling of Organic and IGZO TFTs from 150K to 350K (Invited talk)

Benjamin Iñiguez[1] , Harold Cortés-Ordóñez[1] , Gérard Ghibaudo[2] , Antonio Cerdeira[3] , Magali Estrada[3] ; [1]University Rovira i Virgili, Spain, [2]MINATEC/INPG ,France, [3]CINVESTAV, Mexico

FR2A3-5 12:20

Compact Physics-Based Charge Core Model for CAAC In-Ga-Zn Oxide Multi-Gate FETs

Slobodan Mijalkovic[1], Bogdan Tudor[1], Makoto Watanabe[1], Hitoshi Kunitake[2], Takayuki Ikeda[2], Shunpei Yamazaki[2]; [1]Silvaco, Inc., USA, [2]Semiconductor Energy Laboratory Co., Japan

Sunday, April 11, 2021

11:00–12:40 ShuJin Hall

Session FR2A4: RF reliability and Power electronics reliability

Chair: Xing Wu, East China Normal University
Co-Chair: Yuhao Zhang, Virginia Tech

FR2A4-1 11:00

RF Silicon Technologies and Its Reliability for Sub-6GHz and mmWave 5G Applications (Invited talk)

P. Srinivasan; GLOBALFOUNDRIES Inc., USA

FR2A4-2 11:20

Re-Consideration of Influence of Fluorine on SiO_2 and Si_xN_y Reliabilities (Invited talk)

Yuichiro Mitani; Tokyo City University, Japan

FR2A4-3 11:40

ESD Co-Design of mm-Wave RF Switch in 22nm SOI

Feilong Zhang, Cheng Li, Mengfu Di, Zijin Pan, Han Wang, Albert Wang; University of California, Riverside, USA

FR2A4-4 12:00

Experimental Understanding of the Impact of Channel Percolation on Low Frequency Noise Using Transient Enhanced Diffusion of Channel Dopants

Shuntaro Fujii, Soichi Morita, Tsutomu Miyazaki; Asahi Kasei Microsystems, Japan

FR2A4-5 12:20

Design for Reliability based on Customer Obsession (Invited talk)

Owen Liu; Amazon Corp., Product Integrity, China

Sunday, April 11, 2021

14:00–15:40 ShuFeng Hall

Session FR3P1: Advanced Process Technology I

Chair: Ming Li, Peking University
Co-Chair: Anne Vandooren, IMEC

FR3P1-1 14:00

Nanosheet FETs and Their Potential for Enabling Continued Moore's Law Scaling (Invited talk)

A. Veloso, G. Eneman, A. De Keersgieter, D. Jang, H. Mertens, P. Matagne, E. Dentoni Litta, J. Ryckaert, N. Horiguchi; Imec, Belgium

FR3P1-2 14:20

Technology Trends in 2.5D/3D Packaging and Heterogeneous Integration (Invited talk)

Masaya Kawano ; Institute of Microelectronics, A*STAR, Singapore

FR3P1-3 14:40

Optimization of Contact W Related Processes for 28/22 nm HKMG Technology Node

Hai-Jin Lu, Zong-Yan Pan, Pei-Yu Chen, Zhi-Cheng Zhang, Ming-Zhi Chen; Shanghai Huali Microelectronics Corporation, China

FR3P1-4 15:00

Formation Mechanism of a Rounded SiGe-Etch-Front in an Isotropic Dry SiGe Etch Process for Gate-All-Around (GAA)-FETs

Yu Zhao, Taku Iwase, Makoto Satake, Hirotaka Hamamura; Hitachi, Ltd., Japan

FR3P1-5 15:20

Optimization of Bump Defect at High-Concentration In-Situ Phosphorus Doped Polysilicon/TEOS Oxide Interface for 3D NAND Flash Memory Application

Dongxue Zhao[1,2,3], Zhiliang Xia[1,2,3], Linchun Wu[3] , Tao Yang[1,2,3], Dongyu Fan[1,2,3], Yuancheng Yang[3] , Lei Liu[3] , Wenxi Zhou[3] , Zongliang Huo[1,2,3]; [1]Institute of Microelectronics of the Chinese Academy of Sciences, China, [2]University of Chinese Academy of Sciences, China, [3]Yangtze Memory Technologies Company, Ltd., China

Sunday, April 11, 2021

14:00–15:40 ShuShan Hall

Session FR3P2: Materials and Designs for Wearable Sensing

Chair: Feng Yan, The Hong Kong Polytechnic University
Co-Chair: Wentao Xu, Nankai University

FR3P2-114:00

Flexible and Wearable Sensing Electronics (Invited talk)

Ting Zhang; Suzhou Institute of Nano-Tech and Nano-Bionics, China

FR3P2-2 14:20

Emerging Designs for Polymer-Based Optoelectronics and Energy Storage (Invited talk)

Tse Nga Ng; University of Califonria San Diego, USA

FR3P2-3 14:40

Highly Stable Fibrous Solid-State Ag/AgCl Reference Electrode

Chaochao Shen, Xin Xi, Wei Tang, Xiaojun Guo, Ruili Liu; Shanghai Jiao Tong University, China

FR3P2-4 15:00

Fabrication of Highly Sensitive Flexible Tactile Sensor with Hierarchical Microstructures for Wearable Electronics

Qifeng Du[1], Ying Chen[1,2], Zhijian Wang[1], Jun Ai[1], Baicheng Zhang[1], Lanlan Liu[1], Xue Feng[3]; [1]Institute of Flexible Electronics Technology of THU, China. [2]Qiantang Science and Technology Innovation Center, China,[3]Tsinghua University, China

FR3P2-5 15:20

Printed Stretchable Multifunctional E-Textile for Wearable Electronics

Bin Tian, Wei Wu; Wuhan University, China

Sunday, April 11, 2021

14:00–15:40 ShuYun Hall

Session FR3P3: Neural network circuits and systems

Chair: Yuchao Yang, Peking University
Co-Chair: Xiaojian Zhu, Chinese Academy of Sciences

FR3P3-1 14:00

Implementation, Operation and Applications of Memristive Neural Networks (Invited talk)

Qiangfei Xia; University of Massachusetts, USA

FR3P3-2 14:20

In-memory computing with memristor content addressable memory circuits (Invited talk)

Catherine Graves; HP Labs, USA

FR3P3-3 14:40

A Neural Network-Based Harmonic Suppression Algorithm for Medium-To-High Resolution ADCs (Invited talk)

Xizhu Peng[1] , Yihang Mi[1] , Yunfan Zhang[1] , Yao Xiao[1] , Wei Zhang[1] , Yong Tang[1] , He Tang[1,2]; [1] University of Electronic Science and Technology of China, China, [2]Guangdong Institute of electronic information engineering, University of Electronic Science and Technology of China, China

FR3P3-4 15:00

Artificial Neuron with Spike Frequency Adaptation Based on Mott Memristor

Qiumeng Wei[1], Jianshi Tang[1,2], Xinyi Li[1], Yanan Zhong[1], Bin Gao[1,2], He Qian[1,2], Huaqiang Wu[1,2]; [1]Institute of Microelectronics, Tsinghua University, China, [2]Beijing Innovation Center for Future Chips (ICFC), Tsinghua University, China

FR3P3-5 15:20

Associative Learning Circuit Based on Synaptic Transistors with Temporal Dynamics

Chang Liu, Zhaokun Jing, Yuchao Yang, Ru Huang; Peking University, China

Sunday, April 11, 2021

14:00–15:40 ShuJin Hall

Session FR3P4: Applications for Machine Learning in Semiconductor Manufacturing

Chair: Tang He, University of Electronic Science & Technology of China
Co-Chair: Shuji Ikeda, tei Solutions Inc

FR3P4-1 14:00

Applications of AI Technologies in Flash Memory Business (Invited talk)

Ryohei Orihara; Digital Process Innovation Center Kioxia Corporation, Japan

FR3P4-2 14:20

Applications for Machine Learning in Semiconductor Manufacturing and Test (Invited talk)

Chen He[1] , Hanbin Hu[2] , Peng Li[2]; [1]NXP Semiconductors, Austin, USA, [2]University of California at Santa Barbara, USA

FR3P4-3 14:40

Machine Learning Approaches Optimizing Semiconductor Manufacturing Processes (Invited talk)

Tsuyoshi Moriya; Tokyo Electron Limited, Japan

FR3P4-4 15:00

Applications for Machine Learning in Semiconductor Manufacturing (Invited talk)

Richard Burch, Luke Merrick, Qing Zhu, Tomonori Honda, Jeff David; PDF Solutions, USA

FR3P4-5 15:20

Improving accuracy and cycle-time in computational lithography with Machine Learning (Invited talk)

Shibing Wang; ASML, Netherlands

Sunday, April 11, 2021

16:00–17:40 ShuFeng Hall

Session FR4P1: Advanced Process Technology II

Chair: Xiaojian Zhu, Chinese Academy of Sciences
Co-Chair: Bich-Yen Nguyen, SOITEC

FR4P1-1 16:00

Sputtering Growth of Metal Oxynitride Semiconductors for Excitonic Devices (Invited talk)

Ryota Narishige, Naho Itagaki, Masaharu Shiratani; Kyushu Univ., Japan

FR4P1-2 16:20

Growth of Ferroic Metal Oxide Films with Desired Properties by Polymer-Assisted Deposition (Invited talk)

Samyak Dhole, Quanxi Jia; University at Buffalo – The State University of New York, USA

FR4P1-3 16:40

Effect of Low Temperature Annealing on PN Junction Formation Using Si Paste

Huan Zhu[1], Yusuke Kuboki[1], Morihiro Sakamoto[1], Yoshimine Kato[2]; [1]Department of Automotive Science, Kyushu University, Japan, [2]Faculty of Engineering, Kyushu University, Japan

FR4P1-4 17:00

Optimization of Tilted Profile in Ultra-High Aspect Ratio Etch Process for 3D NAND Flash Memory

Jinqing He[1,2,3], Zhiliang Xia[1,2,3], Meng Wang[3], Guangxuan Zhang[3] , Haiqing Dou[3] , Zongliang Huo[1,2,3]; [1] University of Chinese Academy of Sciences, China, [2]Institute of Microelectronics of the Chinese Academy of Sciences, China,[3]Yangtze Memory Technologies Company, Ltd.,China

FR4P1-5 17:20

Forming Low-Resistivity Tungsten Contacts and Avoiding Fluorine Diffusion by Flash Lamp Annealing (FLA)

Shogo Shigemasu, Hideaki Tanimura, Hikaru Kawarazaki, Shinichi Kato; SCREEN Semiconductor Solutions Co. Ltd., Japan

Sunday, April 11, 2021

16:00–17:40 ShuShan Hall

Session FR4P2: Flexible and Stretchable Systems

Chair: Jie Zhang, Jiangnan University
Co-Chair: Inhee Lee, Unversity of Pittsburgh

FR4P2-1 16:00

Artificial synapses and sensorimotor nerves (Invited talk)

Wentao Xu; Nankai University, China

FR4P2-2 16:20

Rubbery electronics and integrated systems (Invited talk)

Cunjiang Yu; University of Houston, USA

FR4P2-3 16:40

Printed conformable electronics for body-worn sensors and systems (Invited talk)

Matti Mäntysalo; Tampere University, Finland

FR4P2-4 17:00

FMM Free Organic and Hybrid Electronics Manufacturing Enabled by Photolithography (Invited talk)

Tung-Huei Ke[1], Calvin Mona Sandehang[1,2], Chi-Ting Tsai[1,3], Gema Molina Alvarez[1] , Erwin Vandenplas[1] , Paul Heremans[1,2], Pawel E. Malinowski[1]; [1]imec, Belgium, [2]KU Leuven., Belgium, [3]National Cheng Kung Univ., Belgium

FR4P2-5 17:20

Semi-Disposable Self-Adhesive Sensor System for Wearable Electrocardiogram Detection

Fangran Bian, Sujie Chen, Ming Li, Yishen Pei, Xiaojun Guo; Shanghai Jiao Tong University, China

Sunday, April 11, 2021

16:00–17:40 ShuYun Hall

Session FR4P3: Neuromorphic and quantum computing

Chair: Dmitri Strukov, UC Santa Barbara
Co-Chair: Xi-Zhu Peng, University of Electronic Science and Technology

FR4P3-1 16:00

Wafer-scale integration of 2D materials in high-density memristive crossbar arrays for artificial neural networks (Invited talk)

Mario Lanza; King Abdullah University of Science and Technology, SAU

FR4P3-2 16:20

Metal-oxide memristors for Sensory applications (Invited talk)

Themis Prodromakis, University of Southampton, UK

FR4P3-3 16:40

Ge/Si Quantum Wires for Quantum Computing (Invited talk)

Fei Gao[1] , Jie-Yin Zhang[1] , Jian-Huan Wang[1] , Ming Ming[1] , Ting Wang[1] , Jian-Jun Zhang[1] , Hannes Watzinger[2] , Josip Kukučka[2] , Lada Vukušić[2] , Georgios Katsaros[2] , Ke Wang[3] , Gang Xu[3] , Hai-Ou Li[3] , Guo-Ping Guo[3]; [1]Institute of Physics, Chinese Academy of Sciences, China, [2]Institute of Science and Technology,Austria, [3]University of Science and Technology of China, China

FR4P3-4 17:00

Convertible Volatile and Non-Volatile Resistive Switching in a Self-Rectifying Pt/TiO_x/Ti Memristor

Zuheng Wu[1,2], Xumeng Zhang[1,2,4], Tuo Shi[1,2,3], Yongzhou Wang[1], Rui Wang[1,2], Jian Lu[1], Jinsong Wei[1], Peiwen Zhang[1] , Qi Liu[1,2,3,4]; [1]Institute of Microelectronics of Chinese Academy of Sciences, China; [2]University of Chinese Academy of Sciences, China; [3]Zhejiang Laboratory, China. [4]Fudan University, China

FR4P3-5 17:20

Brain-Like Networks in Random Memristor Array Based on FORCE Training

Xumeng Zhang[1], Zuheng Wu[2], Rui Wang[2], Jian Lu[2], Jinsong Wei[2], Qi Liu[1], Ming Liu[1,2]; [1]Fudan University, China, [2]Institute of Microelectronics of Chinese Academy of Sciences, China

Sunday, April 11, 2021

16:00–17:40 ShuJin Hall

Session FR4P4: Novel Materials and Devices: Challenges and Opportunities in Semiconductor Manufacturing

Chair: Qi Liu, Fudan University
Co-Chair: John Dallesasse, University of Illinois at Urbana-Champaign

FR4P4-1 16:00

Integration of Resistive Switching Memory on Advanced Technology Nodes (Invited talk)

Xiaoxin Xu; Institute of Microelectronics, CAS, China

FR4P4-2 16:20

Manufacture and Characterization of Ultrathin Flexible Chips (Invited talk)

Kunwei Zheng[1] , Shisheng Ca[i1] , Ying Chen[2, 3], Yinji Ma[1] , Xue Feng[1]; [1]Tsinghua University, China,[2]Institute of Flexible Electronics Technology of THU, China, [3]Qiantang Science and Technology Innovation Center, China

FR4P4-3 16:40

Unified Compact Modeling of Charge Trapping in 1/f Noise, RTN and BTI (Invited talk)

Gilson Wirth[1] , Mauricio B. da Silva[2] , Thiago H. Both[3]; [1]Electrical Eng. Dept., UFRGS, Brazil, [2]UFSM, Dept. of Electronics and Comp., Brazil, [3]UFPel, Centro de Engenharias, Brazil

FR4P4-4 17:00

Engineered substrate as a fast track to technology performance (Invited talk)

Christophe Maleville; Soitec, France

FR4P4-5 17:20

Thermoelectric and Photoelectric Effects of 2D Bismuth for Flexible Electronics

Zhengrui Zhu[1,2], Siyao Jiang[1], Wen Zhong[1], Zhaoying Dang[1], Jiayi Chen[1], Beibei Zhu[1], Li Tao[1,2]; [1]School of Materials Science and Engineering, Jiangsu Key Laboratory of Advanced Metallic Materials, [2]Center for 2D Materials, Southeast University, Nanjing, China

Friday, April 9, 2021

&

Saturday, April 10, 2021

18:30–20:30 WTHPE: Interactive Forum

Chair: Jianshi Tang, Tsinghua University
Co-Chair: Yi Li, Huazhong University of Science and Technology

WTHPE-001

Evaluation of $MoS_{2(1-x)}Te_{2x}$ fabricated by different bottom-up methods

Yusuke Hibino[1,2], Kota Yamazaki[1], Yusuke Hashimoto[1], Naomi Sawamoto[3], Hideaki Machida[4], Masato Ishikawa[4], Hiroshi Sudoh[4], Hitoshi Wakabayashi[4], Atsushi Ogura[1,3]; [1]Meiji University, Japan,[2]JSPS Research Fellow, [3]MREL, Japan ,[4]Gas Phase Growth Ltd., Japan, [5]Tokyo Tech, Japan

WTHPE-003

Uniform CoPt permanent magnetic film with high in-plane coercivity

Zhi Li[1,2], Kun Zhang[1,2], Weibin Chen[1,3], Zitong Zhou[1,2], Zhiqiang Cao[1,2], Shaohua Yan[1,2], Weisheng Zhao[1,2], Qunwen Leng[1,2,4]; [1]School of Integrated Circuit Science and Engineering, Beihang University, China [2]Qingdao Research Institute, Beihang University, China, [3]Shandong University, China, [4]Goertek Inc., China

WTHPE-004

Opto-electric resistive switching and synaptic emulation in lead-free perovskite film

Swapnadeep Poddar, Yuting Zhang, Yiyi Zhu, Qianpeng Zhang, Zhiyong Fan; Hong Kong Univ. of Sci. and Tech, Hong Kong SAR, China

WTHPE-005

Fabrication and characterization of $Al_{0.8}Sc_{0.2}N$ piezoelectric thin films

Wenkui Lin [1,2], Wei Cheng [2], Yiqun Wang [2], Yuhua Sun [2], Qiang Zha [2], Chunhong Zeng [2], Qi Cui [2], Baoshun Zhang [2]; [1]Univ. of Sci. and Tech. of China, China, [2]Suzhou Institute of Nano-Tech and Nano-Bionics, CAS, China

WTHPE-006

Investigation into Electrical Conductivity and Electromagnetic Interference Shielding Performance of Ag/TPU Hybrids Filled with Various Silver Fillers

Haorui Zhang[1, 2], Zhiqiang Lin[1], Tao Zhao[1], Pengli Zhu[1], Yougen Hu[1], Rong Sun[1]; [1]Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, China, [2]Shenzhen College of Advanced Technology, University of Chinese Academy of Sciences, China

WTHPE-007

Seed layer dependent bottom pinned magnetic tunnel junctions

Weibin Chen[1,2], Shaohua Yan[2,3], Yaodi Yang[2] , Zhiqiang Cao[2,3], Yixuan Lin[1] Zitong Zhou[2,3], Shishen Yan[1], Qunwen leng[2,3,4]; [1]Shandong University, China,[2]Qingdao Research Institute, Beihang University, China, [3]School of Integrated Circuit Science and Engineering, Beihang University, China, [4]Goertek Inc, China

WTHPE-008

Achieving A Low Contact Resistivity of 0.11 Ω·mm for Ti_5Al_1 /TiN S/D Contact on $Al_{0.2}Ga_{0.8}N$/AlN/GaN Structure without Barrier Recess

Yang Jiang[1] , Zepeng Qiao[1] , Fangzhou Du[1] , Gaiying Yang[5] , Mengya Fan[1] , Xinyi Tang[1] , Qing Wang[1,2,6] , Hongyu Yu[1,2,3,4]; [1]Southern University of Science and Technology,China, [2]Shenzhen Institute of the Wide-bandgap Semiconductors, China,[3]GaN Device Engineering Technology Research Center of Guangdong,China, [4]Engineering Research Center of Integrated Circuits for Next-Generation Communications (Ministry of Education),China, [5]Southern University of Science and Technology, China, [6]Dongguan Institute of Opto-Electronics Peking University , China

WTHPE-009

Fabrication of E-mode all-GaN devices with self-terminated and self-alignment process

Meihua Liu, Yufeng Jin; Peking University Shenzhen Graduate School, China

WTHPE-010

Research of etching process of $Al_{0.8}Sc_{0.2}N$ based on ICP etching equipment

Xiaoyi Wang[1,2], Wenkui Lin[2,3], Xiaofan Yun[2,4], Qiang Zha[2], Haiou Li[1], Baoshun Zhang[2]; [1]Guilin University of Electronic Technology, China, [2]Suzhou Institute of Nano-Tech and NanoBionics, CAS, China,[3]Univ. of Sci. and Tech. of China, China, [4]Nanjing University of Science and Technology, China

WTHPE-011

Growth Optimization of Low-Pressure Chemical Vapor Deposition Silicon Nitride Film

Wen Lei[1], Maojun Wang[2], Xinnan Lin[1], Meihua Liu[1], Jiansheng Luo[1], Yufeng Jin[1]; [1]Peking University Shenzhen Graduate School, China, [2]Peking University, China

WTHPE-012

Development of HSQ replacement gate process for silicon nanowire MOS devices

Kun Tu[1,2], Xiaoqiao Dong[2], Baotong Zhang[2], Ru Huang[2], Ming Li[2], Peimin Lu[1]; [1]Fuzhou University, China, [2]Peking University, China

WTHPE-013

Atomic Layer Deposition Deposited Al-Doped ZnO Films for Transistor Application

Junchen Dong, Qi Li, Dedong Han, Yi Wang, Xing Zhang; Peking University, China

WTHPE-014

A RF Integrated Transformer with Fe_3O_4 Nanoparticles Film

Shifeng Li[1], Kewen Zhu[1], Lijun Ma[1], Bang Wu[1], Wanghui Zou[2], Feng Liu[1]; [1]Wuhan University, China, [2]Changsha University of Science and Technology, China

WTHPE-015

Persistent Spin Helix-based Spin Field Effect Transistor

Zhizhong Chen, Jian Shi; Rensselaer Polytechnic Institute, USA

WTHPE-016

Performance Evaluation of Negative Capacitance Reconfigurable Field Effect Transistor for Sub 10 nm Integration

Zihan Sun[1], Xianglong Li[1], Yabin Sun[1], Ziyu Liu[2], Yanling Shi[1] Xiaojin Li[1]; [1]East China Normal University, China, [2]Fudan University, China

WTHPE-017

Role of Interfacial Traps at SiO_2/Si Interface in Negative Capacitance Field Effect Transistor (NCFET) Based on Transient Negative Capacitance (NC) Theory

Xiaoqing Sun[1,2], Yuanyuan Zhang[1,2], Jinjuan Xiang[1,2], Kai Han[3], Xiaolei Wang[1,2],Wenwu Wang[1,2]; [1]Institute of Microelectronics, Chinese Academy of Sciences,China, [2]University of Chinese Academy of Sciences, China; [3]Weifang University , China

WTHPE-018

WS_2 pMISFETs by Sputtering and Sulfur-Vapor Annealing with TiN/HfO_2-Top-Gate-Stack, TiN Contact and Ultra-Thin Body and Box

Takuya Hamada, Masaya Hamada, Satoshi Igarashi, Taiga Horiguchi, Iriya Muneta, Kuniyuki Kakushima, Kazuo Tsutsui, Tetsuya Tatsumi, Shigetaka Tomiya; Hitoshi Wakabayashi Tokyo Institute of Technology, Japan

WTHPE-019

Self-started Piezoelectric Energy Conditioning System based on Electrostatic Driving MEMS Switch

Jiahao Zhao[1,2], Yingying Li[2], Yiguo Chen[2]; [1]Beijing Innovation Center for Future Chips, China,[2]Department of Precision Instrument, Tsinghua University, China

WTHPE-020

Evaluation of an Effective DC Solid State Circuit Breaker Based on CS-MCT

Yuxiao Yang, Wanjun Chen, Hongyang Zhang, Xiaorui Xu, Bo Zhang; University of Electronic Science and Technology of China (UESTC), China

WTHPE-021

High Performance β-Ga_2O_3 Vertical Rectifier With Double Step Structure Termination Using Thermally Oxided TiO_x Dielectrics

Zhaofeng Sun, Yuangang Wang, Yuanjie Lv, Shaobo Dun, Hongyu Liu, Zhihong Feng; Hebei Semiconductor Research Institute, China

WTHPE-022

Reducing Reverse Leakage Current of AlGaN/GaN heterostructures Using Low-fluence Neutron Irradiation

Rong Wang[1,2]; [1]ZJU-Hangzhou Global Scientific and Technological Innovation Center, China, [2]Zhejiang University, China

WTHPE-023

Self-Reactive Etching of β-Ga_2O_3 for Fabricating Trench Schottky Barrier Diodes

Wenbo Tang[1,2], Xiaodong Zhang[1,2], Tao He [2], Yongjian Ma [1,2], Xing Wei[1,2], Yong Cai[2], Gaohang He[3], Sunan Ding[3], Baoshun Zhang[2]; [1]University of Science and Technology of China, [2]Suzhou Institute of Nano-Tech and NanoBionics, China, [3]Suzhou Institute of Nano-Tech and Nano-Bionics, China

WTHPE-024

Study of bilayer Al_2O_3/in-situ SiNx dielectric stacks for gate modulation in ultrathin-barrier AlGaN/GaN MIS-HEMTs

Jiaqi He[1,2], Wei-Chih Cheng[1,4], Yang Jiang[1] , Qing Wang[1,3,5], Hongyu Yu[1,3], [1] Southern University of Science and Technology, China, [2]The Hong Kong Polytechnic University, China,[3]Engineering Research Center of Integrated Circuits for Next-Generation Communications, Ministry of Education, China,[4]The Hong Kong University of Science and Technology, China, [5]Dongguan Institute of Opto-Electronics Peking University,China

WTHPE-025

Fabrication on n-Ga_2O_3/p-GaN diode by wet-etching lift-off and transfer-print

Yang Liu[1], Lai Wang[1], Yuantao Zhang[2], Xin Dong[2], Zhibiao Hao[1], Yi Luo[1], Changzheng Sun[1], Yanjun Han[1], Bing Xiong[1], Jian Wang[1], Hongtao Li[1]; [1]Tsinghua University, Beijing, China,[2]Jilin University, China

WTHPE-026

A DC-DC converter utilizing β-Ga_2O_3 Schottky barrier diode

Wei Guo[1], Guangzhong Jian[2], Feihong Wu[1], Kai Zhou[1], Guangwei Xu[1], Xuanze Zhou[1], Qiming He[2], Xiaolong Zhao[1], Shibing Long[1]; [1]University of Science and Technology of China, China, [2]Institute of Microelectronics of Chinese Academy of Sciences, China

WTHPE-027

A High Voltage Superjunction MOSFET with Enhanced Reverse Recovery Performance

Yun Xia, Wanjun Chen, Ruize Sun , Chao Liu, Zhaoji Li, Bo Zhang; University of Electronic Science and Technology of China, China

WTHPE-028

A Dual Hole Barriers IGBT with High dV/dt Controllability and Extreme Low EMI Noise

Shuyi Zhang[1], Wanjun Chen[1, 2], Xiaorui Xu[1], Chao Liu[1], Nan Chen[1], Qi Zhou[1], Bo Zhang[1]; [1]University of Electronic Science and Technology of China (UESTC), China; [2]Institute of Electronic and Information Engineering of UESTC in Guangdong, China

WTHPE-029

Vertical Field-Plated NiO/Ga_2O_3 Heterojunction Power Diodes

Hehe Gong[1], Xinxin Yu[1,2], Yang Xu[1], Jianjun Zhou[2], Fangfang Ren[1], Shulin Gu[1], Rong Zhang[1], Jiandong Ye[1]; [1]Nanjing University, China, [2]Nanjing Electronic Devices Institute, China

WTHPE-030

A Fully Integrated CMOS Power Amplifier with a 133% Relative Bandwidth upon Multilayer Inductors

Daming Ren[1], Yiwei Zou[1], Wei Zou[2], Xuecheng Zou[1]; [1]Huazhong University of Science and Technology,China, [2]Hubei University of Technology, China

WTHPE-031

Physics-based parameter extraction methodology for channel doping gradient (CDG) LDMOS transistors based on HiSIM-HV2 model

Shubham Patil, Kumari Neeraj Kaushal, Mandar S. Bhoir, Nihar R. Mohapatra; Electrical Engineering, IIT Gandhinagar, Gandhinagar, India

WTHPE-032

A Compact Model for Relaxation Effect in Analog RRAM for Computation-in-Memory System Design and Benchmark

Yuyi Liu, Bin Gao, Feng Xu, Wenqiang Zhang, Yue Xi, Jianshi Tang, He Qian; Tsinghua University, China

WTHPE-033

Analytical Modelling of Ferroelectricity Instigated Enhanced Electrostatic Control in Short-Channel FinFETs

Jhang-Yan Ciou[1], Sourav De[1], Chien-Wei-Wang[1], Wallace Lin[1], Yao-Jen Lee[2], Darsen Lu[1]; [1]National Cheng Kung University, Taiwan; [2]Taiwan Semiconductor Research Institute, Taiwan.

WTHPE-036

Magnetic and electronic properties of Mn doped Sr/Si(111)-(3 × 2) HCC surface

Jun Shuai Chai, Yuan Yuan Zhang, Xiao Lei Wang, Hao Xu, Jin Juan Xiang, Wen Wu Wang; Chinese Academy of Sciences, China

WTHPE-037

Junctionless Omega-Gate MOSFET: A Short-channel Subthreshold Model and Its Evaluation of Noise Margin for Subthreshold Logic Gate

Te-Kuang Chiang, Shen Wei-Cheng, Jiang Yu-Yu; National University of Kaohsiung, Taiwan

WTHPE-038

Modelling of multiple-channel influence on GaN based HEMTs

Xing Chen[1], Dandan Lv[2], Jinfeng Zhang[2], Hong Zhou[2], Zeyang Ren[2], Chong Wang[2], Yong Wu[1], Dong Wang[1], Yingyi Lei[3], Wenxiu Zeng[1], Hong Zhang[2], Jincheng Zhang[2], Yue Hao[2]; [1]Xidian-Wuhu Research Institute, China, [2]Xidian University, China, [3]Xi'an Microelectronic Technology Institute, China

WTHPE-039

A first-principles study of the interface property in oxide-based RRAM

Nianduan Lu[1], Shang Ma[12], Jiezhi Chen[3], Qian Zhou[2], Ling Li[1], Ming Liu[1]; [1]Institute of Microelectronics of Chinese Academy of Sciences, China,[2] Beihang Univ., China, [3]Shandong Univ., China

WTHPE-040

Ag/HfO_2-based Threshold Switching Memristor as an Oscillatory Neuron

Qilin Hua[1], Chunsheng Jiang[2], Weiguo Hu[1]; [1]Chinese Academy of Sciences, China, [2]Chinese Academy of Engineering Physics, China

WTHPE-041

A New Multi-Stimuli-Based Simulation Method for ESD Design Verification

Mengfu Di, Zijin Pan, Cheng Li, Albert Wang; University of California, Riverside, USA

WTHPE-042

Measurements and Simulation of Self-Heating in 40 nm SOI MOSFETs

Xiong Zhang, Payam Mehr, Dragica Vasileska, Trevor Thornton; Arizona State University, USA

WTHPE-043

Study on the theory and model of overcut effect of focused ion beam sputtering etching process

Han Tian, Xing Yan; Southeast University, China

WTHPE-044

2D Structural Variation Impact on Electrostatic Performance of Sub-5nm Nanosheet Transistors Subject to Strong Quantum Confinement

Haowen Luo, Xingsheng Wang, Xiangshui Miao; Huazhong University of Science and Technology, China

WTHPE-045

Effect of Screening and Depolarization in Cylindrical Ferroelectric Capacitor

Mengqi Fan, Pengying Chang, Gang Du, Jinfeng Kang, Xiaoyan Liu; Peking University, China

WTHPE-046

Oxygen Vacancy Formation Accompanied by Hf Oligomer in Amorphous-HfO_x-Based RRAM: a First Principles Study

Siyao Yang[1], Bin Gao[1], Feng Xu[1], Qi Hu[1], Jianshi Tang[1], Jiezhi Chen[2], He Qian[1]; [1]Tsinghua University, China; [2]Shandong University, China

WTHPE-047

A Memristor-Based Neural Network Design for Associative Learning

Siqi Wang, Boyi Dong, Yaoyao Fu, Yuhui He, Xiangshui Miao; Huazhong University of Science and Technology, China

WTHPE-048

A Non-Resonant Recessed Gate AlGaN/GaN HEMT Terahertz Detector

Shasha Bai，BaoqingLiu，Kang Li，Linan Yang; Xidian University, China

WTHPE-050

Sudoku DTSCR ESD Array in 22nm FDSOI

Cheng Li, Feilong Zhang, Zijin Pan, Mengfu Di, Chenkun Wang, Albert Wang; University of California, Riverside, USA

WTHPE-051

HTRB & THB Reliability Improvement Using Capping Layer in Power Discrete Trench Devices

David Goh, W. J. Chen, F. Tahir, Shin Phay Lee, V. C. Ngwan; STMicroelectronics Pte Ltd, Singapore

WTHPE-052

Study of Anomalous Hot-Carrier Degradation of NMOS Transistor with 3D-NAND Hydrogen-Rich Process

Chao Sun, Wu Tian, JianPing Wang, Wenshan Xu, Can Zhong, Guangyuan Liu, Changlong Hu, Ning Jiang, Lei Xue; Yangtze Memory Technologies Co.Ltd, China

WTHPE-053

Soft Errors in Negative Capacitance FDSOI SRAMs

Govind Bajpai[1,2], Aniket Gupta[1,2], Om Prakash[1], Yogesh S. Chauhan[3], Hussam Amrouch[4]; [1]Karlsruhe Institute of Technology, Germany, [2]National Institute of Technology Uttarakhand, India, [3] Indian Institute of Technology Kanpur, India, [4] University of Stuttgart, Germany

WTHPE-054

Internal-Distributed CDM ESD Protection

Mengfu Di, Zijin Pan, Cheng Li, Albert Wang; University of California, Riverside, USA

WTHPE-055

Error Correction Scheme for Reliable RRAM-Based In-Memory Computing

Yixuan Hu, Kaili Cheng, Zuodong Zhang, Runsheng Wang, Yuan Wang, Ru Huang; Peking University, China

WTHPE-056

Impacts of Operation Intervals on Program Disturb in 3D Charge-trapping Triplelevel-cell (TLC) NAND Flash Memory

Xiaotong Fang, Yachen Kong, Yifan Guo, Menghua Jia, Xuepeng Zhan, Yuan Li, Jiezhi Chen; Shandong University, China

WTHPE-057

Vertical TSV-Like Diode ESD Protection

Cheng Li[1], Mengfu Di[1], Zijin Pan[1], Huaqiang Wu[2], Albert Wang[1]; [1]University of California, Riverside, USA, [2]Tsinghua University, China

WTHPE-058

A controller-embedded predictor for preventing unexpected failure in 3D NAND flash

Yuqian Pan, Mingyang Gong, Haichun Zhang, Zhuo Chen, Zhenglin Liu; Huazhong University of Science and Technology, China

WTHPE-059

A Study of the Electrical and Mechanical Reliability Properties of Suspended Graphene NEMS Devices for ESD Protection Applications

Li Shen[1], Yaoming Lv[1], Lele Jiang [1], Zhenghui Kong [1], Yu Lu[1,2], Qi Chen[3], Albert Wang[3], Yuhua Cheng[1,4]; [1]Peking University, China, [2]Shanghai Xirun Technologies, Co. Ltd, China, [3]University of California, Riverside, USA, [4]School of Electrical Engineering and Computer Science, Peking University, China

WTHPE-060

Development of a TLP System with a Novel Current Sampling Technique for ESD Protection Applications

Yu Lu[1,2], Yang Hong[2], Yuhua Cheng[2,3]; [1]Shanghai Xirun Technologies, Co. Ltd, China, [2]Peking University, China,[3] School of EECS, Peking University, China

WTHPE-061

Low temperature curable polyimides for advanced package application

Yuying Sui [1,2], Jinhui Li[1], Tao Wang[1], Liang Shan[1], Qiang Liu[1], Guoping Zhang[1]; [1] Chinese Academy of Sciences, China, [2]China University of Petroleum, China.

WTHPE-062

The Influence of Pre-Layer Processing on the Signal Integrity of 5G High Frequency Communication Multilayer LCP Lines

Haiqi Lai[1], Tao Chen[1], Guannan Yang[1,2], Yu Zhang[1,2], Chengqiang Cui[1,2]; [1]Guangdong University of Technology, China; [2]Jihua Laboratory, Foshan, China

WTHPE-064

Low CTE Polyimide for Advanced Package Application

Ao Zhong, Jinhui Li, Liang Shan and Qiang Liu; Guoping Zhang; Rong Sun; Shenzhen Institutes of Advanced Technology, Chinese Academy of Sciences, China

WTHPE-065

Crosstalk of octagonal TSV array arrangement based on differential signal

Jiang Han[1], Ziyu Liu[2], Ziyuan Zhu[1], Lin Chen[1], Qingqing Sun[1]; [1]Southwest University, China; [2]Fudan University, China

WTHPE-066

Stress adjusting for hillock size reduction in UTS CIS base on graphics analysis

Xianghua Hu, Guangzhi He, Xiaofang Gu, Qiliang Ni Huali; microelectronics Corp., China

WTHPE-067

A smart dummy flow in layout design for Xtacking Technology

Gavin Li[1], Jet Jiang[1], Frank Hou[1], Shaojun Liu[1], Zhengfang Liu[2], Xuesheng Fan[2], Chunshan Du[2]; [1]Yangtze Memory Technologies Co. Ltd., China, [2] Mentor Graphics (Shanghai) Electronics Technology Co., Ltd, China

WTHPE-068

Anomaly Detection and Analysis of FDC Data

Danli Gong[1], Yiwen He [2], Xiong Shao [3]; [1]Shanghai Huali Intergrated Circuit Corporation, China, [2]Shanghai Huali Intergrated Circuit Corporation, China,[3]Shanghai Huali Intergrated Circuit Corporation, China

WTHPE-069

Focal Auxiliary Classifier Generative Adversarial Network for Defective Wafer Pattern Recognition with Imbalanced Data

Jiahao Liu[1], Fuzuo Zhang[1], Bing Yang[2], Fuquan Zhang[2], Ying Gao[2], Huangang Wang[1]; [1]Tsinghua University, China, [2]Semiconductor Technology Innovation Center (Beijing) Crop., China

WTHPE-070

Neuronal Firing Characteristics in the NbO_2 based Mott Memristor

Xiaojian Zheng[1], Xinyi Li[1], Jianshi Tang[1,2], Bin Gao[1,2], He Qian[1,2], Huaqiang Wu[1,2]; [1] Institute of Microelectronics, Beijing Innovation Center for Future Chips (ICFC), Tsinghua University, China, [2]Beijing National Research Center for Information Science and Technology (BNRist), Tsinghua University, China

WTHPE-071

Core-Shell Dual-Gate Nanowire Synaptic Transistor with Short/Long-Term Plasticity

Md. Hasan Raza Ansari[1], Daehwan Kim[1], Seongjae Cho[1], Jong-Ho Lee[2], Byung-Gook Park[2]; [1]Gachon University, South Korea, [2]Seoul National University, South Korea

WTHPE-072

HfO_2/RuO_2 Interface Mediated Oxygen Balance in Memristor: An Ab Initio Study

Yun-Lai Zhu[1], Jun-Hui Yuan[1], Li-Heng Li[1], Kan-Hao Xue[1], Xiao-Min Cheng [1], Xiang-Shui Miao[1]; [1]Huazhong University of Science and Technology, China

WTHPE-073

In-Memory Hamming Distance Calculation Based on One-Transistor-Two-Memristor (1T2M) Structure

Zhizheng Zhang, Yi Li, Ling Yang, Jiancong Li, Xiangshui Miao; Huazhong University of Science and Technology, China

WTHPE-074

Optimal Design of DDR3 STT-MRAM Memory

Yueting Li[1], Gefei Wang[1,2], Kaihua Cao[1], Qunwen Leng[1], Weisheng Zhao[1]; [1]Beihang University, China, [2]Truth Memory Tech. Co. Ltd, China

WTHPE-075

Demonstration of a Fast, Low-voltage, III-V Semiconductor, Non-volatile Memory

Dominic Lane[1], Peter Hodgson[1], Richard Potter[2] Manus Hayne[1]; [1]Lancaster University, UK, [2]University of Liverpool, UK

WTHPE-077

A cantilever-structured AlGaN/GaN HEMT for building a strain-controlled platform

Xiao Cui[1,2], Qilin Hua[1,2], Keyu Ji[1,3], Bingjun Wang[1,3], Shuo Zhang[1], Weiguo Hu[1,2]; [1]Beijing Institute of Nanoenergy and Nanosystems, Chinese Academy of Sciences, China, [2]School of Nanoscience and Technology, University of Chinese Academy of Sciences, China, [3]Guangxi University, China

WTHPE-078

A Method of Forming Full-Wheatstone Bridge for Linear TMR Magnetic Sensors

Dingsong Jiang[1,2], Zhihong Lu[1,2], Mingming Chen[4], Jianzhong Yang[1,2,3]; [1]Department of Precision Instrument, Tsinghua University, China, [2]The State Key Laboratory of Precision Measurement Technology & Instruments, Tsinghua University, China, [3]Innovation Center for Future Chips, China, [4]University of Geosciences (Beijing), China

WTHPE-079

Tunable Sensing Performance of Linear Perpendicular TMR Sensor

Shaohua Yan[1,2], Zitong Zhou[1], Zhiqiang Cao[1,2], Yaodi Yang[2], Zhi Li[1,2], Weibin Chen[2,3], Qunwen Leng[1,2,4], Weisheng Zhao[1,2]; [1]School of Integrated Circuit Science and Engineering, Beihang University, China, [2]Beihang-Goertek Joint Microelectronics Institute, Qingdao Research Institute, Beihang University, China, [3] Shandong University, China, [4]Goertek Inc., China

WTHPE-080

Visible Light Sensitivity Enhancement of CMOS Image Sensor with Pseudo High Refractive Index Film Integrated by Directed Self-Assembly Process

I. Oshiyama, T. Shigetoshi, I. Mita, N. Sumitani, T. Oinoue, S. Saito, T. Okawa, Y. Ebiko, K. Yokochi, Y. Kitano, Y. Hagimoto, T. Hirano, H. Iwamoto; Sony Semiconductor Solutions Corp., Japan

WTHPE-081

Orientation Dependent Structural Facet Recognition Method in Anisotropic Wet Etching on R-plane Single Crystal Sapphire

Jiabao Yao, Jin Qian, Xiaoli Qiu, Yan Xing; Southeast University, China

WTHPE-082

Pressure and Thermally Induced Spin Crossover in a 2D Iron(II) Coordination Polymer {Fe[bipy(ttr)^2]}n

Mengyun Yuan[1], Ruixin Li[1], Quanjun Li[1], Ludmila Berezhnaya[2], Hennagii Fylymonov[3], Maksym Seredyuk[4], Nikita Liedienov[1,5], José Antonio Real[4], Georgiy Levchenko[1,5]; [1]Jilin University, China, [2]Donetsk Institute of Physics and Engineering, Ukraine, [3]Southern Federal University, Russia, [4]Universitat de Valencia, Spain, [5]Donetsk Physical –Technical Institute, Ukraine

WTHPE-083

FBAR Magnetic Sensor Composed of CMOS Compatible Materials

Xiaofan Yun[1,2], Wenkui Lin[2,3], Xiaoyi Wang[2,4], Zhongming Zeng[2] , Xinping Zhang[1] , Baoshun Zhang[2]; [1]Nanjing University of Science and Technology, China, [2] Suzhou Institute of Nano-Tech and NanoBionics, CAS, China, [3] Univ. of Sci. and Tech. of China, China, [4] Guilin University of Electronic Technology, China

WTHPE-084

UV-assisted High-sensitivity Room-temperature Pd-gated HEMT NO_2 Gas Sensor

Chong Xing, Dongcheng Xie, Haochen Zhang, Kang Song, Lei Yang, Yue Sun, Danhao Wang, Shi Fang, Zhongyu Shi, Lei Xu, Haiding Sun, Shibing Long; University of Science and Technology of China, China

WTHPE-085

A High Dynamic Range Capacitance-to-Digital Converter with Adaptive Parasitic Compensation

Junjie Shi[1], Xudong Qian[1], Shuangxi Lin[2], Xiaofei Chen[1]; [1]Huazhong University of Science and Technology, China ,[2]Wuhan Institute of Technology, China

WTHPE-086

Integrated Active Microfluidics using Flat Panel Display Technology with Two Different Semiconductor Grade Polymers

Boshen Liang[1,2], Grim Keulemans[1], Dominika Wysocka[1], Alexey Podkovskiy[1], Lei Zhang[1], Veronique Rochus[1], Tim Stakenborg[1], Paul Heremans[1,2], David Cheyns[1]; [1] Imec, Belgium, [2] KU Leuven, Belgium

WTHPE-087

Narrowband Photodetector by Integrating PTCDI-C_{13} J-aggregates with Graphene

Beilei Sun[1], Zefeng Chen[1], Jian-Bin Xu[13]; [1] Department of Electronic Engineering, The Chinese University of Hong Kong, Hong Kong SAR, China, [2]Materials Science and Technology Research Center, The Chinese University of Hong Kong, Hong Kong SAR, China

WTHPE-088

High-performance Photodetectors Based on 2D Defect-Rich Bi_2O_2Se Nanosheets

Chuanhui Gong, Xianfu Wang; University of Electronic Science and Technology of China, China

WTHPE-089

Fabrication and Research of MSM UV Detectors with Different Electrode Materials

Jun Liao, Cheng Wu, Rui Zhang, Yong Li, Tao Li; Shaoyang University, China

WTHPE-090

Design for a TE Mode Magneto-optical Circulator Based on Asymmetric Silicon Slot Waveguides

Yucong Yang[1], Shuyuan Liu[1], Wei Yan[1], Yan Zhang[2], Jun Qin[1], Longjiang Deng[1], Lei Bi[1]; [1]University of Electronic Science and Technology of China, China, [2]Chongqing United Microelectronics Center, China

WTHPE-091

Broadband frequency-doubled linearly chirped microwave waveform generation based on Fourier domain mode-locked optoelectronic oscillator

Guozheng Li[1,2], Tengfei Hao[1,2], Zengting Ge[1,2], Wei Li[1,2], Ming Li[1,2]; [1]Chinese Academy of Sciences, China, [2]University of Chinese Academy of Sciences, China

WTHPE-092

Disruptive Technology of Building Internet of Underwater Things: Laser-based Underwater Solid-State Lighting

Daqi Shen[1], Langyi Tao[1], Jinghao Yu[1], Pengfei Ye[1], Zhengxuan Sheng[1], Lvyang Zhou[1], Mingmin Shi[1], Shiliang Mei[2], Xiang Wan[1], Xiaojuan Lian[1], Xiaoyan Liu[1], Yi Tong[1]; [1]Nanjing University of Posts and Telecommunications, China, [2]Fudan University, China

WTHPE-093

Direct Patterning Copper Circuit on Textile for Wearable Electronics

Fei Li, Haijun Wang, Xiaofeng Shi, Yu Dai, Jie Zhang; Jiangnan University, China

WTHPE-094

Flexible Memristor based on Graphene-Silk Fibroin Bio-composite Paper

Xin Guo, Xinge Zhou, Changying Cao, Shan Wang, Quanhong Chang, Lei Huang; Shanghai Normal University, China

WTHPE-095

High-performance MXene-based pressure sensor for wearable electronics

Lili Wang[1], Guozhen Shen[2]; [1]Jilin University, China, [2]University of Chinese Academy of Sciences, China

WTHPE-096

A high-performance flexible fiber based on CNTs for real-time remote control of robots

Yinghui Li, Yucheng Lin, Shenshun Duan, Jun Wu, Wei Lei; Southeast University, China

WTHPE-097

High-performance, sub-2 volts TiO_2 thin film transistors enabled by ultrathin ZrO^2 gate dielectrics

Jie Zhang, Peng Cui, Guangyang Lin, Yuping Zeng; University of Delaware, USA

WTHPE-098

Flexible piezoresistive sensors with 3D CB/graphene conductive networks

Lijun Ma, Ye Gao, Shifeng Li, Xiao Lei, Xiaotian Li, Feng Liu; Wuhan University, China

WTHPE-099

Circuit Design and Experimental Verification of Low-voltage Organic Field-effect Transistor-based Common Source Amplifier

Li'ang Deng, Wei Tang, Lei Han, Yukun Huang, Xiaojun Guo; Shanghai Jiao Tong University, China

WTHPE-100

Cost-effective, mask-less, and high-throughput prototyping of flexible hybrid electronic devices using dispense printing and conductive silver ink

Sahira Vasquez[1], Mattia Petrelli[1], Martina Costa Angeli[1], Julio Costa[2], Enrico Avancini[1], Giuseppe Cantarella[1], Niko Münzenrieder[1,2], Paolo Lugli[1], Luisa Petti[1]; [1]Free University of Bozen-Bolzano, Italy, [2]University of Sussex, U.K

WTHPE-101

A 12-bit Fully Differential SAR ADC with a Novel Capacitor Mismatch Calibration

Xizhu Peng[1], Hanpeng Liu[1], Yuke Liu[1], He Tang[1,2]; [1]University of Electronic Science and Technology of China,[2]University of Electronic Science and Technology of China, China

WTHPE-102

Lateral p−n Homojunction formed by Local Doping for High-Performance Photodetector

Jiacheng Sun[1,2], Junying Zhang[2], Yuyan Wang[1,2]; [1]Tsinghua University, China,[2]Beihang University, China

WTHPE-103

Nanoscale Inverters Enabled by a Facile Dry-Transfer Technique Capable of Fast Prototyping of Emerging Two-Dimensional Electronic Devices

Yachun Liang, Jiankai Zhu, Fei Xiao, Bo Xu, Ting Wen, Song Wu, Jing Li, Juan Xia, Zenghui Wang; University of Electronic Science and Technology of China, China

WTHPE-104

Light-modulated graphene/organic phototransistor with infrared polarity switching

Jiayue Han[1,2], Xinwei Han[1,2], Chao Han[1,2], Jun Gou[1,2], Jun Wang[1,2]; [1]University of Electronic Science and Technology of China, China [2]University of Electronic Science and Technology of China, China

WTHPE-105

FDSOI NCFET with Stepped Thickness Ferroelectric Layer

Mingyuan Gu[1,2], Jiafei Yao[1,2], Yufeng Guo[1,2], Maolin Zhang[1], Qicong Liang[1,2], Jiayi Wu[1], Jincheng Liu[1], Dongxiang Xu[1]; [1]Nanjing University of Posts and Telecommunications, China, [2]National and Local Joint Engineering Laboratory of RF Integration and Micro-Assembly Technology, China

WTHPE-106

Fabrication of p-$MoTe_2$/n-MoS_2 heterostructure and its electrical characterization

Xinyu Chen[1], Yangye Sun[2], Ling Tong[1], Simeng Zhang[1], Xiaoxi Li[1], Jingyi Ma[1], Xiaojiao Guo[1], Minxing Zhang[1], Zhengzong Sun[2], Wenzhong Bao[1]; [1] School of Microelectronics, Fudan University, China, [2]Department of Chemistry, Fudan University, China

WTHPE-107

Quantum dot formation on suspended graphene nanomesh by helium ion beam milling technology

Fayong Liu[1], Manoharan Muruganathan[1], Shinichi Ogawa[2], Yukinori Morita[2], Zhongwang Wang[1], Marek Schmidt[1] , Hiroshi Mizuta[1,3]; [1]Japan Advanced Institute of Science and Technology, Japan, [2]National Institute of Advanced Industrial Science and Technology, Japan, [3]Hitachi Cambridge Laboratory, UK

WTHPE-108

Simulation and construction of physical reservoir based on gas molecules/carbon nanotubes/polyoxometalate composite structure

Shuo Wu[1], Wenli Zhou[1,2], Yu Zhu[1], Changsheng Chen[1]; [1]Huazhong University of Science and Technology, China, [2]Wuhan National Laboratory of Optoelectronics, China

WTHPE-109

Memristive Combinational and Sequential Logic for In-memory Computing

Xiaodi Huang, Ling Yang, Yi Li, Xiangshui Miao; Huazhong University of Science and Technology, China

WTHPE-110

Tunable synaptic devices based on ambipolar $MoTe_2$ transistor

Tingting Gao[1], Xuefei Li[1], Linxin Han[1], Yanqing Wu[1,2]; [1]Huazhong University of Science and Technology, China, [2]Peking University, China

WTHPE-111

A Flexible LIF Neuron Based on NbO_x Memristors for Neural Interface Applications

Jiaxue Zhu [1,3], Zuheng Wu[1,3], Xumeng Zhang[2], Yongzhou Wang[1], Jian Lu[1,4], Pei Chen[1], Lingli Cheng[1,3], Tuo Shi[1,4] Qi Liu[2]; [1]Institute of Microelectronics of Chinese Academy of Sciences, China; [2] Fudan University, China, [3]University of Chinese Academy of Sciences, China, [4]Zhejiang Laboratory, China.

WTHPE-112

Self-adaptive Matrix Equation Solving in Analog Memory Array

Jiancong Li, Houji Zhou, Yi Li, Xiangshui Miao; Huazhong University of Science and Technology, China

WTHPE-113

Investigation of Non-Linear Selection Effect on RRAM based Neuromorphic Computing Array with Passive Selective Element

Shengyu Bao, Zongwei Wang, Yaotian Ling, Zhizhen Yu, Yabo Qin, Yimao Cai, Ru Huang; Peking University, China

WTHPE-114

Impact of Non-Idealities in RRAMs on Hardware Spiking Neural Networks

Tejas Ketkar, Shubham Sahay; Indian Institute of Technology Kanpur, India

WTHPE-115

Memristive Stateful Logic with N-Modular Redundancy Error Correction Design towards High Reliability

Xi Zhu, Hui Xu, Hongchang Long, Qingjiang Li, Zhiwei Li, Haijun Liu, Yinan Wang; National University of Defense Technology, China

WTHPE-116

Efficient High Frequency Spin Wave Excitation with Undulating Ferromagnetic Film

Yuchen Cai, Qiming Shao; The Hong Kong University of Science and Technology, Hong Kong, China

WTHPE-117

Optoelectronic Synaptic Devices Based on the Heterostructure of Silicon Nanomembrane and P3HT

Peiwen Huang[1], Lei Yin[1], Yayao Li[1], Yue Wang[1], Deren Yang[1,2], Xiaodong Pi[1,2]; [1]State Key Laboratory of Silicon Materials & School of Materials Science and Engineering, Zhejiang University, China,[2]Institute of Advanced Semiconductors, Hangzhou Innovation Center, Zhejiang University, China

WTHPE-118

Chiplet-based System-on-Chip for Edge Artificial Intelligence

Mark Ping Chan Mok, Chi Hong Chan, Walter Chung Shui Chow, Yuzhong Jiao, Sha Li, Peng Luo, Yiu Kei Li, Meikei Ieong; United Microelectronics Centre (Hong Kong) Ltd., Hong Kong, China

WTHPE-119

Low Power Mixed-Signal Binarized CNN Processor

Chi Hong Chan, Yuan Lei, Peng Luo, Sheng Lin, Xiao Huo, Yiu Kei Li, Mei Kei Ieong; United Microelectronics Centre (Hong Kong) Ltd., Hong Kong, China

WTHPE-120

A Ta_2O_5/ZnO Synaptic SE-FET for supervised learning in a crossbar

Xiaoyao Song, Ashwani Kumar, Maria Merlyne De Souza; University of Sheffield, UK

Special Events

1) Young Engineers' Networking

Thursday, April 8, 2021

17:30–19:30 ShuJin Hall

Chair: He Tang, UESTC, China
Co-Chair: Qi Liu, Fudan University, China,
Co-Chair: John Dallesasse, University of Illinois at Urbana-Champaign, USA,
Co-Chair: Patrick Fay, University of Notre Dame, USA,
Co-Chair: Shuji Ikeda, tei Solutions Inc, Japan

The "Young Engineers' Networking" event is designed for young engineers and would-be engineers (e.g., students) to meet well-established engineers and to network with fellow young engineers. The "Young" and "Would-be" engineers will have a chance to directly interact with world famous professors, researchers and engineers in the Microelectronics, in an informal and friendly setting, to hear their successful experiences and to obtain valuable advices. This Networking event is open to all participating young and would-be engineers onsite. Registration to EDTM2021 is not required for attending this networking event. Light refreshments will be provided.

2) Women-in-Engineering (CWiE) Summit

The IEEE Chapters and Women-in-Engineering (CWiE) Summit, will be held during EDTM2021, which will provide a forum for local IEEE volunteers and women students and professionals to meet together and share their experiences and ideas on education, research and career activities in area of microelectronics, and offer valuable mentorship opportunities.

Registration

1) **In-Person** Technical Sessions Registration allows attending all technical sessions and includes tickets for daily lunch, banquet and 2 receptions. **Virtual** registration can only attend the meetings online (no other benefits, such as daily lunch, banquet and reception). **Technical Sessions Registration** means registration for the technical sessions only, not including Tutorials/Short Courses.

2) **Tutorial or Short Course Registration** is for attending tutorials or short courses (including lunch on the Tutorials/Short Courses day), but NOT attending any conference technical sessions. Tutorial or Short Course registration does NOT include tickets for the banquet and receptions.

3) Each accepted paper must be registered at an **In-Person/ Non-Virtual** rate (even for a virtual presentation)

4) Each accepted paper must be registered by **2/15/2021** in order to be allowed for presentation at EDTM2021 and be included in the Proceedings

5) **One** in-Person/non-Virtual registration covers **ONE** paper only. For example, if you have 2 papers, there must be 2 non-virtual registrations, each for one paper.

6) Extra ticket for the Banquet and the two Receptions can be purchased. This Banquet/Reception registration cannot be used to attend any technical session, tutorial or short course.

7) Attendees for the IEEE China Chapters & Women-in-Engineering (**CWiE**) Summit must register at an **In-Person/Non-Virtual** rate, which offers full conference benefits (i.e., technical sessions, daily lunches, banquet and receptions. But not including the Tutorials and Short Courses)

8) If you have any question, please send E-mail to nancy@tlan-group.com.

Registration Rates

	In-Person Advanced (3/20/2021 by 24:00 Beijing Time)	In-Person On-Site (>3/20/2021)	Virtual
Technical Sessions			
IEEE members	$500.00	$600.00	$50.00
Non-members	$600.00	$700.00	$100.00
IEEE Student members	$250.00	$300.00	$25.00
Student Non-members	$300.00	$350.00	$75.00
IEEE Life members	$250.00	$300.00	$25.00
Tutorials			
IEEE members	$100.00	$150.00	$30.00
Non-members	$150.00	$200.00	$50.00
IEEE Student members	$75.00	$100.00	$25.00
Student Non-members	$100.00	$125.00	$40.00
IEEE Life members	$75.00	$100.00	$25.00
Short Courses			
IEEE members	$200.00	$250.00	$40.00
Non-members	$250.00	$300.00	$60.00
IEEE Student members	$150.00	$200.00	$30.00
Student Non-members	$200.00	$250.00	$50.00
IEEE Life members	$150.00	$225.00	$30.00
CWiE Event			
IEEE members	$500.00	$600.00	
Non-members	$600.00	$700.00	
IEEE Student members	$250.00	$300.00	
Student Non-members	$300.00	$350.00	
IEEE Life members	$250.00	$300.00	
Extra Tickets			
Welcome Reception	$50.00		
Business & Exhibition Night	$50.00		
Closing Banquet	$70.00		

Visa Information

- Visa may be required to enter China.
- If needed, EDTM2021 can provide an Invitation Letter for your visa application.
- Please be aware of any travel restrictions amid the COVID-19 pandemic, and we are closely monitoring the situation.
- Should you need any assistance, please contact us at nancy@tlan-group.com .

Speakers' Instructions

Instructions for ORAL Presentations (including Invited)

Time Allocation for Presentations

	Presentation Time	Discussion Time	Total
Plenary talk	40 min	5 min	45min
Invited talk	15 min	5 min	20 min
Contributed talk	15 min	5 min	20 min
Tutorial & Short Course	60 min/lecture	10 min/lecture	70 min/lecture
(Each T/SC track has 3 lectures for a total of 3.5 hours)			

Preparing Your Presentation

Please use the provided PPT **Template** to prepare your oral presentations.

All speakers will use the laptop prepared by the conference for the presentation.

Windows 10 (English Version)

Applications: Power Point only (Version: 2007 or newer)

Fonts: Windows standard fonts

Use your own computer for presentation is **NOT** allowed.

Submit your PPT files in emails to your session co/chairs by **3/7/2021**

Your PPT slides will be pre-loaded to the presenting computers

Please bring your back-up PPT in a USB memory stick.

Please be in the session room at least 15 minutes prior to your session to check your slides and report to your session co/chairs.

Oral Presentations

You can control the slides using the provided laser pointer at the podium.
During presentations, you will be alerted by Time card and caution Bell.

After a lapse of ..	Caution	
12 minutes	Show "3 Min" time card	Warning
14 minutes	Show "1 Min" time card	Ending talk
15 minutes	Bell one time	End of talk
15 ~ 20 minutes	Q&A session	End of presentation

Virtual Presentation Formats

- EDTM2021 will go Hybrid. There will be a big in-Person meeting and you are welcome to come to Chengdu and enjoy the REAL conference. In case travel is prohibited, Virtual presentation/participation is supported.

1. **Plenary Keynote Speakers：** **Live** presentation on Zoom.
   - Please provide a pre-recorded video as a back-up
   - Please check your time zone
2. **Tutorial & Short Course Speakers:** **Live** presentation on Zoom.
   - Please provide a pre-recorded video as a back-up
   - Please check your time zone
3. **Invited & Regular Oral Speakers:** Presentations will be given by **pre-recorded videos**.
   - Please provide a pre-recorded video as a back-up
   - **Please upload your recorded videos to EDAS by 3/7/2021**

Instructions for Recording PPT Presentation as a Video

Example with Microsoft Office 2019

Step 1: select **Slide Show** > **Record Slide Show**

Step 2: choose from two options:

- **Record from Current Slide**
- **Record from Beginning**

Step 3: when ready, select **Record** and start presentation/speaking

Step 4: manage your recording:

- **Pause:** to pause a recording
- **Stop**: to end a recording
- **Replay**: to replay a recording
- **Pen**, **Highlighter**, **Eraser**: use the pen, highlighter or eraser tools to mark up your presentation/recording

Step 5: Remove your recording: select **Clear** and choose from options

Step 6: save a recording as a video: select **File** > **Export**

- Save your recording in **MP4**

Step 7: Upload your recorded presentation video to EDAS

Instructions for Poster Presentations (Session Code: WTHPE)

Poster Display and Removal

	Time and Date
Set-up	13:30 - 15:30, April 9
Presentation Time	18:30 - 20:30, April 9 18:30 - 20:30, April 10
Each/same poster paper will be presented TWICE in the same poster session (WTHPE) during the above date/time.	
Removal	09:00 - 15:00, April 11

Please use the provided poster **Template** to prepare your poster.

Include the paper number (#) at the top left corner of the poster panel.

The size of poster should be in A0 size with Portrait orientation.

Size (Width x Height): 841mm x 1189mm.

Poster sessions will be held in the Poster Area on the 3rd floor, next to the registration room (see the map below).

All posters presenters are responsible for putting up and removing their posters on their designated board during the times shown above.

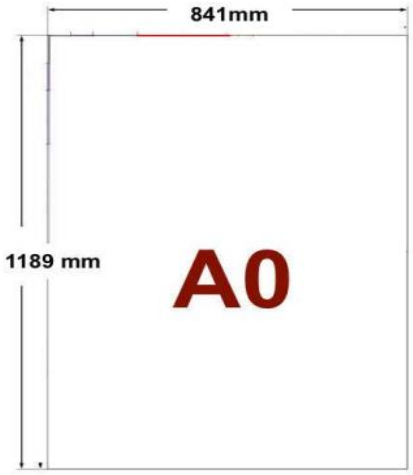
Posters remaining after the removal time will be removed and disposed of by the conference.

Each/same poster paper will be presented **TWICE** in the same Poster Session (WTHPE) during the above two dates/times.

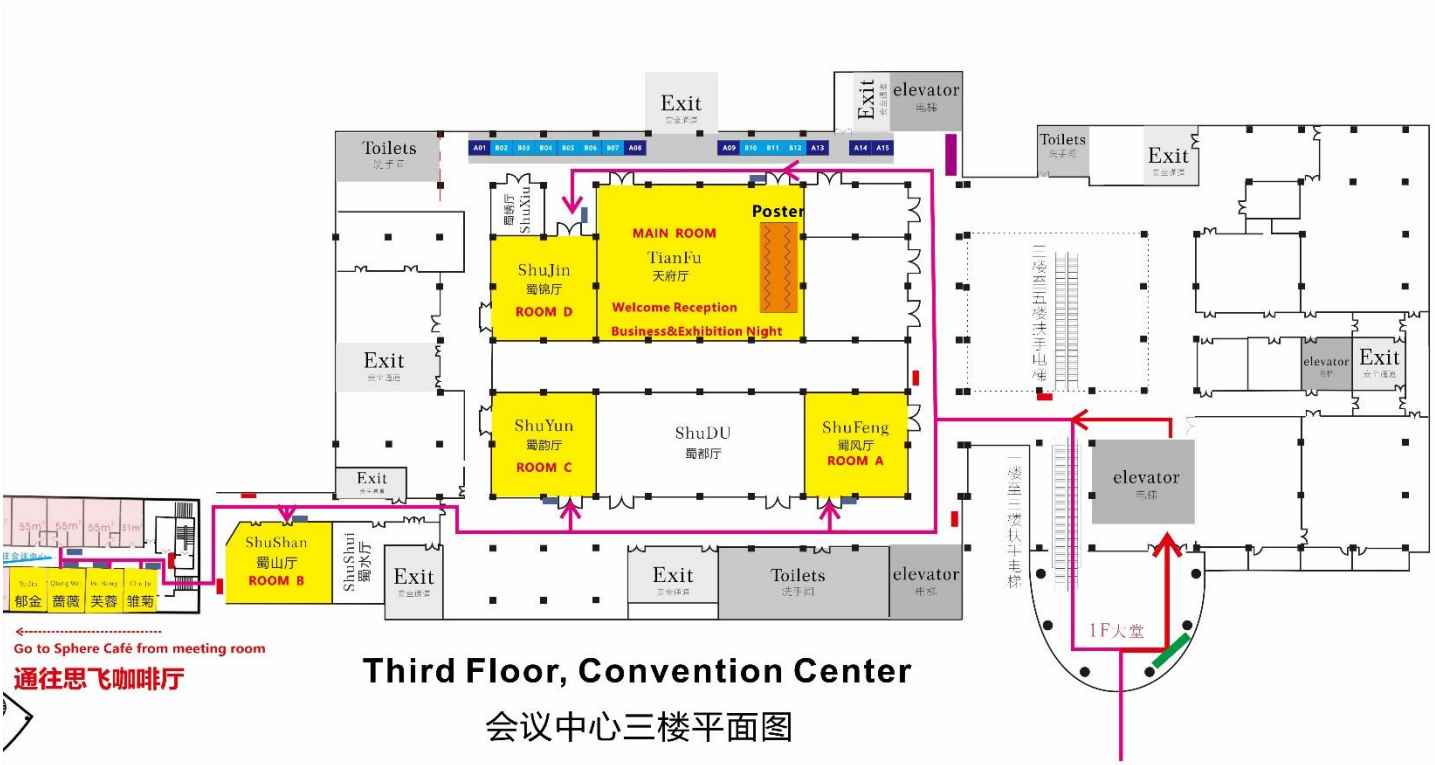
One author is required to interactively present your poster paper onsite.

Presenters are asked to arrive at least 10 minutes ahead of the scheduled poster presentation time.

Presenters should use double side tape or Velcro tape to put up your poster.



Conference Venue Map



Third Floor, Convention Center

会议中心三楼平面图

Second Floor, Holiday Inn

假日酒店2楼平面图

- Conference Hall
- Agenda Board
- Exhibition Booth
- Poster
- Welcome Board
- Guide Board
- Conference information Board
- Restaurant

VIP go to meeting room from the lobby of confernece center

VIP由会议中心大堂前往会场

Attendees go to Sphere Café from meeting room

参会人员由会场前往思飞咖啡厅

Attendess go to meeting room from the lobby of conference center

参会人员由会议中心大堂前往会场

Chengdu Local Transportation Information

Chengdu City Layout

Access to Venue - the Century City International Convention Centre

From North Railway Station:

By Subway: Take Line 1 from North Railway Station to Century City Station (15 stops); out from Exit A of Century City Station, walk ~1069 meters to the Venue.

By Taxi: ~16 kilometers, ~40 minutes, costs ~CNY50

From East Chengdu Railway Station:

By Subway: Take Line 7 from East Chengdu Railway Station to South Railway Station (6 stops); change to Line 1 from South Railway Station to Century City Station (5 stops); out from Exit A of Century City Station, walk ~1069 meters to the Venue.

By Taxi: ~16 kilometers, ~35 minutes, costs ~CNY40.

From South Railway Station:

By Subway: Take Line 1 from South Railway Station to Century City Station (5 stops); out from Exit A of Century City Station, walk ~1069 meters to the Venue.

By Taxi: ~6 kilometers, ~15 minutes, costs ~CNY20.

From Chengdu Shuangliu International Airport (CTU):

By Subway: Take Line 10 from Terminal-2/Terminal-1 of Shuangliu International Airport to Taipingyuan Station (4 stops); change to Line 7, from Taipingyuan Station to South Railway Station (3 stops); then change to Line 1, from South Railway Station to Century City Station (5 stops); out from Exit A of Century City Station, walk ~1069 meters to the Venue.

By Taxi: ~14 kilometers, ~40 minutes, costs ~CNY50.

Tourist Sites

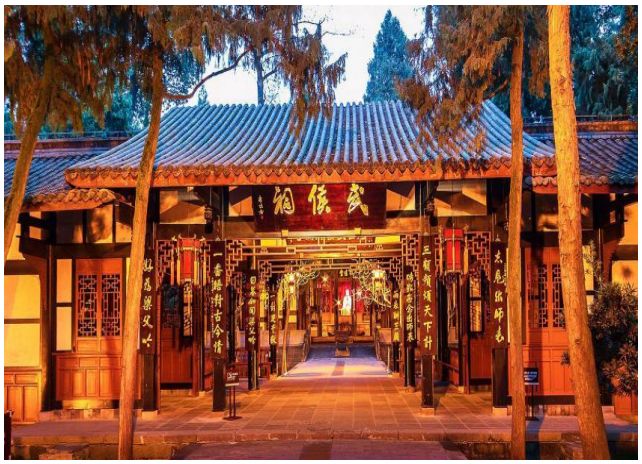
KuanZhaiXiangZi (宽窄巷子). Very nice place with lots of hi-end tea houses, restaurants and local snacks. Great for relaxing. Streets date back from late Qing-Dynasty, but rebuilt recently. Free government Wi-Fi in this place.

TianFu Square (天府广场) (Center of Chengdu). This square, overlooked by an enormous Chairman Mao statue in the center of the city, has been spruced up. Every evening at dusk, as well as at noontime, an elaborate music water show bursts out from the square's fountains. Below the square is the hub of Chengdu's subway system.

People's Park (人民公园) (West of Tianfu Square, two blocksaway, 15 mins walking distance.). This park is an important leisure place for Chengdu citizen. Every day, especially the holidays, the park is crowded with local people, hence, good for tourists to feel the real local life. Just follw the music, your can easily found local folks singing and dancing groups. You can also find people practicing Chinese calligraphy with water on the ground near a monument in the north-western corner of this park. There are many tea houses inside the park where locals drink tea and play majong. The average price of one cup of tea is CNY¥10. Do not forget to taste the famous Zhong's Dumpling(钟水饺) and various fancy local snaks in a Sichuan snak restaurant in the park, all at fair prices. This park is free to the public.

Sichuan Science and Technology Museum (四川科技馆) (Take a taxi or bus to Tianfu Square and walk to the large building directly behind the Chairman Mao statue). This huge four-storey museum is filled with interactive exhibits about science, aerodynamics, space, mathematics, robotics and physics. Children love the interactive displays and indoor playground on the 4th floor. During weekdays, the museum may be crowded with local school kids. Closed on Mondays. Entry fee CNY¥30, free for children.

Wuhouci Temple (武侯祠) (near Jinli Ancient Street, south-west of Tianfu Square). This temple is built to commemorate Zhuge Liang(诸葛亮) who was the Premier of Shu (蜀) Kingdom in ancient Three Kingdoms time. He is famous in China for his magic master mind of predicting everything in future, particularly in war games.



Jinli Ancient Street (锦里古街). This neighborhood is part of the old city of Chengdu. Packed with attractive hotels and small stores of old-fashion styles. Antiques are sold in different stores. Jinli Street is very popular among both tourists and locals, especially at night, for the bars, restaurants, and nightclubs. You can find a lot of famous local snack food over there, priced at CNY¥1-10. You can also tour the Wuhouci Temple nearby (entry fee CNY¥60, free with a Panda Card). Don't forget to have a camera with you.

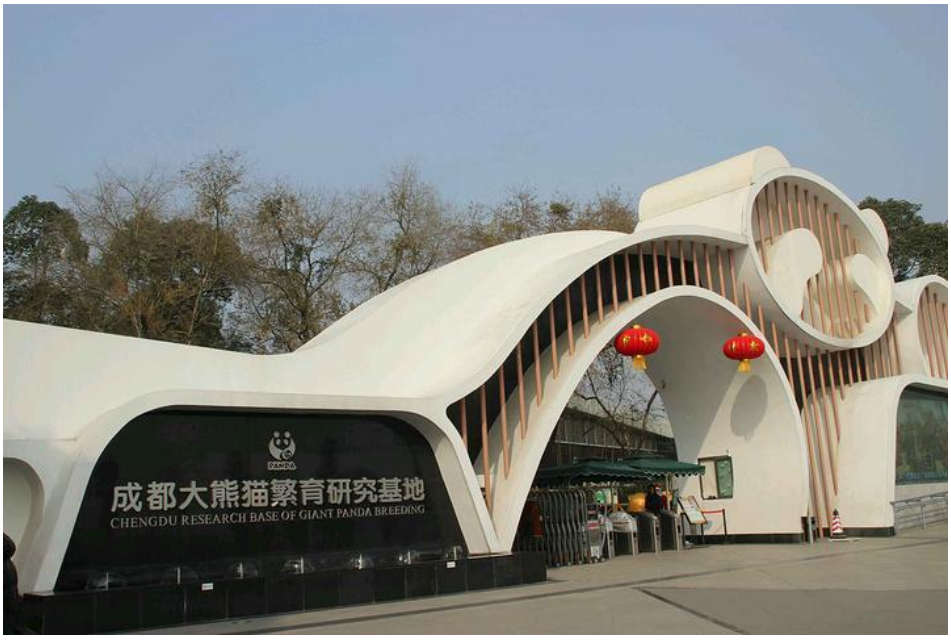
Jinsha Archaeological Site (金沙遗址) (Take Line 7、14、82、83、96、111、311、401 and 502, and get off at the north of Qingyang Avenue.Take Line 901 and get off at Jinsha Relics Road.). Recently discovered ancient ruins featuring various tools and art pieces from around 3,000 years ago. The amount of unearthed items is just massive. They include pottery, blades, jade items, building foundations and various golden art pieces.

Wenshu Temple (文殊院) (15 Wenshuyuan St, 成都文殊院街 15 号, off Renmin Zhong Rd). This Tang Dynasty Buddhist temple is the most impressive, and perhaps also the most worshipped, temple in Chengdu. It is dedicated to the Buddhist holy figure of Wisdom, Wenshu Pusa (Manjusri Bodhisatva), and contains more than 450 Buddha statues and other precious relics. In addition to the halls and gardens, the temple also has a charming tea

house that offers a taste of Chengdu life as it is frequented by locals as a place for chess games, reading, knitting, or just chatting with friends. Entry fee is CNY¥5
.

Qingyang Temple (青羊宫) (Palace of the Black Ram) (9 Xierduan, Ring Rd One, 一环路西二段 9 号). This Taoist temple is the oldest and biggest of its kind in the area, located in the west of the downtown. This is a large and still-active temple built per the taoist philosophy. While having a long history, the buildings are quite modern, featuring frequent shows. A teahouse and a vegetarian restaurant can be found within the temple complex.

Chengdu Panda Research Base of Giant Panda Breeding（成都大熊猫繁育研究基地） (Take tourist bus 902 from Xinnanmen Bus Station, or bus 97 or 198, or take a taxi from downtown). This is the biggest facility of this kind in the world. Due to habitat destruction and other reasons, the giant panda is maybe the most famous but endangered animal. It is home to some 60 giant pandas. It also hosts some red pandas and a colony of black-necked cranes. The best time to visit is in the morning, when pandas are most active. Feeding time is around 9:30-10:00am.


成都大熊猫繁育研究基地
CHENGDU RESEARCH BASE OF GIANT PANDA BREEDING

IEEE
445 Hoes Lane
Piscataway, NJ 08854, USA

EDTM 2021

Chengdu Century City New International
Convention and Exhibition Center
April 8–11, 2021

PROGRAM