**Guidelines for EDTM Paper**

**with 14-pt Title even for 2 Rows**

Nihar Ranjan Mahapatra1, Shubham Sahay2, Mayank Shrivastava3, and Yogesh Chauhan2

1IIT Gandhinagar, India, 2IIT Kanpur, India 3IISc Bangalore, India

**Abstract**

This abstract is a brief (75 words) synopsis of your **3-page** **camera-ready** paper.

Keywords: Manufacturing, CMOS and SOI

**Introduction**

This template has been tailored for output on A4- or letter-sized paper. Margins, column widths, line spacing, and type styles are built-in; examples of the type styles are provided throughout this document and are identified in italic type, within parentheses, following the example, for the Electron Devices Technology and Manufacturing conference (EDTM) [1]. Final camera ready 3-page paper of text with 2 columns, figures and tables should be submitted by October 15, 2023. The paper should explain why and how it was done, principal results, and their significances.

**Formats and Fonts**

14, 12 and 10 pt of Times New Roman are used for the title, author/affiliation and text, respectively. In particular, the use of the International System of Units (SI Units) is advocated. And use a zero before decimal points: “0.25”, not “.25”.

*A. Equations*

10-pt Italic of Times New Roman is used for the equation, as shown in Eq. (1). The number of equation within parentheses are to position flush right.

*y = f(x)* (1)

*B. References*

When referring to them in the text, type the corresponding reference number in square brackets as shown at the end of this sentence [1].

*C. Table*

8 pt of Times New Roman is used for the caption, as shown in Table 1.

*D. Figure*

Note that the digest of EDTM will be provided as electronic information. The font size in the figures should be large enough to make it readable in the printed version on A4 paper. 8 pt of Times New Roman is also used for the caption.

**Conclusion**

Summarize the contents of paper. And finally, don't forget to check the spelling.

**Acknowledgments**

The authors gratefully acknowledge the contributions of J. E. Lilienfeld, J. Bardeen, W. Brattain, and W. Shockley to the semiconductor industry.

**References**

1. <https://ewh.ieee.org/conf/edtm/2023/>
2. K. Ishimaru, “Future of Non-Volatile Memory -From Storage to Computing-,” IEDM Tech. Dig., p.12 (2019).
3. M. D. Ganeriwala, A. Singh, A. Dubey, R. Kaur and N. R. Mohapatra, “A bottom-up scalable compact model for quantum confined nanosheet FETs”, IEEE Trans. Electron Devices, 69, pp. 380-387 (2022).
4. A. Sharma, R. Goel, and Y. S. Chauhan, "Analysis and Modeling of OFF-state Capacitance in LDD MOSFETs", IEEE Electron Devices Technology and Manufacturing Conference (EDTM) (2023).
5. S. Lashkare, S. Chouhan, T. Chavan, A. Bhat, P. Kumbhare, and U. Ganguly, "PCMO RRAM for Integrate-and-Fire Neuron in Spiking Neural Networks", IEEE Electron Device Lett., 39, pp. 484 (2018).
6. T. Ketkar, and S. Sahay. "Impact of Non-Idealities in RRAMs on Hardware Spiking Neural Networks." in 5th IEEE Electron Devices Technology and Manufacturing Conference (EDTM), pp. 1-3, 2021.
7. S. S. Parihar, S. Thomann, G. Pahwa, Y. S. Chauhan, and H. Amrouch, "5nm FinFET Cryogenic SRAM Evaluation for Quantum Computing", 81st Device Research Conference (DRC) (2023).
8. S. Sahay, and M. J. Kumar, “Junctionless field-effect transistors: design, modeling, and simulation” IEEE-Wiley Press, ISBN: 9781119523529 (2019).

Table 1: List of font sizes.

|  |  |  |
| --- | --- | --- |
| Text | Type | Font [pt] |
| Title | Bold | 14 |
| Authors |  | 12 |
| Affiliation |  | 12 |
| Headings | Bold | 10 |
| *Sub-headings* | Italic | 10 |
| Main text |  | 10 |
| *Equation* | Italic | 10 |
| References |  | 8 |
| Footnotes |  | 8 |
| Table caption |  | 8 |
| Figure caption |  | 8 |



Fig. 1: Logos of the IEEE, EDS, and EDTM