Redefining Hardware Specializations at Runtime on ASIC/SoC Platforms for Application Acceleration

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Prof S.K. Nandy
Supercomputing Education and Research Center
Indian Institute of Science, Bangalore

Abstract

With shrinking feature sizes in CMOS technology, the ITRS roadmap projects that by year 2020 62% of a SoC will be reconfigurable in order to be able to fix hardware errors post fabrication. Runtime reconfigurable ASICs/SoCs therefore bears the promise to reduce design turnaround time. The total cost of solution is also reduced since a variety of applications from a given domain and their derivatives can now be hosted on the same platform without having to incur additional NRE cost of fabrication.

In this presentation, we will discuss how runtime reconfigurable ASICs/SoCs can be modelled so that multiple applications and their derivatives in a domain are synthesized on it. We will discuss the architecture of such a platform, together with a electronic system level (ESL) design flow wherein an application described in a High Level Language (eg. C, C++) is systematically transformed into application substructures for which hardware specializations are synthesized on the ASIC/SoC platform at runtime.