

# Power Optimal Network-on-Chip Interconnect Design

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**Abstract**—Chip Multi Processors (CMP) have become a widely studied topic and used in commercial products like Intel’s Quad Core and the PS3 playstation. Large part of these chips are interconnects. Increasing communication complexity due to large number of cores has made essential design and architecting of new strategies for interconnects such as Network on Chip (NoC). Technology scaling has made power dissipation in the interconnect a substantial part compared to that in the logic cells. Ways to reduce power dissipation in interconnects on chips has thus become necessary. With 65nm products available and 45nm in the offing, chip designers are forced to use actual fab based data, instead of predictive models for the purpose of analysis. In this paper, we present a methodology by which optimal bus width and frequency of operation for interconnects and routers in a CMP based NoC can be determined that provide guaranteed throughput and dissipate minimum power. We develop closed form expressions for the power dissipated in terms of bus width and frequency. We then use Lagrange multiplier method to arrive at the optimal values. We present the optimisation of a 4x3 router in 90nm technology. Inputs on how to use the methodology for design space exploration is also given. Further, usage of the methodology in the context of reconfiguration also explained.

## I. INTRODUCTION

With technology scaling into deep sub-micron, the frequency of operation and the number of transistors on the chip are increasing[1]. Today, chips with many processing cores has become a reality[2], [3]. Clocking strategies are becoming ever challenging [4], [5]. Wider, reconfigurable bus [2] and GALS approach are some of the suggested approaches for clock and interconnect design. Networks-on-Chip (NoC) is one of the proposed solution for the on-chip network architecture[6]. NoC, being a modular and scalable solution scores above the rest.

Low power techniques has enabled the reduction of power dissipation in logic cells. The dissipation in the interconnects has not seen similar rate of reduction. Lack of an interconnect architecture design and optimisation tool has been identified as one of the major issues to be overcome, by the ITRS [7].

We consider the problem of reducing the power dissipated in the interconnect and the router of an NoC, while maintaining a minimum throughput. We present our solution for the general CMP category of NoC. Fig.1 shows the general scenario of a CMP type NoC. Application Specific System on

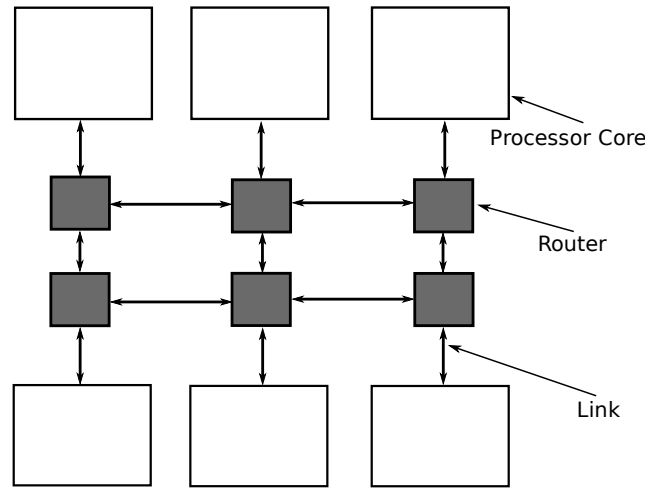


Fig. 1. An example of six core CMP. The links can take various widths.

Chip (ASSoC) category of NoCs use ad-hoc solutions that cannot be extended to other cases since they exploit case specific data and constraints during optimisation and design.

Consider two entities on a chip (Fig.1) that need to exchange data at a rate of 2GB/s. The extreme ways of achieving this is to have

- 1) bus width of 16Gbits and the entities clocking at 1Hz
- 2) a serial link that switches at 16GHz

The first one occupies enormous area and the interconnect consumes the major fraction of the power and the second requires exorbitant switching frequency and the logic cells that constitute the entities now consume the major fraction of the power. Somewhere between the two solutions there must exist an optimum or range of values where the conditions are suitable for implementation.

In this paper, we present a CMP based NoC design which takes throughput requirement as constraint and gives an optimal bus width and frequency of operation. These optimal values can be used by reconfiguration tools to pre-compute power optimal configurations to evaluate the optimality of the incremental changes performed during reconfiguration.

In Section III we present the formulation of the optimisation problem. Section IV provides one way of solving the proposed

formulation. Further we have a brief explanation on how the models used in formulation and solution were developed in Section V. Experimental results are presented in Section VI. Conclusions and future work in presented in Section VII.

## II. PREVIOUS WORK

Solving the power optimisation has been considered before [8], [9], [10]. All of them employ iterative schemes or search based techniques wherein the existence or convergence of solution cannot be guaranteed. While some approaches enforce many conditions[8], [10] others require layout verified design libraries to be present [9].

We propose a novel concept of using closed form expressions to evaluate power. This enables us to use many standard techniques to solve the optimisation problem. Further, the pre-requisites to solve are fewer in our formulation. The methodology proposed can also be used for design space exploration.

## III. PROBLEM FORMULATION

Consider a network of processing elements and memories. The topology is given by a graph  $G(V, E)$  where  $v_i \in V$  denotes processing elements or memories with in-built routers,  $e_k = \{v_i, v_j\} \in E$  denotes the physical link between two nodes. The worst case traffic that is required to be supported by the NoC interconnect is  $T$  Mb/s.

The objective of the design procedure is to provide a frequency  $f$  of operation for the router and a buswidth  $q$  for the physical links that interconnect the routers such that the sum of power dissipated in the router and the interconnect is minimal while meeting the throughput of  $T$  MB/s.

*Components of the power equation:* The total power consumed by the system ( $P$ ) consists of the power consumed by the router ( $P_1$ ), interconnect lines that make up the physical links ( $P_2$ ), the interconnect inside the router ( $P_3$ ) and the power consumed in the node ( $P_4$ ).

We deal only with the design of the NoC interconnect, hence  $P_4$  is treated as a constant value and not considered in our solution. The router can be viewed as made of two categories of logic cells: those which vary in number with change in the buswidth (mostly the data path elements) and those that do not (mostly the control path elements). If the power consumed by data path elements is  $\alpha_p$  and the power consumed by the control path elements is  $\beta_p$  then  $P_1$  can be expressed as  $(\alpha_p q + \beta_p) f$ .

Power dissipated in the interconnect depend on the bitrate (frequency) and length of the interconnect. Of the various models proposed for interconnects [11], [12], [13], we choose the lumped R-C model for our analysis. We use the resistance and capacitance values given in the 90nm technology library file for the lumped R-C model. The data available is for segments of  $1\mu\text{m}$  and hence we consider the interconnect to be made of  $1\mu\text{m}$  segments with values as given in the libraries. Effective capacitance  $C$  of interconnect with arbitrary length is calculated from the total impedance for that length. Power dissipated is then  $\alpha \frac{1}{2} C V_{dd}^2 f$ , where  $\alpha$  is

the switching factor,  $V_{dd}$  is the supply voltage and  $f$  is the frequency of operation. Values obtained by this method were in close correlation to the back annotated information obtained from layout. Straight line fit was then done on the power values obtained using the model for various lengths. The coefficients for straight line are  $a, b$ ; then  $P_2 = (al + b)f$  where  $l$  is length of the interconnect.

The technology library files also give area occupied by each logic cell. Total area occupied by data path elements is termed  $\alpha_a$  and by control path elements is termed  $\beta_a$ . The area occupied by the router can then be stated as  $(\alpha_a q + \beta_a)$ . Area along with basic floor plan information is used to obtain the average length of the interconnect inside the router. Consider a 4 port router shown in Fig.2(a). The data lines from one port have to travel to all other ports. Assuming that the router layout is shaped as a square, and one port is on each side of the router, the average length of interconnect for one port is twice the side of the square.

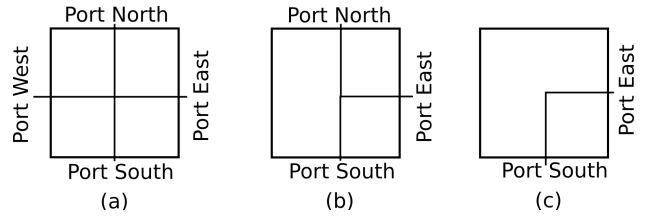


Fig. 2. FloorPlan for (a)Node in the centre of mesh, (b)Node along edge of mesh or ring of spidergon, (c)Node at corner of mesh

Similarly, the average length of 3 port router shown in Fig2(b) is  $1\frac{1}{2}$  times the side and 1 times for 2 port router shown in Fig 2(c). The average length when used in the 'l' of expression for  $P_2$  gives us  $P_3$ .

The design problem can be now stated as an optimisation problem as follows:

$$\text{Min}(P) \quad (1)$$

subject to :

$$\begin{aligned} f &\geq 0, \\ q &\geq 0, \\ fq &\geq T \end{aligned} \quad (2)$$

Where,

$$\begin{aligned} P &= P_1 + P_2 + P_3 \\ &= (\alpha_p q + \beta_p) f + (a\sqrt{\alpha_a q + \beta_a} + b) f q \\ &\quad + 8q f (a\sqrt{\alpha_a q + \beta_a} + b) \end{aligned} \quad (3)$$

Equation 3 is the closed form expression for power  $P$  and we can adopt various standard techniques to solve the same.

## IV. SOLUTION

None of the optimisation approaches till date, present closed form expressions for the power consumed. However, optimisation based approach for the power reduction is not new[8], [9],

[10]. In all these cases, search based techniques are used on a set of discrete points. Due to this, solution convergence cannot be guaranteed for all initial conditions. Also introduction of extra variable brings in additional dimension to search space.

Our formulation has closed form expressions which allows us to visualise the scenario through graphs as shown in Fig 3.

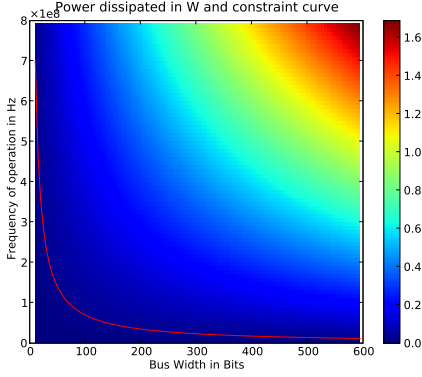


Fig. 3. Surface plot for P

Fig 3 shows a contour plot of power dissipation against buswidth  $q$  along x-axis and frequency  $f$  along y-axis. The colour bar by the side of the plot shows power dissipation in Watts corresponding to different colours in the plot. The throughput constraint is shown as a red curve in the plot.

The constraints (2) are satisfied only at points  $(f, q)$  such that  $f$  and  $q$  are strictly positive. It suffices to look at the compact set

$$S = \{(f, q) \mid f \leq F, q \leq Q, T \leq fq \leq FQ\} \quad (4)$$

Where  $F$  and  $Q$  are the maximum implementable bus width and frequency respectively. Relaxing the constraint  $fq \geq T$ , we get the Lagrangian function

$$L(f, q, \lambda) = P(f, q) - \lambda(fq - T) \quad (5)$$

Conditions that need to be satisfied by critical points are

$$\frac{\partial L}{\partial f} = 0 \quad (6)$$

$$\frac{\partial L}{\partial q} = 0 \quad (7)$$

$$\frac{\partial L}{\partial \lambda} \geq 0 \quad (8)$$

$$\lambda \geq 0 \quad (9)$$

$$\lambda \frac{\partial L}{\partial \lambda} = 0 \quad (10)$$

In case the optimal solution cannot be found by algebraic methods, numerical methods can be used on set  $S$ .

## V. DEVELOPING THE MODELS

In this section, we present the method by which values for  $\alpha_p, \beta_p$  and other coefficients are chosen for an example router architecture. The same procedure can be used for other router architectures. The router considered in this paper has

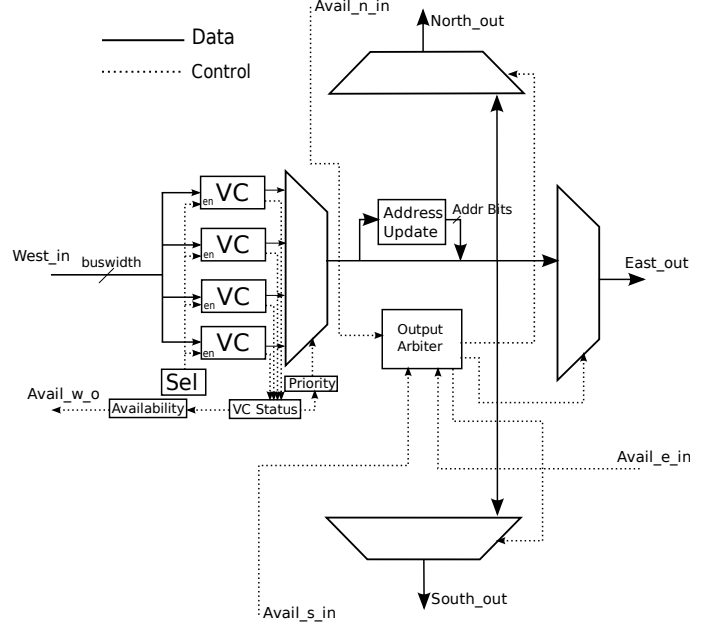


Fig. 4. Architecture of basic block in router

the architecture as shown in Fig.4 [14].

$\alpha_p$  is the power contributed by data-path elements and  $\beta_p$  is the power contributed by control-path elements. Consider a 4-to-1 multiplexer; logic required to drive the select lines of the multiplexer does not vary with bus width, but the logic required to drive the input lines does vary with bus width. Here logic that drives the select lines is the control path logic and the logic that drives the input lines is the data path logic. On similar lines, for the router in Fig.4 virtual channel and multiplexers form some of the the data path elements. Using the back-end library file, we identify the logic cells used for synthesis of these data-path elements. Library files provide power dissipated in logic cells with nW/Mhz as unit.  $\alpha_p$  is sum of these power values for all cells used in data-path elements. In Fig.4, modules like Output Arbiter, Address Update form part of the control path.  $\beta_p$  is the sum of power values for all the control path elements.

One has to exercise caution while selecting the cells from library file, as there are different sizes of same functional units and various cells with very similar functionality. Area occupied by the cell is also listed in the library file.  $\alpha_a$  is sum of areas for cells used in data-path elements and  $\beta_a$  is the sum of areas for control path elements.

We have written a C program which evaluates the effective capacitance of an 'n' stage R-C ladder. This capacitance value is used in  $\frac{1}{2}CV_{dd}^2f$  equation to estimate the power. Verification of the values obtained by the C program is done

as described below: Using Cadence SoC Encounter<sup>1</sup> layout for a design consisting of back-to-back inverters is done with various die-density in placement stage. This generate layouts with inverters having interconnects of various lengths connecting them. In order to obtain straight interconnect without jumps and vias, appropriate placement and routing blockages are placed. Parasitic extraction is done for each case and SPEF file obtained is used in Synopsys Prime Power<sup>2</sup> to estimate the power. The power value is compared with value obtained from C program. Since the values have close correlation, a C program is used to plot power against length for various frequencies. Kpolynom<sup>3</sup> is then used to get a straight line fit for the values.  $a$  and  $b$  are coefficients of the equation for straight line fit.

## VI. RESULTS

We consider a 4x3 router[14] which can service every port in each clock cycle. Architecture is shown in Fig.4. The router is made of 4 such basic blocks, one for each input port. We use 90nm library provided by Euro Micro lab. Various parameters used in the design are listed in Table I.

$a = 1.58 \times 10^{-16}$	$b = 1.6 \times 10^{-14}$
$\alpha_p = 333 \times 10^{-15} W/Hz$	$\beta_p = 705.6 \times 10^{-15} W/Hz$
$\alpha_a = 398.252 \mu m^2$	$\beta_a = 595.83 \mu m^2$
$T = 2 \times 10^{11} bits/s$	

TABLE I  
VALUES OF DESIGN PARAMETERS

The procedure to calculate the optimum bus width  $q$  and the frequency  $f$  is as follows. From complementary slackness constraint (10) there are two cases possible.

1) Condition  $f q = T$

(6) gives us expression involving  $q$  and  $\lambda$  from which we get expression for  $\lambda$  in terms of  $q$ . Substituting this for  $\lambda$  in (7) and simplification results in equation (11) which has  $f, q$  as variables.

$$9fq \left( \frac{a\alpha_a}{2\sqrt{\alpha_a q + \beta_a}} \right) - \frac{\beta_p f}{q} = 0 \quad (11)$$

The condition  $f q = T$  and (11) form a system of simultaneous equations. Eliminating  $f$  from these, results in (12).

$$81a^2\alpha_a^2q^4 - 4\alpha_a\beta_p^2q - 4\beta_a\beta_p^2 = 0 \quad (12)$$

With values in Table I, the feasible values for (12) are 1.497, 12.97.

2) Condition  $\lambda = 0$

Using condition  $\lambda = 0$  and solving (6) gives feasible  $q$  values as 277.6, 1.33, 1.66. The same condition in (7) and using  $q \neq 0$  gives feasible  $q$  values as 0.03.

Bus-Widths, Freq (GHz)	Power Dissipated			
	P1(mW)	P2(mW)	P3(mW)	P(mW)
q=10, f=5	20.17	1.33	10.67	32.18
q=12, f=4.1	19.58	1.37	11.03	32.00
q=14, f=3.5	19.17	1.42	11.36	31.95
q=16, f=3.1	18.85	1.45	11.67	31.98
q=18, f=2.7	18.61	1.49	11.97	32.07

TABLE II  
POWER DISSIPATED FOR VARIOUS BUS-WIDTHS

Evaluating  $P$  for all the feasible values of  $q$ , 12.97 corresponds to the minimum. Hence the required bus width is 13 bits and associated frequency is 3.84GHz. Since the objective function has low sensitivity around the minimal point, we conclude bus width 8 to 16 corresponds to the power optimal region.

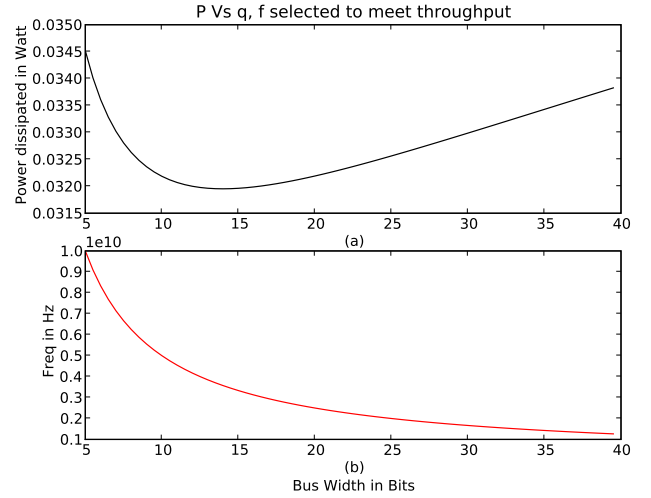


Fig. 5. (a)Power dissipated versus buswidth, (b)Frequency versus buswidth

Graph in Fig. 5(a) shows variation of total power dissipation against the bus width  $q$ , Fig. 5(b) shows the frequency required to meet the throughput for a given bus width. Sensitivity of graph in Fig. 5(a) about the optimal is quite low. However, sensitivity of graph in Fig. 5(b) in the same region is high. In the case of not being able to operate at optimal frequency, we know from Fig. 5(a) the trade-off on power in order to meet the timing. Hence, not only do we present a means to obtain the optimal conditions, but also an analysis procedure by which one can visualise the design space.

Table II lists component-wise split up of power values for certain bus widths along with frequency required to meet the throughput.

## VII. CONCLUSION AND FUTURE WORK

For CMP category of NoC, usage of closed form expressions to evaluate power is a novel concept. The proposed analytical method reduces the design cycle time. The method also allows to perform design space exploration with negligible effort for subsequent design iterations. Once the expression

<sup>1</sup>Product by Cadence, www.cadence.com

<sup>2</sup>Product by Synopsys, www.synopsys.com

<sup>3</sup>Software available with KDE

for power is developed, effect on total power consumption for various number of ports in routers and usage of bigger cells in select places can be studied.

When an SoC that uses NoC gets reconfigured to meet different throughput or topology, our model can be used by the implementation tools to obtain the optimal parameters for the new configuration. Various power optimal configurations can be pre-built and can be used for NoC reconfiguration. It is even possible to use our solution in embedded systems to compute the power optimal configurations, if the embedded system can generate the configuration.

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