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A Modular FPGA-based Phased Array System for Ultrasonic Levitation with MATLAB

1st Sebastian Zehnter
Chair of Control Engineering
University of Augsburg
Augsburg, Germany
sebastian.zehnter@informatik.uni-augsburg.de

2nd Christoph Ament
Chair of Control Engineering
University of Augsburg
Augsburg, Germany
christoph.ament@informatik.uni-augsburg.de

***Abstract*—In the present work, a modular and low-cost FPGA-based phased array system was developed that uses transducers emitting at 40 kHz for the acoustic levitation of small objects ($\leq$ 4 mm). The system consists of a driver board, transducer arrays with various layouts, and software developed in MATLAB®. The software can be used to simulate the acoustic field, calculate acoustic traps, and control the driver board via a provided USB-SPI interface. The driver board controls up to 100 channels simultaneously with square-wave signals up to 20 Vpp with $\pi/1024$ phase resolution and 10 bit amplitude resolution. Several phased arrays can be linked via a provided I^{2}C interface to increase the number of available channels. The functionality of the system is demonstrated by the levitation of small objects using a flat 40 kHz transducer array.**

***Index Terms*—Phased arrays, FPGA, ultrasonic, acoustic, levitation, non-contact handling, MATLAB, open hardware**

I. INTRODUCTION

The controlled handling of small or fragile objects may not be sufficiently solved with conventional mechanical gripping systems. Non-contact grippers transmit forces and torques to the object without mechanical contact and offer an innovative solution for this task. For manipulation, aerodynamic, electrostatic, optical, magnetic or acoustic effects are used [1]. In comparison, acoustic levitation has hardly any requirements on the material properties of an object and makes it possible to transport both solids and fluids without contact. Its wide range of applications includes biophysics [2], materials science [3] and microsystems technology [4]. The single-beam levitation of small objects in mid-air was experimentally demonstrated by Marzo et al. in 2015 [5]. In their approach, a large number of transducers that form a phased array are controlled individually with respect to their phases to generate a desired acoustic field by the interference of the emitted waves. The object is suspended in air by spatially defined maxima of the acoustic radiation force which create an acoustic trap [6].

Researchers are currently facing a difficult task in selecting a suitable phased array system to utilize acoustic levitation in their scientific fields. Commercially available systems such as Stratos™ (Ultrahaptics, Bristol, UK) [7] or Holographic Whisper (Pixie Dust Technologies, Tokyo, Japan) [8] are designed for specific applications, namely haptic sensations and parametric speaker, and therefore unsuitable for this task. In addition, commercial products are usually closed systems that tend to be hardly adaptable to requirements in various fields of research. Other non-commercial systems such as UARP [9] [10] or ULA-OP [11] [12] that have been developed for reasearch purposes do not aim directly at the lower frequencies of airborne ultrasound of 20 to 100 kHz. Hence, Marzo et al. introduced the two open low-cost systems TinyLev [13] and Ultraino [14] that are based on the Arduino platform. Although they both provide a sound introductory to study the effects of ultrasonic levitation, their capabilities are either limited by the available number of GPIOs or the low operating frequency and consequently the low phase resolution. Thus, an FPGA-based approach such as the recently proposed design by Beasley et al. [15] for the Xilinx Zynq SoC offers a promising solution for extending the capabilities of open systems for ultrasonic levitation. However, the usage of proprietary development boards limits the modularity of the system.

In the present work, we present a modular and open low-cost FPGA-based phased array system that is controlled by MATLAB® and provide additional open software and hardware to encourage further reasearch in ultrasonic levitation.

A. Related work

In recent years, several phased array systems have been built for various applications. A selection of prototypes that were developed in academic context in the last six years are listed together with this approach in Table I. To provide a better insight, they are categorized regarding the following aspects:

- *utilized hardware*: the device type and its clock rate, the amplifier type and its maximum voltage as well as the number of transducers used in the phased array system and their emitting frequency
- *calculation platform*: whether the phase angles are calculated directly on the hardware (HW) or in software (SW)
- *interface*: the interface used for data transmission between a PC and the phased array system
- *performance*: expressed in the update rate of the beam pattern and the resolution of phase angles and amplitudes
- *source openness*: whether the created software and hardware is provided to others as open source
- *extensibility*: the possibility to enlarge the phased array system by coupling multiple devices to each other.

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TABLE I
OVERVIEW OF SELECTED PROTOTYPES OF PHASED ARRAY SYSTEMS THAT WERE DEVELOPED IN ACADEMIC CONTEXT

	Carter [16] Ultrahaptics	**Ochiai [17] Pixie Dust**	**Inoue [18], [19], [20]**	**Marzo [13] TinyLev**	**Marzo [14] Ultraino**	**Beasley [15]**	**Strobino [21]**	**this approach**
year	2013	2014	2016	2017	2017	2019	2019	2019
device(s)	CPLD	FPGA	FPGA	Arduino Nano	Arduino Mega	SoC FPGA	SoC FPGA	FPGA
clock rate	400 MHz	50 MHz	N/A	16 MHz	16 MHz	100 MHz	50 MHz	81.92 MHz
amplifier	N/A	L293DD	NJM2670	L297N	TC4427	TC4427A	MAX17079GTL+	MIC4127
voltage	$\leq 15\,\mathrm{V}$	$\leq 24\,\mathrm{V}$	$\leq 24\,\mathrm{V}$	$\leq 70\,\mathrm{V}$	$\leq 17\,\mathrm{V}$	$\leq 16\,\mathrm{V}$	$\leq 18\,\mathrm{V}$	$\leq 20\,\mathrm{V}$
transducer	320	285	249	72	64	64	88	100
emitting freq.	40 kHz	40 kHz	40 kHz	40 kHz	40 kHz	40 kHz	40 kHz	40 kHz
calculation	SW	HW	HW	HW	SW	HW	HW	SW
interface	Ethernet	USB	EtherCAT	N/A	USB-UART	USB-UART	Avalon®	USB-SPI
update rate	N/A	1 kHz	11 kHz	N/A	$\leq 0.1\,\mathrm{kHz}$	$\geq 6.49\,\mathrm{kHz}$	$\geq 1\,\mathrm{kHz}$	$\leq 1\,\mathrm{kHz}$
phase res.	$\pi/25$	$\pi/8$	N/A	$\pi/12$	$\pi/5$	$\pi/128$	$\pi/625$	$\pi/1024$
amp res.	N/A	3 bit	N/A	fixed	3 bit	fixed	fixed	10 bit
open source	N/A	N/A	N/A	yes	yes	yes	yes	yes
extendable	yes	no	yes	no	yes	N/A	N/A	yes

B. Overview and classification of the approach

This driver board of the FPGA-based phased array system is operated with a clock rate of 81.92 MHz and offers 100 indiviual channels to control transducers emitting at 40 kHz with square-wave signals up to 20 Vpp with $\pi/1024$ phase resolution and 10 bit amplitude resolution. A software calculates the set of phase angles and amplitudes, and transfers it via an USB-SPI interface to the driver board. This interface has a sufficient transmission speed to update the set of transducers on a rate of 1 kHz. In addition, multiple devices can be linked via I^{2}C bus to obtain a considerably larger phased array system.

When comparing the present approach with systems listed in Table I, it can be stated that, for cost-effectiveness reasons, the utilized hardware of the low-cost prototype is not able to keep up with the phased array systems developed by Carter [16], Ochiai [17] or Inoue [18], [19], [20].

However, compared to other proposed low-cost open source systems, the developed prototype has similar performance data, but a higher number of channels as well as a higher phase and amplitude resolution, which is favourable for a higher positional accuracy of the levitating particle. Especially the high amplitude resolution is a particular feature, that is only included in a few systems. This enables the usage of the algorithm proposed by Andersson and Ahrens [22] to generate multiple acoustic traps at different locations without interference. In addition, this feature allows the resulting trapping strength to be adapted to different particle densities [13] and further unneeded individual transducers to be dynamically switched off in order to save energy. The lower update rate compared to the systems proposed by Beasley et al. [15] and Strobino [21] is explained by the calculation platform used (HW vs. SW) and will be discussed in detail in Section II-B.

II. FRAMEWORK FOR ULTRASONIC LEVITATION

A. Design of the phased array system

The framework for ultrasonic levitation is illustrated in Figure 1 and includes a toolbox developed in MATLAB® and the phased array system. The latter consists of a custom-made FPGA-based driver board and a printed circuit board (PCB) on which the transducers (TRANS) and the amplifiers (AMP) are mounted. The PCB and the driver board can be linked via four connectors (CON). To meet various requirements, two PCB layouts for the flat mounting of transducers with diameters of 10 mm and 16 mm as well as an adapter board for arbitrary geometric arrangements were realized.

On the custom-made driver board, a FT2232H chip from FTDI provides both JTAG and USB-SPI interfaces for programming and communication. Due to the usage of the MPSSE engine, the transmission speed is limited to a sufficient maximum of 3.75 MB/s, but compared to faster available interfaces such as Bit Banging (25 MB/s) or the FT245 Synchronous FIFO mode (40 MB/s), only 4 pins instead of 11 or 15 pins are required for data transmission [23].

Lattice's MachXO2 was chosen as FPGA because of its adequate performance and exceptionally low price. Its TQFP-144 package is suitable for hand soldering and offers 114 GPIOs, of which 100 are used in the present work for individual control of the transducers. Other package types like BGA may offer a much higher pin count, but require an expensive multilayer board design and soldering these package types is too demanding and error-prone for rapid prototyping in our labs. On the FPGA, a finite state machine (FSM) written in VHDL interprets the data (d) received from the PC via USB. This data can be forwarded to a wave generator module to generate individual square-wave signals to control the transducers. The excitation of transducers with digital square-waves considerably reduces the complexity of electrical design and is common practice, since their output is almost sinusoidal [24]. In order to minimize the interference between old and new data sets during a receiving process, phase angles and amplitudes are stored in a double buffer structure $(\mathrm{d_{buf}})$ as proposed in [14].

The square-wave signals generated by the FPGA at $3.3\,\mathrm{Vpp}$ are not sufficient to directly drive most of the commercially available transducers that are operated at $\approx 20\,\mathrm{Vpp}$. Hence, it is necessary to amplify them to an appropiate level. For this task, MOSFET gate drivers (AMP) are mainly used in literature (see Table I). Microchip's MIC4127 was chosen because it both allows a comparatively high maximum voltage of $20\,\mathrm{Vpp}$ and is offered in a small MSOP package which is favourable for a compact PCB layout. Other drivers may provide up to $70\,\mathrm{Vpp}$, but require active cooling in long term operation. In addition, many fabricated transducer types are not suitable for such high excitation voltages, as they begin to lose their linear amplitude-to-voltage relationship [13]. Thus, common models for characterizing the behavior of transducers, as described in [25], would no longer be valid, the same applies to the superposition principle to calculate the total acoustic field.

In order to reduce heat development at high excitation voltages close to $20\,\mathrm{Vpp}$, an additional fan was mounted on the driver board. Its PWM-controlled speed can be comfortable adjusted by software (see Section II-B). In addition, the implemented PWM-based control of transducer amplitudes offers a further possibility to limit heat generation. When selecting an appropriate transducer type, there is always a trade-off between quality (e.g. high acoustic output, small amplitude and phase deviation) and cost-effectiveness. Based on a detailed experimental analysis of several transducer types provided by the supplementary information of [13], we decided to use both MA40S4S from Murata and MSOA1640H10T from Manorshi to meet each criteria.

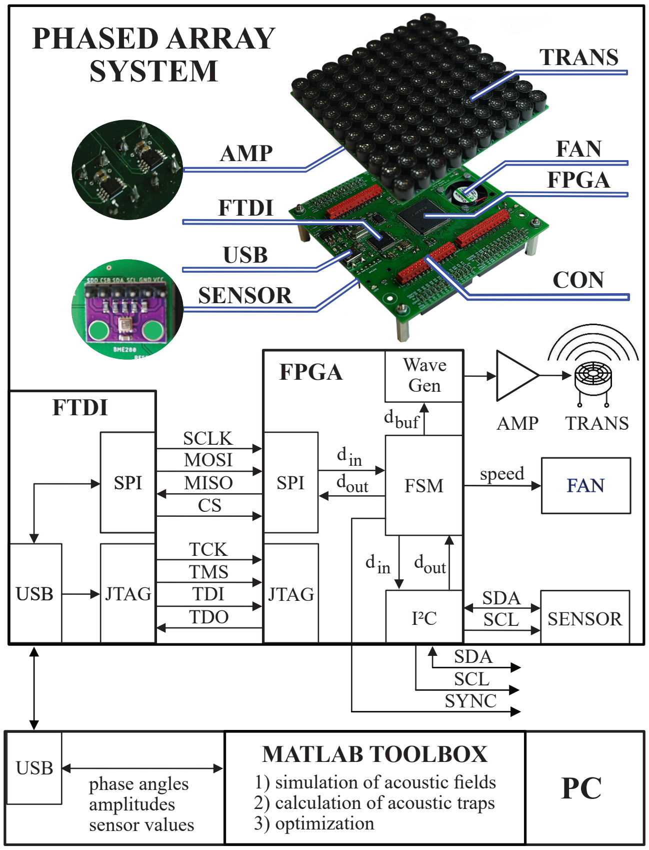

Fig. 1. Overview of the proposed framework for acoustic levitation.

The system further provides an I^{2}C interface, which allows several modules to be linked to obtain a considerably larger phased array system. The bus operates in master-slave-mode and is controlled by the FSM of the I^{2}C master. Via this interface, amplitudes and phase angles can be sent and received by software (see Section II-B) using a simple protocol. In addition to the clock line (SCL) and the data line (SDA), a line (SYNC) has been added that transmits a synchronization signal related to the acoustic frequency of the transducers to avoid beating effects. Thus, the resulting time deviation between the interconnected phased array systems can be minimized to the deviation caused by the different cable lengths, which should be negligible compared to the acoustic frequency of $40\,\mathrm{kHz}$. Although the I^{2}C bus enables a high number of subscribers, it is not recommended to utilize it to its full extent, since the update rate for a new configuration of the overall system should already decrease from $1\,\mathrm{kHz}$ below $0.1\,\mathrm{kHz}$ with more than four linked phased array systems. Furthermore, a humidity, pressure and temperatur sensor (Bosch BME 280) was added to the I^{2}C bus. This sensor is able to measure the three listed quantities with an absolute accuracy of $\pm 3\,\%$, $\pm 1\,\mathrm{hPa}$ and $\pm 1\,°\mathrm{C}$ (range $0 - 65\,°\mathrm{C}$) [26]. The integration of such a sensor is necessary because, in addition to humidity and air pressure, the temperature in particular has a high influence on air density and thus on the speed of sound in the medium. Without consideration and compensation for these quantities, a significant phase drift would occur in the operation of the phased array system, as observed by Beasley et al. [15].

B. Software

In addition to the phased array system, a software has been developed in MATLAB® to control it, see Figure 1. Although MATLAB® is not open source, we chose it because it is part of the standard tools in engineering environment and is preferred for system simulation and control design. The software is able to transmit calculated amplitudes and phase angles via USB-SPI interface to the driver board, as well as to query current sensor values in order to consider environmental influences in the calculation of the wave length and the speed of sound in the medium. The software utilizes models frequently used in the literature, such as in [5] and [25], to describe the characteristics of a transducer and to calculate the resulting acoustic fields. In [5], Marzo et al. presented two methods for the calculation of acoustic traps, namely an approach based on holographic acoustic elements (focus point and specific

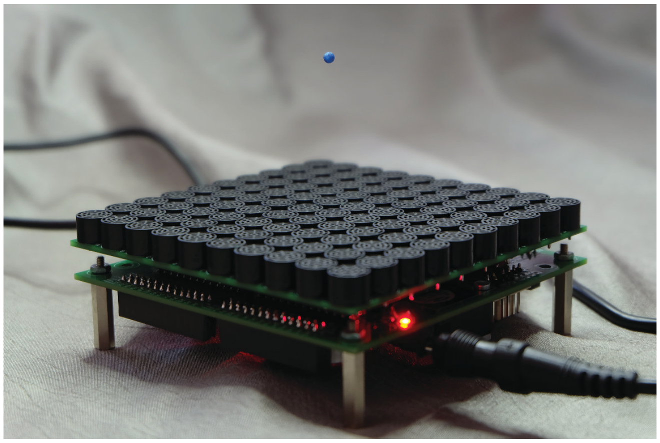

Fig. 2. The created phased array system levitating a blue polystyrene bead ($d = 3\,\mathrm{mm}$) in a twin trap (see Fig. 3) $4\,\mathrm{cm}$ above the center of the device.

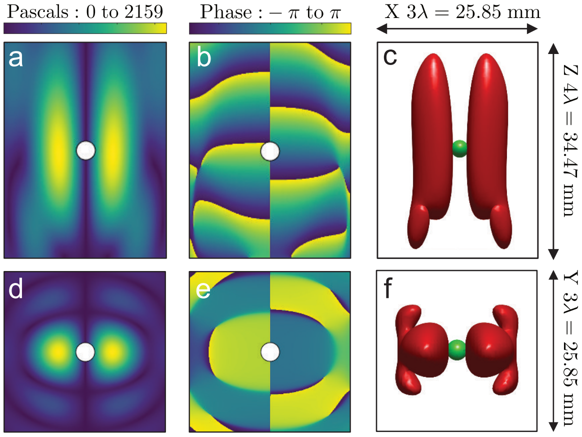

Fig. 3. The simulated fields of the corresponding twin trap. Amplitude field (a,d), phase field (b,e) and amplitude isosurfaces (c,f) of $900\,\mathrm{Pa}$ are shown.

trap signatures) and a generic optimization-based approach. Both approaches were implemented to ensure a high flexibility. While the former is limited to certain conditions, but allows a real-time calculation of phase angles on the FPGA itself as shown in [15] and [21], the latter is more time-consuming and can only be implemented in software. This causes a further delay in the update rate due to the necessary data transfer of the optimization results to the driver board. For this reason, the update rate for software-based approaches is significantly lower than for hardware implementations, as shown in Table I. In contrast, the optimization-based approach is much more versatile and can also be used, for example, for arbitrary geometric arrangements of the transducers. In addition, the optimization-based approach can easily be extended to the algorithm proposed by Andersson and Ahrens [22] by adjusting the quality function of the optimization problem.

III. RESULTS

The developed low-cost phased array system is shown in Figure 2. It operates at a frequency of $81.92\,\mathrm{MHz}$ and controls up to 100 channels simultaneously with square-wave signals up to $20\,\mathrm{Vpp}$ with $\pi/1024$ phase resolution and $10\,\mathrm{bit}$ amplitude resolution. Phase angles and amplitudes and thus the position of the object can be successfully altered with update rates up to $1\,\mathrm{kHz}$. In addition, a software was developed in MATLAB® to simulate acoustic fields, calculate acoustic traps (see Figure 3) and control the device. Besides the custom-made FPGA-based driver board, two PCB layouts for the flat mounting of transducers with diameters of $10\,\mathrm{mm}$ and $16\,\mathrm{mm}$ as well as an adapter board for arbitrary geometric arrangements of the transducers were realized.

IV. DISCUSSION

The proposed system features a custom-made FPGA-based driver board instead of a proprietary development board like in [15] or [21] in order to maximize the number of channels that are available for the individual control of the transducers. The downside for this approach is the increased complexity in the overall assembly of the driver board. In addition, the use of a software-based (and optional optimization-based) approach to calculate amplitudes and phase angles reduces the maximum update rate significantly, but provides a high degree of flexibility. Furthermore, the extension of the overall system via the $\mathrm{I^2C}$ interface is not suitable for connecting a large number of phased array systems without reducing the update rate. This problem could be solved by using a dedicated FPGA board for communication in a star topology via a faster interface. In addition, the current system does not provide measurement of the object position of the particle. In order to achieve a closed loop control, the use of a depth camera (Intel RealSense D415) is currently being tested. The images are evaluated by a custom software written in C++ using OpenCV libraries and the determined position is transferred to the software in MATLAB® via a socket connection. In initial tests, the position of the particle was determined with accuracies in the sub-millimeter range at sampling rates of up to 30 frames per second. Another possibility is the interesting approach proposed by Beasley et al. [15], in which additional transducers are used as receivers to determine the position of the object by measuring the echo signal from the particle. Although this approach offers a significantly higher sampling rate, the accuracy with which one or even several object positions can actually be determined remains unclear.

V. CONCLUSION AND FUTURE WORK

In the present work, we have described an FPGA-based phased array system for the acoustic levitation of small objects. The software als well as the hardware which were created in this project will be provided as open system in order to encourage further research in the scientific field of acoustic levitation. The next steps include the integration of the depth camera in the overall system and the design and testing of a suitable position control loop.

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