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Low-Jitter Systems Synchronization for Doppler Measurements

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***Abstract*—In some Doppler laboratory measurement, more instruments need to work together. In some cases, a signal generator produces the excitation bursts, while echoes from fluid are sampled by a separate card. In another significant case, the thousands of elements of a 2D array probe are partitioned among different echographs or sections of a complex system. Synchronization of instruments that do not share a common clock is an issue. A Pulse Repetition Interval (PRI) sync signal can be distributed to the equipment, but the jitter produced when the signal is sampled by the individual clock of each instrument results in unbearable noise in the Doppler analysis. In this work, a method that reduces this jitter to less than 100ps rms is presented. The proposed method was implemented in a FPGA of a custom Doppler board. Experiments performed by investigating a 0.5 m/s flow in an 8 mm pipe show that the proposed method can synchronize a Doppler system to an asynchronous trigger without degradation of the measured Doppler spectrum.**

Keywords— Jitter reduction; frame jitter; FPGA; dynamic phase shift; PLL.

I. INTRODUCTION

In ultrasound Doppler flow investigations sinusoidal bursts of energy are transmitted every Pulse Repetition Interval (PRI). The target displacement among subsequent pulses produces shifts in the echo sequence that are related to the target velocity. The receiver detects and processes such shifts to obtain the flow velocity. If the burst sequence period, PRI, is affected by a temporal jitter, i.e. each PRI length changes by a small random value, a corresponding error in the target shift is measured in the receiver. The result is a background noise in the Doppler spectrum that can prevent a correct velocity measurement. This kind of jitter, where the whole echo data frames are randomly translated one with respect to the others, is known as frame jitter [1], and differs from the typical data jitter that applies to each single sample [2]. Doppler applications are quite sensitive to frame jitter, and a frame jitter higher of 100ps rms produces notable noise and artefacts in the Doppler spectrum.

Frame jitter can be present in Doppler laboratory tests that exploit separate instruments or systems working together on the same acquisition. In a possible scenario, a waveform generator produces the transducer excitation when triggered by the PRI pulse generated by a separated acquisition card that saves the received echoes. A commercial high-end waveform generator, like, e.g. 33612B (Keysight Technologies Inc. Santa Rosa, CA, USA) declares in the documentation [3] a 2.5 ns rms jitter in the trigger input, which results in an intolerable frame jitter in the Doppler measurements. In a different scenario 4 256-channel echographs work together to manage a 1024-element probe [4]. If the echographs, each working with its own internal clock f_{ck}, would have been synchronized by distributing a common PRI pulse, the frame jitter would have resulted in [1]:

$$\sigma_f = \frac{1}{f_{ck}\sqrt{12}} \qquad (1)$$

For example, a f_{ck}=100MHz produces a 2.9 ns rms jitter, clearly too high for Doppler applications. In [4] the problem was solved by distributing a common clock reference to all the echographs. However, distributing the master clock can be quite difficult, and often commercial instruments or systems do not allow a direct access to the system clock.

In this work, a full digital synchronization method is presented that reduces the frame jitter to less than 100 ps rms when triggered by an asynchronous PRI pulse. The proposed system was integrated in a Field Programmable Gate Array (FPGA) and tested in a Doppler system [5] designed for fluid characterization [5]. Experiments show how the proposed method, when triggered by an asynchronous PRI, produces Doppler images similar to the reference, obtained with a synchronous PRI.

II. METHOD

The proposed Synchronization Circuit (SC) is integrated in an Altera-Intel Cyclone III FPGA. The SC architecture is shown in Figure 1. The "PRI Pulse" signal feeds a Tapped-Delay-Line (TDL), which is a structure typically employed for the measurement of sub-ns temporal intervals in Time-to-Digital converters [7]. Here, every PRI pulse, the TDL measures the temporal difference between the PRI edge, and the edge of the main FPGA clock, CLK. The result is presented as a thermometric code containing a '1' for each delay cell that was crossed by the PRI pulse before CLK edge. An encoder converts the TDL output in a binary code. The controller, CTRL, uses this measurement to tune the phase of the CLK_{ph} PLL output so that it is aligned to the PRI pulse. This is achieved by changing the PLL settings on-the-fly through the PLL "Dynamic Shifting Interface" (DSI) [8]. In summary, the result of these operations is that, every PRI pulse, the CLK_{ph} output is aligned on-the-fly to the incoming PRI pulse edge. The aligned CLK_{ph} can then be

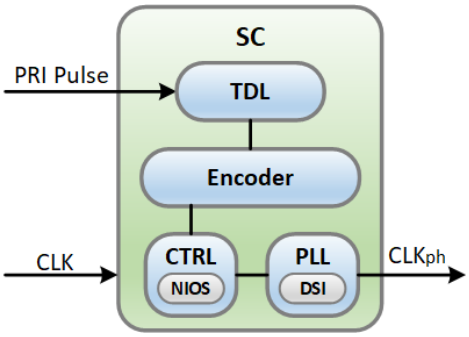

Figure 1. Architecture of the proposed Synchronization Circuit. It includes a Tap-Delay-Line (TDL), an Encoder, a control (CTRL) and Phase-Locked-Loop (PLL) units.

used to feed a Doppler transmission (TX) and/or reception (RX) section.

In the following section, a brief description of the main components of the SC is reported.

A. TDL and Encoder

A TDL is composed by an array of elements, each constituted by a delay cell and a register, as sketched in Figure 2 (middle). The delay of the TDL elements realizes a delay line (D_1-D_N), which the PRI Pulse propagates in. At the CLK edge, the status of the propagations is stored in the register array. Thus, at the first rising edge of CLK after the PRI Pulse edge has entered the TDL, the TDL Status identifies how many delay elements have been crossed. For instance, in Figure 2 (top), the 1-0 transition is between the D_3 and D_4 delay elements, as shown in the TDL Status register that has the 4 LSBs at 1. From the status we read that 4 delay elements have been crossed. If the delay D_i of each cell is known, it is possible to estimate the delay t_j between the PRI Pulse and the CLK edges.

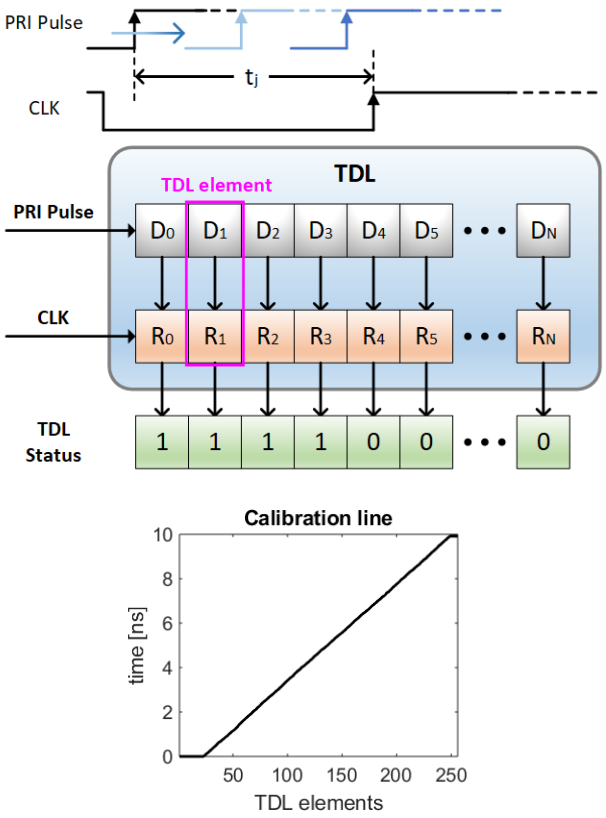

Figure 2. Pulse propagation (Top) in the Tapped-Delay-Line (Middle) and its calibration line (Bottom).

TABLE I
IMPLEMENTATION PARAMETERS

Parameter	Value
TDL	
Delay Elements	256
Mean Delay	45 ps
Total delay	11.52 ns
PLL	
TDL clock	100 MHz
VCO Frequency	600 MHz
Shift resolution	210 ps
DSI	
DSI clock	200 MHz
Time per Step	25 ns
Max Step number	48

The values of the delays D_i are quantified through a statistical calibration process [9], performed by the CTRL block of Figure 1, which include a NIOS II soft processor (see next section). At system startup, an asynchronous signal is internally routed in the PRI Pulse input, and hundreds of measurements are automatically performed and stored. Since the probability of getting a hit in a particular delay cell is related to the delay of the cell, it is possible to estimate the delays D_i. According to this procedure, based on the stored measurements the NIOS II soft-processor elaborates a calibration line [9], like the one shown in Figure 2 (bottom).

In the presented implementation we employed CLK of 100 MHz. Thus, the temporal difference between the PRI Pulse and CLK edges can range in 10 ns interval. The TDL should feature a number of elements suitable to span an interval a bit greater than 10 ns. This grants not to fail hits near the interval borders. The mean delay value of the implemented TDL elements was estimated through the statistical approach, and corresponded to 45 ps. This value allows to cover a temporal interval of 10 ns (i.e. the CLK period) with at least 223 TDL elements. Employing 256 elements ensured to cover a time interval of 11,5 ns. Figure 2 bottom shows the calibration line of the implemented TDL. The mean delay value of is 45ps and the standard deviation of the delay elements was 6.9 ps.

B. CTRL and PLL

The CTRL block manages all of the circuit operations. It embeds some custom VHDL blocks, a NIOS II soft-processor and an on-chip RAM, where the calibration line is stored. As previously said, the CTRL block handles the TDL calibration process, starting the calibration procedure, saving the corresponding TDL Status registers and elaborating the data. Once the calibration line has been calculated, it is stored in the dedicated RAM to be used for t_j measurement during the run-time operations.

The CTRL block also handles the PLL phase shifting through a dedicated serial interface, called "Dynamic Shifting Interface" (DSI) [8]. DSI lets to dynamically change the PLL outputs phase without losing the lock condition. The interface has a dedicated clock (up to over 200 MHz for the Cyclone III devices) and requires 5 clock cycles for each phase shift step. Every shift, it is possible to select the output to be shifted and the shift direction (up/down). The shift resolution res_{PhS} is related to the Voltage-Controller-Oscillator (VCO) frequency f_{VCO} by:

$$res_{PhS} = \frac{1}{8 \cdot f_{VCO}} \qquad (2)$$

In this implementation the PLL was set with a f_{VCO} of 600 MHz and a DSI clock of 200 MHz. According to (2) The res_{PhS} was about 210 ps. The f_{VCO} value affects the shift resolution and consequently the shifting time. For instance, with res_{PhS} = 210 ps, shifting the CLK_{ph} of, e.g., 2.5 ns, takes 12 shift steps; to span a 10 ns range, 48 shifts are required. Thus, the phase alignment lasts 1.2 µs in the worst case.

III. Experiments and Results

The proposed synchronization circuit was implemented in the Cyclone III [8] family (Altera-Intel, Santa Clara, CA USA) of the Doppler board described in [5]. Experiments include the quantification of the residual jitter present after the proposed synchronization technique, and the evaluation of the Doppler image quality in presence of such residual jitter.

A. Jitter performance of the synchronization circuit

The experimental setup employed in this test is reported in Figure 3. The function generator produced sinusoidal bursts composed by 7 cycles at 5 MHz with a PRI of 200 µs. The function generator issued also the PRI Sync, synchronous with the burst start, that was used as trigger for the Doppler system, where the proposed circuit was implemented. The Doppler system acquired and stored 4096 bursts triggered by the PRI Sync. The test was repeated with the synchronization circuit active and by-passed, and results were compared by elaborating data in Matlab (The Mathworks, Natick, MA). The phase of each burst was quantified by taking the phase of the peak of the spectrum amplitude obtained by a Fast Fourier Transform (FFT). The jitter was evaluated by calculating the differences among these phases.

TABLE II. Synchronization Circuit (SC) Performance

Measurement Condition	Frame Jitter	
	Peak-to-Peak (ps)	*RMS (ps)*
SC OFF	10021	2884
SC ON	563	91

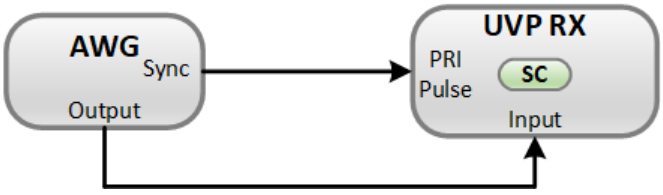

Figure 3. Experimental setup for the quantification of the jitter performance in the proposed synchronization circuit.

Results are summarized in Table II. When the synchronization circuit is by-passed (top row), the jitter is about 10 ns peak-to-peak, corresponding to the system clock period, as predicted by (1). When the synchronization circuit is activated (bottom row), the jitter drops below 600ps peak-to-peak corresponding to 91ps rms. In this condition the proposed circuit reduces the jitter more than 17-fold.

B. Doppler imaging improvement

This test aimed to evaluate how the reduction of the frame jitter carried out by the proposed circuit contributes to improve the quality of the Doppler analysis. The test was divided in 3 experiments, and Figure 4 shows the setups employed in each experiment. In the first test the Doppler system [5] was used to investigate a 0.5 m/s flow in an 8 mm pipe of a laboratory flow-rig. The Doppler system managed both transmission and reception, so minimal frame jitter was expected, and results are used as reference. Acquired data were processed through coherent demodulation [10] and spectral analysis to obtain the Doppler spectral matrices [11]. Each row of the matrix represents a depth, and is composed by the Doppler power spectral density, represented in color code. Figure 5, top reports the Doppler spectral matrix for this experiment. The parabolic

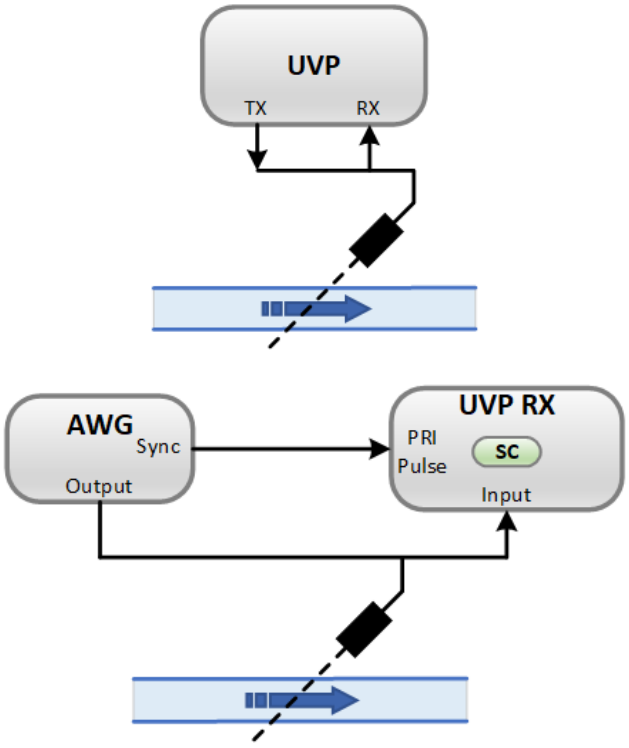

Figure 4. Experimental setup employed in the test of the quality of the Doppler spectral matrices. A reference image was obtained (top), and compared with images calculated from and asynchronous PRI pulse with the proposed circuit active and inactive (bottom).

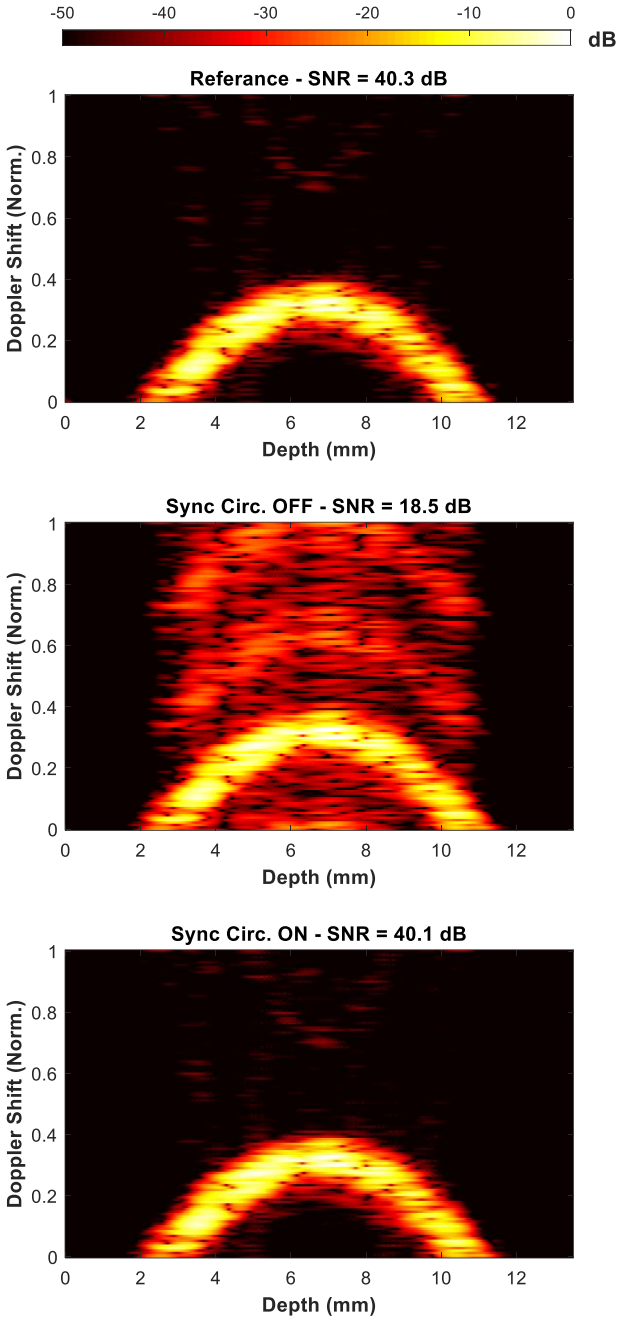

Figure 5. Power spectral density matrices for the Doppler signal. Depth and frequency normalized to 1/PRI are reported in horizontal and vertical axes, respectively. Power is color code in a 50dB dynamics. Top: reference matrix measured with no jitter. Middle: matrix in presence of jitter and proposed circuit not active. Bottom: in presence of jitter and proposed circuit active.

profile developed by the flow is clearly visible. A Signal-to-Noise-Ratio (SNR) of 40.3 dB was calculated. In the second experiment (Figure 4, bottom), the Keysight 33500B function generator excited the transducer with the same bursts sequence used in the first experiment, while the Doppler system acquired the echoes, triggered by the PRI Sync produced by the function generator. The trigger was sampled by the Doppler system with a 100 MHz clock and the synchronization circuit disabled, thus a 10 ns peak-to-peak jitter was present. Acquired data were elaborated to obtain the Doppler spectral matrix, shown in Figure 5, middle. Due to the high frame jitter, artefacts are visible in the background. The reduction of the image quality is confirmed by the decrease of the SNR, now reduced to 18.5 dB. The last experiment was carried out like the previous one, but with the synchronization circuit active. The spectral matrix is reported in Figure 5, bottom. The artefacts are not visible, and the image quality is qualitatively similar to the reference of Figure 5, top. This result is confirmed by the SNR of 40.1dB, comparable to the 40.3 dB of the reference image.

IV. Conclusions

In this work, a full digital synchronization method capable of significantly reducing the frame jitter, was presented. The method can be implemented in FPGA, and its performance was shown suitable for research Doppler applications [12]. The employment of this technique can simplify the synchronization of complex ultrasounds systems, or it can be used in experiments where more separated instruments works jointly.

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