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Wafer Level Characterization of Row-Column Addressed CMUT Arrays

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***Abstract*—This paper presents a measurement methodology for wafer level characterization of row-column addressed (RCA) capacitative micromachined ultrasound transducers (CMUT). Characterization of a 62+62 element RCA CMUT is presented. To facilitate wafer level electrical characterization measurements between adjacent electrodes can be used to characterize the device. This allows for determination of the individual element capacitance. Current-voltage measurements between adjacent top or bottom electrodes provides valuable information about process yield.**

I. Introduction

Row-Column Addressed (RCA) capacitive micromachined ultrasonic transducers (CMUTs) are an attractive alternative to fully-populated matrix arrays, as they provide volumetric imaging with a greatly reduced number of electrical connections [1], [2]. Furthermore, they can be mass-produced on wafer scale using silicon process technology which allows for tight control of the dimensions. RCA CMUTs have been fabricated using various fabrication techniques including fusion bonding, anodic bonding and surface micromachining. Several devices have been presented including a 32+32 RCA CMUT chip based on a fusion bonding process with silicon nitride [3], a RCA CMUT chip fabricated using a surface micromachining process [4], a 32+32 anodically bonded RCA CMUT chip [5], a BCB based RCA CMUT chip [6], a 62+62 fusion bonded RCA CMUT probe [7], and a 120+120 element RCA CMUT probe fabricated using sacrificial release microfabrication [8]. As the resolution of the RCA transducer scales linearly with the number of elements the current trend is to increase the number of elements and fabricate large area chips.

In this work we present wafer level characterization of a local oxidation of silicon (LOCOS, origanally used by [9] for CMUTs) based 62+62 element RCA CMUT transducer as shown in Fig. 1. Manual electrical characterization of a transducer having 124 element becomes a tedious job and automated tests need to be implemented on wafer scale, i.e. electrical wafer level test can be used to ensure that only fully functional arrays are used for probe manufacturing and to provide valuable information during process optimization.

Conventional linear arrays are easily characterized electrically using the two terminals on the device, e.g. the capacitance of an element can be measured directly using the two terminals of the element. However, RCA arrays cannot be measured in the same way as e.g. a measurement of the capacitance of a row-element will require that all columns are shorted and vice versa. This is not easily done on commercial wafer probers where micro manipulators are used to place probe needles or a probe card in fixed positions. During wafer level characterization the probe needles remain fixed and the wafer is automatically moved to perform the measurements needed. The objective of this work is therefore to present a methodology for characterization of RCA CMUT arrays with the aim of providing an automated and non-destructive wafer level test to determine if an array is fully functional or not.

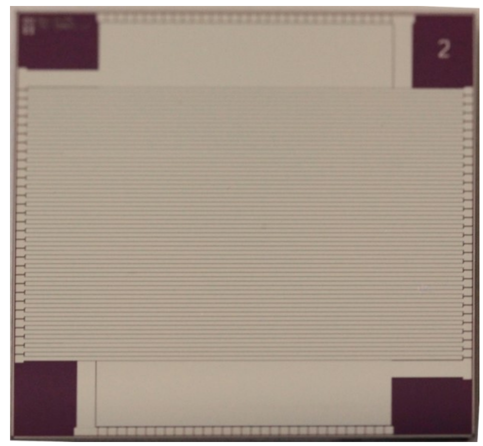

Fig. 1. Image of the 62+62 RCA CMUT chip

The article is organized as follows: First, the measurement methodology is described. Then, the experimental details of the wafer level electrical characterization is given. Finally, the article ends with conclusions.

II. CMUT characterization methodology

The characterization methodology is illustrated in Fig. 2. Two fixed probes, $P1$ and $P2$, are used to connect two neighboring top electrodes (e.g. rows $R2$ and $R3$) to the measurement equipment.

In a typical situation a range of electrical measurements are performed:

1) Current voltage (IV) measurements are made to determine if adjacent top or bottom electrodes are short circuited due to e.g. problems during fabrication.
2) Impedance frequency (Z-f) measurements are performed to determine the frequency for capacitance voltage (CV) measurements and investigate the characteristics of the transmission line.

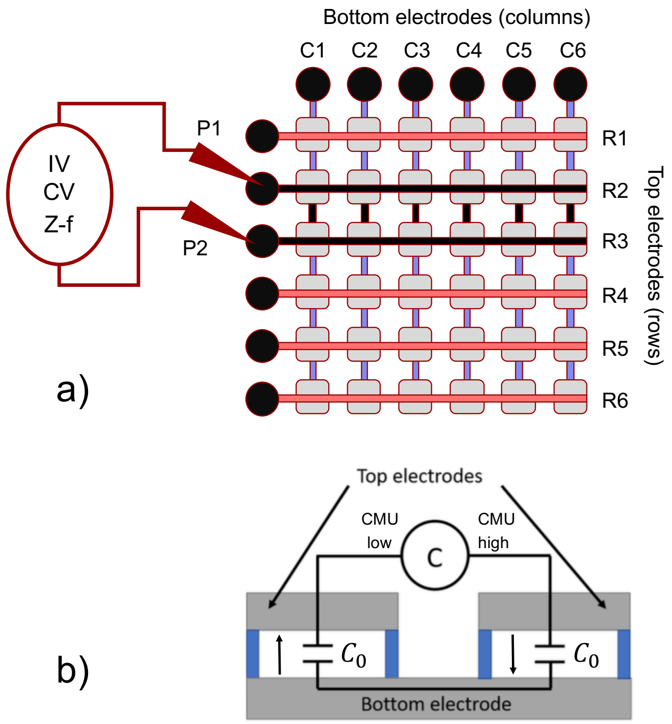

Fig. 2. a) Illustration of the measurement of the capacitance between two neighboring top electrodes, $R2$ and $R3$ using two probes, $P1$ and $P2$. b) The bottom electrodes, $C1$ to $C6$, effectively connect the CMUT cell capacitors in $R2$ in series with the cell capacitors in $R3$. The measured capacitance is therefore $C = C_0/2$. The arrows show the direction of the electric field in the CMUT cavities. The electric field points in opposite directions.

3) CV measurements are used to verify the electro mechanical behavior of the elements which is seen as a parabolic CV curve.

Once the measurement is completed the wafer is moved to allow the fixed probes to connect to e.g. $R3$ and $R4$ and this procedure is then repeated until all elements have been measured. When all rows have been characterized the procedure is repeated on the columns. This allows to determine the electrical characteristics of the array and identify defective elements.

During impedance measurements, the bottom electrodes, columns $C1$ to $C6$, effectively connect the CMUT cell capacitors in $R2$ in series with the cell capacitors in $R3$ as illustrated in Fig. 2b). Ignoring electrode resistance [10] and substrate coupling [11] the measured capacitance, C, is therefore

$$C = \frac{C_0}{2}, \quad (1)$$

where C_0 is the capacitance of a single row element. In this way the element capacitance can be estimated on wafer scale.

The electrical measurements allow to determine if the elements of the array perform as expected and process errors can be detected as abnormal electrical behavior indicating a faulty element. For example, if two neighboring rows are not completely separated during element etching, as illustrated on Fig. 3, the IV measurement will show that the elements are short circuited and impedance measurements, used to calculate the capacitance, will show both a small resistance and phase angle. Likewise, the capacitance between the short circuited elements and a neighboring element will represent a series coupling of $2C_0$ and C_0, i.e. the measured capacitance is (again ignoring substrate coupling) $C = 2C_0/3$. In general, the capacitance between m short circuited elements and n short circuited elements will be

$$C = \frac{mn}{m+n} C_0. \quad (2)$$

Thus, also the capacitance between two neighboring elements can reveal structural defects.

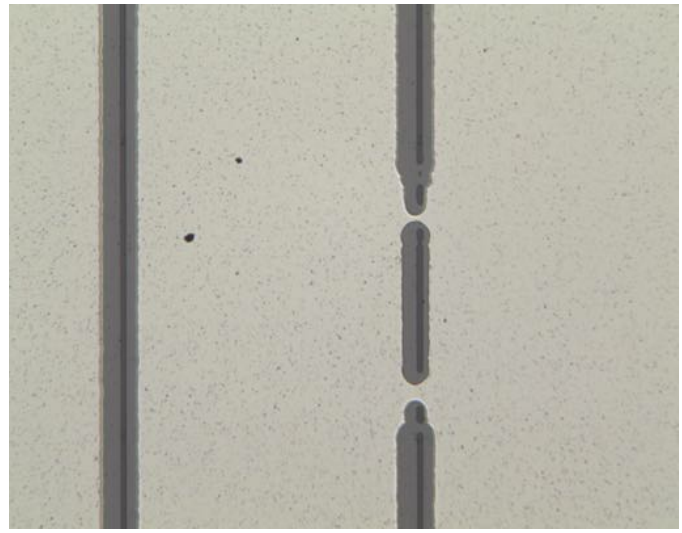

Fig. 3. Short circuit between two adjacent top electrodes (rows).

III. Experimental

The methodology for wafer level characterization of CMUTs relies on a semi-automatic wafer prober and IV, CV and Z-f are the basic tests performed. These measurements were performed on a 62+62 RCA CMUT array from the same wafer as the array described in [12], however, a chip with lithographic errors possessing dielectric charging was selected to demonstrate the possibilities of wafer level test. A Cascade 12K Summit semi-automatic wafer prober and a KEYSIGHT B1500A Semiconductor Device Parameter Analyzer equipped with a B1520A multi frequency capacitance measurement unit (CMU) and six source measurement units (SMU) for IV measurements were used. The KEYSIGHT B1500A is connected to the probe manipulators using a SMU-CMU unify unit (SCUU) which allows to automatically switch between current-voltage and capacitance measurements. The measurement system is also equipped with a guard switch unit (GSWU) which is used for an accurate impedance measurement by connecting the guard lines between CMU high and low near the CMUT. The electrical measurements were performed between neighboring bottom or top electrodes.

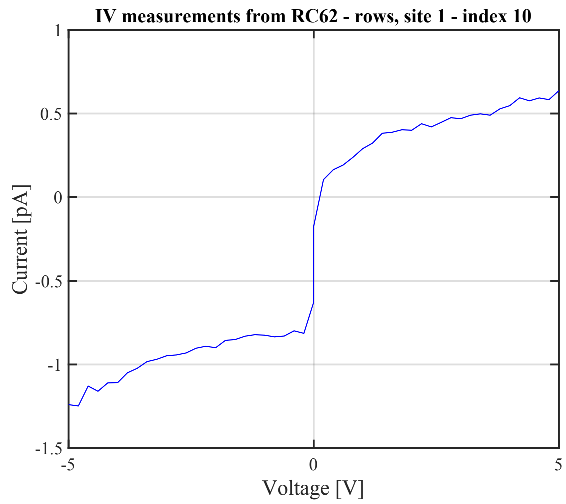

Fig. 4. Typical current-voltage measurement between adjacent row elements show a leakage current in the pA range.

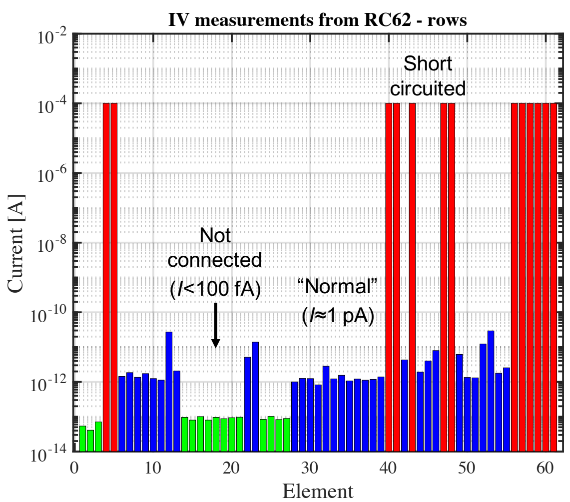

Fig. 5. Plot of the maximum current for each adjacent row elements determined from IV measurements as shown on Fig. 4. The blue bars show normal functioning elements. The red bars indicate elements that are shorted, and the green bars show elements that are not connected.

A. IV characterization

Fig. 4 shows the IV curve measured between two adjacent row elements on the 62+62 RCA CMUT array. The currents is as expected very low, in the pA range, corresponding to a large electrical resistance of around 10 TΩ. Such IV measurements were performed between all adjacent elements in the array and the maximum current was extracted and the result is shown on Fig. 4. The plot reveals three categories of elements. The blue bars show normal functioning elements where the current between adjacent rows is around 1 pA. The red bars indicate elements that are shorted leading to a high current. The reason for the short circuited elements were found to be errors in the definition of the top electrodes as show on Fig. 3. Finally, the green bars show elements that are not connected leading to a very low current on the order of fA. The reason for this error was in all cases found to be an over etch of the aluminum electrode close to the bonding pad leaving the element without connection to the bond pad as illustrated in Fig. 6. Thus, IV measurements are very well suited for process control and can be performed on both top (row) and bottom (columns) electrodes.

Fig. 6. Bond pad and row element not connected due to errors in the lithographic process.

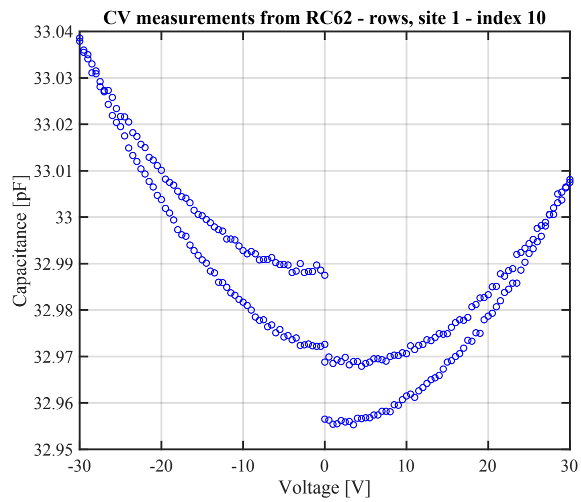

Fig. 7. Capacitance-voltage measurement between adjacent row elements. The CV curve reveals dielectric charging.

B. CV characterization

Fig. 7 shows a typical CV curve as measured on the RCA CMUT chip shown on Fig. 1. The CV curve is parabolic as expected for a CMUT where the applied voltage decreases the gap in the CMUT cells leading to an increasing capacitance. It is noted that the CV curve has hysteresis indicating dielectric charging. Measurements on linear test elements has shown

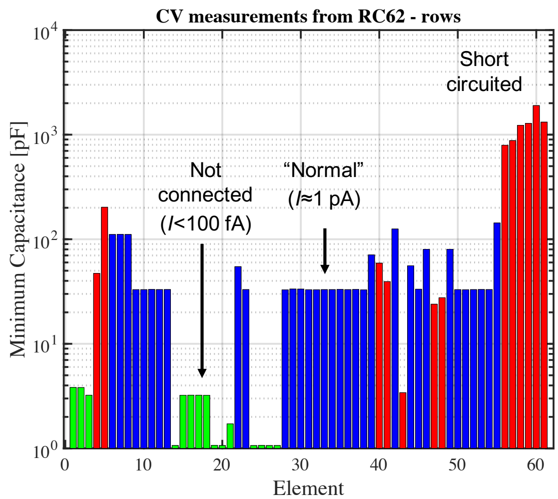

Fig. 8. Plot of the minimum capacitance for each adjacent row elements determined from CV measurements as shown on Fig. 7. The blue bars show normal functioning elements having a capacitance around 30 pF. The red bars indicate elements that are shorted so the capacitance cannot be determined. The green bars show elements that are not connected where the capacitance is around 1 pF.

that the device is electrically stable for one bias polarity. That the charging behavior is observed for *both* voltage polarities is because that measuring between adjacent electrodes means that the electric field in the CMUT cavities of the two elements always points in opposite directions as illustrated in Fig. 2. CV measurements were performed between all adjacent elements in the array and the minimum in capacitance was extracted and the result is shown on Fig. 7. The capacitance of the normal functioning elements is around 33 pF. The capacitance measured between elements which are shorted to neighboring elements is higher as the area of the elements are larger. CV measurements can also be performed between adjacent bottom electrodes.

IV. Conclusion

This paper presented a measurement methodology for wafer level characterization of RCA CMUTs. To facilitate automated wafer level tests, electrical measurements were performed between adjacent top (rows) or bottom electrodes (columns). IV measurements between fully functioning elements showed a maximum current in the pA range. It was found that short circuited elements and elements that are not connected to the bond pads can be be identified electrically. The reason for the errors was found to be related to the etching process used for definition of the top electrodes. CV measurements allowed to determine the element capacitance as this is approximately twice the measured capacitance. When CV measurements are performed between adjacent electrodes the electric field has opposite directions in the two elements and if dielectric charging is present it will show up in the CV curve for both polarities even if the device is stable in one voltage polarity. In conclusion, wafer level characterization of RCA CMUT devices is a valuable tool for selecting the best performing chips and to assist in process optimization.

V. Acknowledgement

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