# 188+188 Row–Column Addressed CMUT Transducer for Super Resolution Imaging

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Abstract—A capacitive micromachined ultrasonic transducer (CMUT), 8 MHz resonance frequency,  $\lambda/2$  cell pitch 188+188 row-column addressed (RCA) array for super resolution imaging is presented. The top- and bottom electrode design features a zig-zag shaped pattern to increase the active cell area for fixed plate thicknesses. The RCA CMUT has been fabricated utilising a deposit, remove, etch, multistep (DREM) process to fully separate the bottom electrodes electrically as well as anodic bonding the array to an insulating borosilicate glass wafer. Linear test elements have been characterized. Electrical measurements show a center frequency of approximately 5.5 MHz and a coupling coefficient of 7.8% for -80 V DC bias and 50 mV AC. Acoustic measurements made in immersion with a single cycle 4 MHz pulse with a -90 V DC bias demonstrate that the fabricated CMUT arrays can emit broadband ultrasound pulses.

### I. INTRODUCTION

The number of interconnections required to perform 3D ultrasound imaging can be greatly reduced by applying a rowcolumn addressed (RCA) scheme compared to a conventional fully populated matrix (FPM) array [1]–[6]. Conventional FPM arrays require  $N^2$  interconnects, where N is the number of elements in the elevation and azimuth direction. By applying a RCA scheme the same number of channels can be obtained by only 2N interconnections. However, the resolution capability is proportional with N, and it is therefore desirable to design 3D transducers with as many channels as possible. The linear scaling law of RCA arrays facilitates 3D transducers with a high number of channels, that otherwise would be exceedingly impractical for FPM arrays. The high achievable resolution with the RCA scheme can be utilized in super resolution imaging to more precisely determine the positions of injected micro bubbles in vascular structures.

This work presents the development of a 188 + 188 element RCA transducer array based on the capacitive micromachined ultrasonic transducer (CMUT) technology. The CMUT cavities are defined by a local oxidation of silicon (LOCOS) [7] process and a deep silicon etch combined with a silicon etch back and an anodic bonding of a glass wafer are utilized to define the bottom electrodes. This process therefore only utilizes one SOI (Silicon On Insulator) wafer for the top plate, and a standard silicon wafer for the bottom electrode. The LOCOS process allows for tightly controlled CMUT cell dimensions and welldefined cavity depths due to the predictability of the grown



Fig. 1: Sketch of a 4+4 row-column CMUT array structure where both the bottom and top electrodes are designed with a zig-zag shaped pattern, with the cells positioned in the overlapping segments.

oxide thicknesses. This technique combined with the advantage from a deposit, remove, etch, multistep (DREM) process and anodic bonding results in that the substrate coupling, which would otherwise lower the receive sensitivity of the bottom electrodes, are avoided as the glass wafer is insulating [8].

## **II. DESIGN & FABRICATION**

## A. Design

The RCA CMUT array is designed having 188+188 elements with a pitch of  $\lambda/2$  (95 µm), an operating frequency of 8 MHz, and a plate thickness of 3 µm. The wafer layout also includes linear CMUT arrays for testing with a slightly different pitch and radii compared to the RCA CMUT arrays. The CMUT cells are designed to be 50 µm wide whereas the linear test elements used in this work are 70 µm wide. The pull-in voltage is designed to be at 220 V. The row and column design for this chip has a zig-zag pattern (illustrated in Fig. 1) to increase the active area of cells for a fixed plate thickness with a factor two compared with a typical straight row-column design [9].

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## B. Fabrication

The fabrication of the CMUT array is based on the LOCOS process, a DREM trench etch process and two bonding steps (fusion and anodic bonding). The LOCOS process is a well known method where a silicon substrate is masked off, blocking the diffusion of oxygen, and selectively oxidized. The masking material used is silicon nitride,  $Si_3N_4$ .

In this work, a combination of a long DREM etch, a backside etch of silicon, and an anodic bonding of a borosilicate glass wafer is performed to separate the bottom elements electrically and to avoid capacitive substrate coupling. The DREM etch is similar to a conventional Bosch process but consists of three finely tuned steps which to a higher degree preserves the deposited fluorocarbon layer everywhere except in the bottom of etched trenches. This process protects the masking material resulting in an infinite selectivity, creating uniform etching scallops of the sidewalls and facilitates deeper etches [10].

The fabrication process for the RCA CMUT array is similar to previous presented processes [11] and all the steps are carried out in the cleanroom at DTU Nanolab. The main steps which are in focus in this work are illustrated in Fig. 2.

The starting point to arrive at step 1, is a silicon wafer with a resistivity of  $<0.025 \,\Omega \,\mathrm{cm}$ , which is thermally oxidised at  $1100 \,^{\circ}\mathrm{C}$  under dry conditions to grow a  $400 \,\mathrm{nm} \,\mathrm{SiO}_2$  layer. This is followed by a deposition of a  $55 \,\mathrm{nm}$  stoichiometric  $\mathrm{Si}_3\mathrm{N}_4$  layer and a  $100 \,\mathrm{nm}$  polycrystalline silicon layer in LPCVD (Low Pressure Chemical Vapour Deposition) furnaces. The polysilicon layer and subsequently the silicon nitride layer are patterned with a photolithographic process combined with dry and wet etching, leaving silicon nitride as masking pads on silicon oxide where the CMUT cavities will be formed.

From this step the wafer is again patterned to open up the silicon oxide, exposing the silicon substrate. The DREM etch is then performed at a temperature of -19 °C using a reactive deep ion etching (DRIE) tool, capable of performing this modified Bosch process, for a final depth of  $110 \,\mu\text{m}$ .

The result is a structure similar to step 1 in Fig. 2, where a  $45^{\circ}$  cross-section of the structure illustrated in Fig. 1 is shown. Depicted are four (black) silicon nitride pads used in the LOCOS process which have been structured on (dark gray) silicon oxide on (gray) silicon. The 110 µm deep DREM etch into the silicon is separating the cells into groups of two. Fig. 3 shows a cross-sectional scanning electron microscope (SEM) image of two etched DREM trenches in silicon, with a depth of 113 µm.

A thermal oxidation is performed under wet conditions at  $1100 \,^{\circ}$ C for a total post SiO<sub>2</sub> thickness of around 840 nm, forming the CMUT cavities (step 2). A SOI wafer is direct bonded by fusion bonding to the structure in step 2 to enclose the cavities (step 3).

To fully separate the bottom electrodes, the wafer stack is flipped and dry etched by a RIE process from the backside, thinning down the substrate by  $\approx 400 \,\mu\text{m}$ . The wafer backside after etching can be seen in the microscope and SEM image in Fig. 4 and 5a respectively. It can be seen from the image,



Fig. 2: Cleanroom fabrication process for the row-column CMUT array. Only the processes comprising the DREM etch, LOCOS oxidation and fusion- and anodic bonding are depicted.

that the dry etching process has etched past the extend of the original  $113 \,\mu\text{m}$  trench, exposing the oxide covering the inside of the trench. These zig-zag oxide structures are left standing due to the high selectivity of silicon to silicon oxide.

To reduce the roughness of the backside surface for anodic bonding and remove the  $SiO_2$  structures present in Fig. 4, the wafer is polished using a Logitech CM62 Orbis CMP (Chemical Mechanical Polishing) machine [12], the result is shown in Fig. 5b.

A borosilicate glass wafer is then bonded by anodic bonding to the backside at a temperature of  $350 \,^{\circ}\text{C}$  using a three step voltage ramp ( $300 \,\text{V}/600 \,\text{V}/800 \,\text{V}$ ). The handle- and BOX layers are then removed from the SOI wafer by dry etching (step 6) leaving the top plate bonded to the cavities. To finalise the CMUTs, first, access to the bottom substrate electrodes are etched through the plate and post SiO<sub>2</sub> by using a patterned hard 100 nm thick aluminium mask. Then, after removing the mask, the top- and bottom electrode contact pads are metallised by depositing and patterning 400 nm aluminium, as well as the underlying silicon by a RIE process. The RCA CMUT arrays are then diced from the wafer.

## **III. CHARACTERIZATION**

## A. Electrical

The electrical response of the CMUT array has been tested by performing impedance measurements on a linear test element. The measurements were made using an Agilent 4294A Precision Impedance Analyzer with a varying DC voltage and an AC voltage of  $50 \,\mathrm{mV}$ .

Fig. 6 shows the measured magnitude and phase of impedance for frequencies up to 10 MHz. The applied DC bias voltage has been varied between -60 V and -80 V, where the latter value correspond to approximately 90% of the CMUT pull-in voltage (-90 V).

In the magnitude plot four clear resonant peaks are seen for the corresponding voltage values. The spring-softening effect



Fig. 3: Scanning electron microscope cross-sectional image of silicon wafer from step 1 in the fabrication process (Fig. 3). The etch depth of  $113 \,\mu\text{m}$  is acquired after performing multiple deposit and removal cycles.



Fig. 4: Scanning electron microscope cross-sectional image of wafer backside from step 4 in the fabrication process (Fig. 2) before polishing. The bottom electrodes are seen as zig-zag shaped DREM etch separated silicon segments.

is also observed by the shift to lower resonance frequencies in the range from  $\approx 6.3$  MHz to  $\approx 5.5$  MHz, by increasing the DC bias. Since these test elements have wider cell diameters the resonance frequency is also lower than the expected 8 MHz for the RCA CMUT array. The electromechanical coupling coefficients given by equation  $k^2 = (1 - (f_{res}/f_{arres})^2) \times 100\%$ , are estimated to be 3.7%, 3.8%, 3.9%, 4.4%, and 7.8%, where  $f_{res}$  and  $f_{ares}$  are the resonance and anti-resonance frequencies respectively. The phase angle is also constant at  $-90^\circ$  except for around the resonant frequency in correspondence with



Fig. 5: Optical images of the wafer backside from step 4 in the fabrication process before anodic bonding is carried out (Fig. 2). (a): After the backside RIE process has separated the bottom electrodes. (b): After polishing the backside using a CMP process.



Fig. 6: Impedance measurements of the fabricated linear CMUT test array at four different DC biases with a 50 mV AC bias. The expected spring softening effect is observed for increased DC magnitude.

typical CMUT capacitance behaviour.

#### B. Acoustic

To acoustically verify the CMUTs' ability to transmit pressure, the array is mounted on a printed circuit board (PCB) and the contact pads are wire-bonded to the board. A dam of acrylic glass is then glued onto the PCB around the array and filled with a polydimethylsiloxane (PDMS) with an approximate thickness of 2 mm. This serves to electrically insulate the elements from the water. The encapsulation procedure is described in [13].

The acoustic signal from the linear CMUT test array has been measured using a HGL-0400 hydrophone connected to a AC-2010 pre-amplifier (Onda Corporation, CA, USA) in immersion aligned 4 cm from the transmitting CMUT array. The elements were actuated with a single cycle 10 V peak-to-peak 4 MHz



Fig. 7: Hydrophone signal from for linear CMUT test array. A single-period, 4 MHz sinusoidal pulse is used to excite the array.



Fig. 8: The amplitude spectrum of the received hydrophone signal for the linear CMUT test array.

sinusoidal pulse with a DC bias of -90 V and the signal from the hydrophone is sampled by a 5442D oscilloscope from PicoScope using 12 bit resolution and a sampling frequency of 62.5 MHz.

Fig. 7 shows the measured hydrophone signal as a function of time and Fig. 8 the amplitude spectrum of the signal. Both show expected typical CMUT characteristics. The bandwidth read off at -3 dB is determined to be 68% and is limited by the bandwidth of the pulse.

The substrate ringing due to the silicon substrate and bonded glass wafer is observed in the spectrum at  $\approx 5 \text{ MHz}$  which is in agreement with the expected frequency.

## IV. CONCLUSION

This paper presented an alternative fabrication method of RCA CMUTs. The method utilises a DREM process combined with an anodicly bonded glass wafer to fully separate the bottom electrodes of the arrays electrically. This ultimately leads to a reduced substrate coupling. Characterization during the fabrication process shows the expected mechanical separation of the elements by etching and backside polishing in preparation for bonding. Electrical and acoustical characterization shows typical CMUT behaviour. Resonant frequencies were measured between 6.3 MHz and 5.5 MHz with DC biases from -60 V to -80 V with corresponding electromechanical coupling coefficients from 3.7% to 7.8%.

From the hydrophone measurements in immersion substrate ringing is observed at 5 MHz and a pulse bandwidth is estimated to be 67.7%.

In conclusion, the fabrication methods and row-column design used, which combines tight control of cavity dimensions by LOCOS and electrical insulation by anodic bonding and DREM, results in a functioning CMUT with a good electrical and acoustical response. The next step will be measuring on a RCA CMUT. A device with these specifications will by a possible candidate for the use in super resolution imaging.

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