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Anodically Bonded CMUT with a Two-Layer Bottom Electrode for Increased Reliability and Reduced Parasitic Capacitance

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***Abstract*—This paper introduces a new fabrication process variation for improving the reliability and performance of capacitive micromachined ultrasonic transducers by using a two-layer bottom electrode on a glass substrate. This structure decouples the active gap from the gap at the interconnects allowing for thicker nitride in the sealing area. A larger gap at the interconnects decreases their parasitic capacitance, and thicker sealing nitride decreases the effects of charging and can prevent dielectric breakdown.**

Keywords—CMUT, Charging, Reliability, Anodic Bonding,

I. INTRODUCTION

To maximize the efficiency and reliability of capacitive micromachined ultrasonic transducers (CMUTs), it is critical to design for low parasitic capacitance, high breakdown voltage, and reduced charging. Previously we made CMUTs with glass spacers inside the cavities which allowed us to operate in collapse mode without charging in the active region [1]. However, the DC voltages caused charging in the sealing region of these devices. Because these devices used one metal layer for the bottom electrode, the gap and sealing layer height were the same. The sealing dielectric was exposed to a high electrical field during high-voltage operation, leading to charging and possibly breakdown [3]. In this work, we use a two-step metallization process to decouple the gap height and the nitride thickness at the sealing location. In the design, presented here, the first metal layer is used for electrical connections and a second layer is added to the active regions to decrease the parasitic capacitance in the overall device structure. This change decreased the device capacitance by 13.5 pF (21.5%), mainly by reducing the parasitic capacitance due to cell-to-cell interconnects. Figure 1 shows schematic cross sections of the two devices for comparison.

II. METHODS

To realize the described device structure, we used a six-mask anodic bonding process based on previous work for fabrication [2]. A 0.7-mm thick, 100-mm borosilicate glass wafer was used as the substrate. On the wafer we included control devices. These control devices were fabricated identically to the others, but the bottom electrode was patterned differently. The control devices' gaps for the interconnects, active area, and sealing area are all the same representing a typical CMUT.

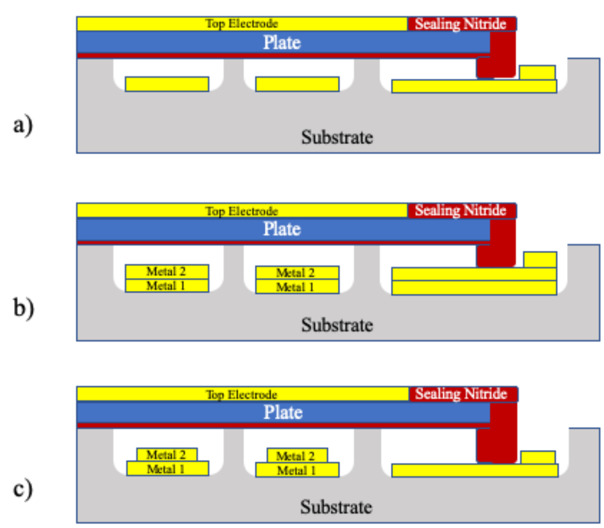

Figure 1: Cross sections of a) Conventional CMUT fabricated using anodic bonding process, b) Control device with the same gap height as a) with 2 metal steps, and c) the proposed device. For this run b) and c) were fabricated

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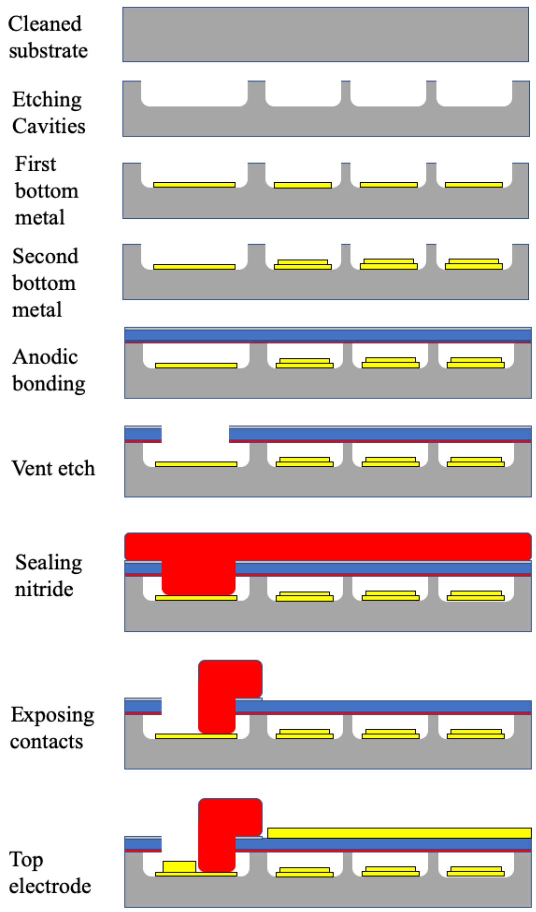

Figure 2: Process flow for fabrication of CMUTs

Substrates were cleaned using piranha solution. The cavities were etched to a depth of 500 nm using reactive ion etching (RIE) followed by buffered oxide etch (BOE) to smooth the cavity. The first layer of the bottom electrode was deposited using e-beam evaporation and patterned by lift-off. This layer is 180 nm of gold with a 20-nm chromium adhesion layer. The second layer was patterned on top with e-beam evaporation and lift-off. This layer was 150 nm of gold to meet the target gap of 150 nm. AFM images showing the patterned electrodes are shown in Fig. 2. The bottom wafer with cavities and the dual layer electrode was cleaned using Nanostrip before being anodically bonded to a silicon-on-insulator (SOI) wafer. The SOI wafer had 300-nm buried oxide and 1.5 µm silicon on top of a silicon handle wafer. The anodic bonding occurred at 750 V and 350°C under vacuum. The temperature was ramped up for thirty minutes with a thirty-minute dwell time. After bonding, the silicon handle layer was removed by grinding and then KOH etching. RIE was then used to etch the device to vent trapped gases resulting from anodic bonding. The gas was evacuated and the cavities were sealed by depositing 1.5-µm conformal

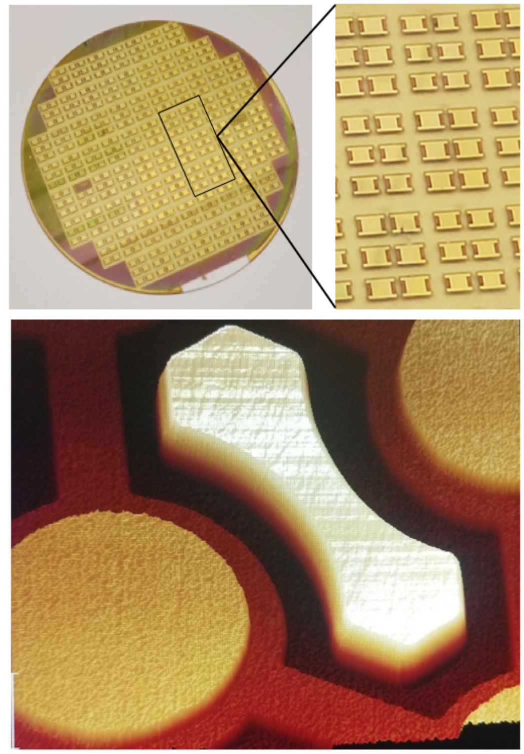

Figure 3: Photographs of the completed wafer with an AFM image showing the electrodes and post before bonding

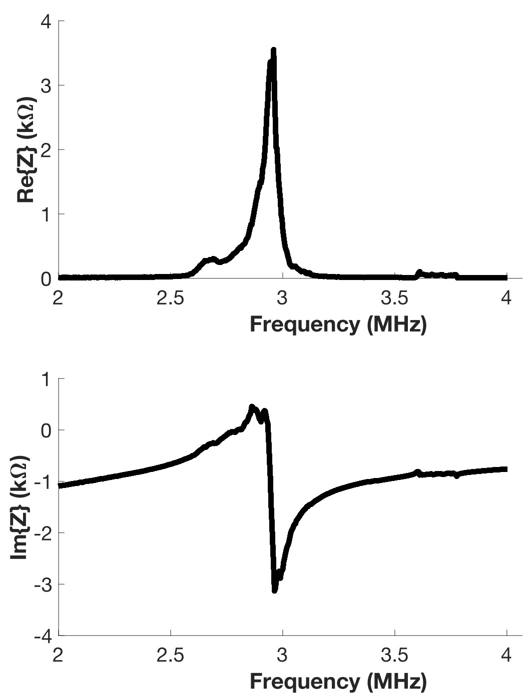

Figure 4: Real and imaginary parts of CMUT impedance

silicon nitride using plasma enhanced chemical vapor deposition (PECVD). The nitride was then etched using RIE to expose the contacts. Finally, the top electrode was deposited using e-beam evaporation and patterned using lift-off.

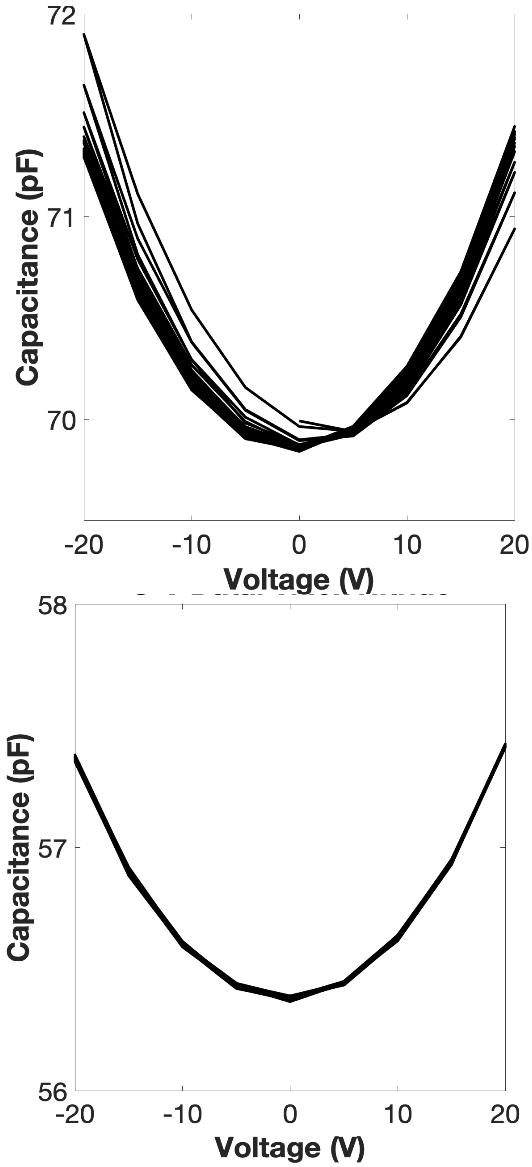

Figure 5: Capacitance vs. voltage (C-V) measurements of control device (top) and improved device (bottom)

III. Results

The fabricated devices were tested using a network analyzer (Model E5061B, Agilent Technologies, Inc., Santa Clara, CA, USA). The devices showed a sharp peak in the real part of impedance at 3.1 MHz. Figure 4 shows the real and imaginary parts of impedance at 40-V-DC.

To evaluate the comparative charging effects experienced by the devices in conventional mode, the real and imaginary parts of impedance was measured as the DC bias was swept from -20 V to 20 V for twenty cycles. The capacitance was extracted from the highest frequency measurement of the imaginary part of impedance. The resulting C-V characteristic is shown in Fig. 3. The curves show a 5-V shift in the control device, but no shift in the improved devices. The curves also show that the new devices have a 13.5 pF lower capacitance due to the decreased parasitics from the interconnects.

The improved C-V characteristics with no shift show that the proposed two-layer metallization provides more consistent operation over time. It is also suitable for CMUTs designed to operate as gas sensors. The frequency drifts due to charging can be minimized with the proposed fabrication method.

IV. Conclusion

To improve the reliability of a CMUT, devices with a two-layer bottom electrode and thicker sealing nitride were fabricated using an anodic bonding process. The completed devices with thicker sealing nitride showed a sharp resonance peak and improved C-V characteristics compared to control devices. The two-layer bottom electrode also allowed for lower parasitic capacitance at the interconnects.

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