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Tiled Large Element 1.75D Aperture with Dual Array Modules by Adjacent Integration of PIN-PMN-PT Transducers and Custom High Voltage Switching ASICs

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Abstract— **Tiled large aperture 1.75D/2D transducer arrays with closely integrated ASIC electronics have the potential for implementing high channel count ultrasound probes for novel applications, however they must have high yield for a large number of elements to maintain good image quality. This constraint can be addressed by tiling together a number of smaller array modules to build up the larger aperture. In this work we present recent imaging results for large apertures with multiple tiled array modules integrating 2D arrays of wide bandwidth PIN-PMN-PT 1-3 composite piezo elements with custom-designed ASICs for buffering and multiplexing functions. The ASICs are optimized to obtain increased sensitivity of the high impedance 2D elements using buffering. We have also been developing novel second-generation ASICs to mitigate the effects of switching transients observed while imaging with the first-generation devices.**

Index Terms—**ultrasound, modular array, ASIC, single crystal, interposer, 3D printing, charge injection**

I. Introduction

Architectures for large aperture transducer arrays with hundreds [1]-[3] to thousands [4]-[5] of elements are being investigated for their utility in volumetric imaging and also for their potential to improve image quality [6] and resolution. To improve yield on the large number of elements a tiled approach [1]-[2], [7] is advantageous. 1.75D/2D transducer arrays [8] with closely integrated ASIC electronics have the potential for implementing high channel count ultrasound probes with improved focusing in elevation for these novel applications. In addition, these large apertures require special considerations to mitigate unique image artifacts due to gaps between modules [1] and electrical transient effects magnified by the large number of required switches.

In this work we present recent imaging results for large apertures with multiple tiled array modules integrating 2D arrays of wide bandwidth PIN-PMN-PT 1-3 composite piezo elements with custom-designed ASICs for buffering and multiplexing functions. The first-generation ASICs are optimized to obtain increased sensitivity of the high impedance 2D elements using buffering and local switching to reduce cable channel count. We have also developed novel second-generation ASICs to mitigate the effects of MOSFET charge-injection observed while imaging with the first-generation devices. These new ASICs utilize off-the-shelf buffer amplifiers closely integrated with the custom devices. In this paper we present imaging results with the first- and second-generation array modules and compare the results to show effective mitigation of the image artifacts.

II. Methods

We fabricated multiple generations of tileable acoustic modules (Figure 1) using techniques described previously in detail [2], [9]. The acoustic stacks were integrated onto printed circuit boards housing custom-designed multiplexing array electronics [2]. There were two generations of ASICs designed, and results for both of these are presented here to compare their performance. In particular, the first-generation ASICs [2] demonstrated good imaging performance however they suffer

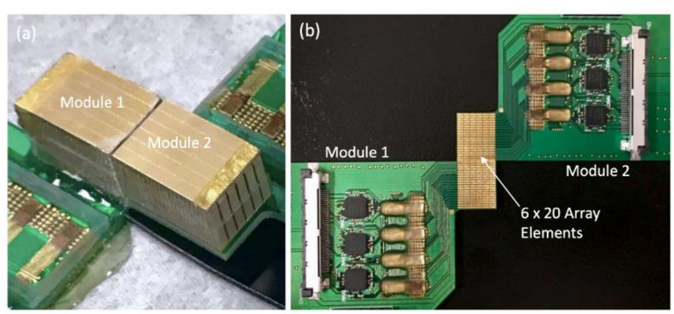

Figure 1: (a) First- and (b) second-generation tileable acoustic/electric modules. (a) Shows PCB ASICs and integrated PIN-PMN-PT stacks.

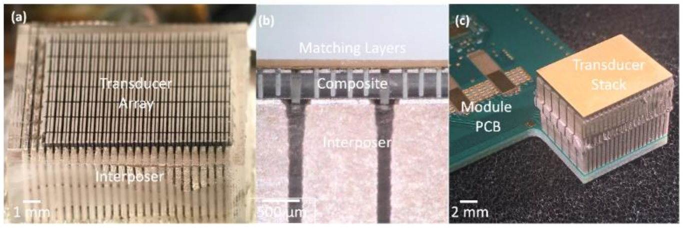

Figure 2: Fabrication of the second-generation tileable acoustic stacks. (a) 2D array of 6×20 elements after initial dicing, (b) cross-section of the completed acoustic stack, (c) mock-up assembly of the array to a bare second-generation PCB.

from visible image artifacts due to switching transients (described below). The second-generation ASICs were designed to mitigate these switching transients by using a low charge injection switch topology. The architecture of these new ASICs will be discussed in detail in Section II-B below. Test and comparison of the two types of ASIC modules with associated acoustic stacks will be presented in Section III.

A. *Acoustic Module Fabrication*

The acoustic modules for the large array were fabricated as described previously [2] for the first-generation test prototypes. The second-generation prototypes were fabricated using a modified process as described below.

Figure 2 shows the newly fabricated acoustic stack during processing. We previously fabricated the array using a PIN-PMN-PT and epoxy composite which was pre-diced and then assembled to the surface of an interposer backing. For the new array, we assembled un-diced bulk PIN-PMN-PT material (CTS, Bolingbrook, IL) 450 μm thick with a 110 μm thick first matching layer composed of 2-3 μm silver epoxy to a fabricated interposer with a 3D printed acrylic grid frame 9 mm tall. The filler material in the grid frame was E-Solder 3022 (Von Roll, Schenectady, NY). We then diced the solid material to form a composite [Figure 2 (b)], sputtered a top ground layer (500 Å Chrome and 1000 Å Gold), and then laminated the second matching layer (130 μm thick ABS plastic). The main advantage for this modified process is that alignment of the composite grid to the interposer grid is done intrinsically and did not require careful XYZ and rotation clamp alignment as before [2]. Another feature of the second-generation PCB and acoustic modules is that the ground connection is brought out on the elevation side [Figure 1(c)], rather than on the azimuthal side, which is important for seamless tiling in azimuth for more than 2 array modules. For initial prototype testing of the performance of the new ASIC (described below) a first-generation acoustic stack was used.

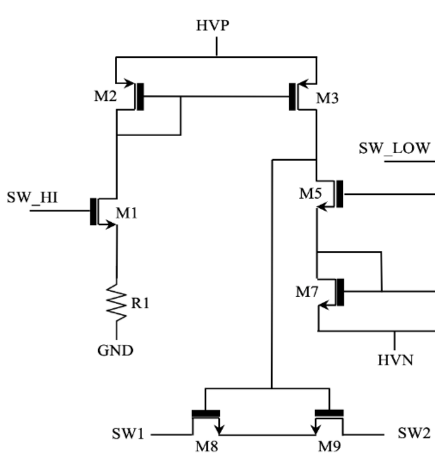

Figure 3: Schematic of the low charge injection high voltage switch. HVP, and HVN are positive/negative high voltage supplies, and VDD is the logic supply voltage (+3V).

B. *Low Charge-Injection Switching ASIC*

An important consideration for an electronically scanned array is the reduction of image artifacts caused by mux switch actuation. This problem is especially acute in arrays where a different multiplexing array configuration is used for the transmit vs. the receive cycle (e.g. full synthetic aperture beamforming) and is made increasingly worse for a larger number of elements. Switch actuation can lead to electronic switching transients (or “glitches”) being coupled to the array elements due to charge injection. The simultaneous transition of thousands of switches in a large 2D array emits a plane wave due to this coupling, and results in visible image artifacts for strongly echogenic targets (e.g. flat plate reflectors, and wires). Mitigation of these artifacts is an important consideration for large area arrays that utilize different array switch configurations on transmit and receive for implementing synthetic aperture beamforming.

To address this requirement for reduced image artifacts, we implemented a new switch architecture for our switching ASIC (Figure 3). This topology is a modification of our earlier switch architecture [10] that reduces the charge injection on the switching terminals (SW1 and SW2) and thereby leads to a reduction in the observed image artifacts due to switching.

The switch consists of high side (M1-M3) and low side (M4-M7) high voltage level shifters which charge and discharge the gate-source capacitance of the actual high voltage switching devices M8 and M9. Charge injection is a well-known phenomenon in CMOS circuits that is caused by establishing (switch on) and quenching (switch off) of the conduction channel under the MOSFET gate. There are many techniques for reduction of charge injection including the use of dummy switches and modulation of the gate-source charging waveform. For the circuit of Figure 1, we implemented drain resistors (R1 and R2) which effectively linearize control of the

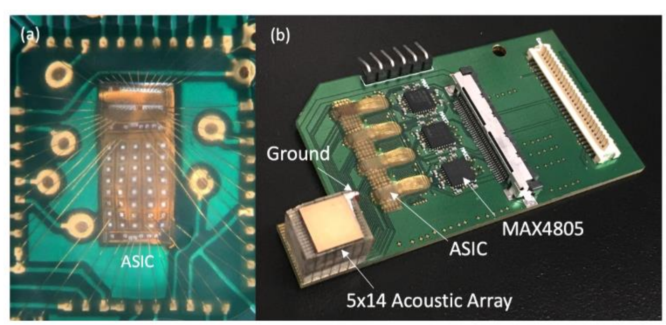

Figure 4: Acoustic/electric module assembly showing (a) fabricated low charge injection ASIC and (b) integrated second-generation acoustic/electric module.

gate voltage and thereby create a slowly ramping control voltage at the gates of the turn on (M1) and turn off (M4) control FETs. The reduced control ramp edge rate translates to a similar reduction in the charging current edge rate in the drains of M3 and M5 which leads to reduced voltage edge rate on the gate source node and results in lower charge injection (discussed further in Section III).

The unit switch cell circuit of Figure 3 was used to build a multiplexing ASIC designed to interface to an array of 5 columns and 8 rows of transducer elements. This ASIC design was implemented in a standard 0.35 μm 50V CMOS fabrication process (AMS H35). Figure 4 (a) shows a photomicrograph of the fabricated device with wire-bond connections for testing. The 5×8 grid of silver colored cell pads is visible in the image.

C. *Acoustic/Electric Module Integration*

The fabricated low charge injection ASICs were integrated with a prototype acoustic stack onto custom-designed Printed Circuit Boards [Figure 4(b)]. In previous work we implemented ASICs with on-chip buffering to match the high impedance of the small 2D elements to the cable and system loads [2]. With the new low charge injection ASIC, we instead used off-the-shelf buffering circuits (MAX4805, Maxim Integrated, San Jose, CA) which incorporate high voltage transmit/receive switches for every channel. The ASICs were wire-bonded to the PCB by a vendor and the acoustic stack was integrated using a conductive adhesive "stamping" technique described previously [2], [9]. Figure 4(b) shows the completed PCB housing the acoustic stack with backing interposer, four switching ASICs and three MAX4805 devices realizing an electronic 20 channel array in azimuth with multiplexing for selection of 6 rows in elevation. The initial fabricated prototype utilized an early acoustic stack that had only 5×14 elements for evaluation. The full 6×20 array described in Section II-C will be integrated with the new ASICs in future work.

III. Results

The first- and second-generation fabricated array modules were interfaced to a Verasonics Vantage 128 system (Verasonics, Kirkland, WA) with the high frequency option for testing in our lab. Interfacing to the ASICs was accomplished using a custom FPGA interface control board described previously [2]. The Verasonics system was programmed to implement full synthetic aperture in the azimuthal direction. Both single and multiple array module configurations were tested and the results will be presented in this section.

A. *Large Tiled Array Imaging*

The array modules shown in Figure 1 (a) were used to build a large aperture tiled array with 6×40 = 240 2D elements implementing a 1.75D array capable of electronically switched beamforming in elevation. The two modules shown in Figure 1(a) each had four first-generation ASICs with on-chip buffer amplifiers and each module interfaced to an acoustic array of 6×20 elements. The tiled array modules were tested separately, operating as a single 6×20 array of elements, and then they were tested as a complete tiled array operating with the full 240 channel aperture. For these imaging experiments, the 1.75D

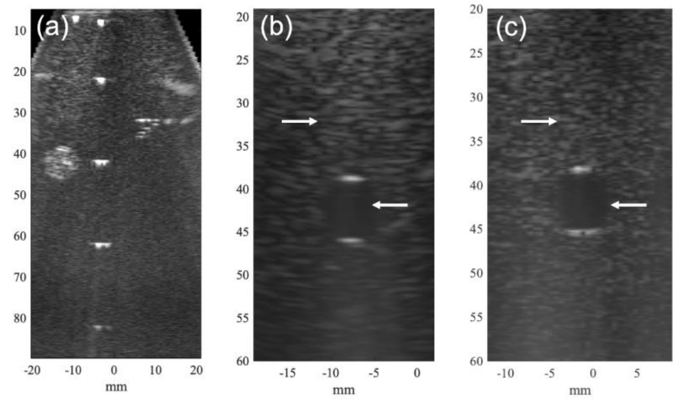

Figure 5: Results for first-generation tileable array modules showing images for (a) two tiled modules, (b) single 6×20 module imaging of an anechoic cyst, and (c) two tiled modules, same embedded structure.

array elements were electronically configured to be tied together in each column to form linear array elements in azimuth. An industry standard CIRS 054GS ultrasound test phantom (CIRS, Norfolk, VA) incorporating echogenic and anechoic inclusions was used for imaging.

Figure 5 (a) shows the image results for the complete 2 module array demonstrating the ability to image a wide field of view with greater than 8 cm penetration into the phantom. As can be seen in the image, there is diverging of the beamforming results for the two arrays leading to defocussing of the wire targets past 4 cm depth in the phantom. This defocussing can be mitigated by calibration of the module registration in the beamforming and will be implemented in future work.

Figure 5(b) shows a close-up view of image results for a single 8 mm diameter anechoic cyst at 40 cm depth as imaged by a single 20 elements-in-azimuth first-generation module. The module demonstrates good contrast resolution however, the grain in the speckle is wide in the azimuthal direction due to the use of a narrow aperture, and in addition the borders of the cyst are poorly defined. Figure 5(c) shows the same cyst as imaged by the two-module tiled array with a 4 elements-in-azimuth wide aperture. As compared with Figure 5(b), the double-wide array obtains improved azimuthal resolution as demonstrated by the finer speckle grain and also by the enhanced definition at the borders of the cyst. Further improvements in contrast and resolution are expected for a larger number of tiled modules (e.g. 1×3 or 1×4 in azimuth).

B. *Improvement in Charge-Injection Induced Image Artifact*

The second-generation array module of Figure 4 was tested to evaluate the improvement in charge-injection performance of the new ASICs as compared to the first-generation devices. As discussed above, switching transients due to charge injection are coupled into each of the 2D array elements through their electrical connection to the ASICs.

To take full advantage of large array apertures, the array is operated in full synthetic aperture mode. In this case the switches are configured in a first mux setting prior to transmit, then immediately after transmit on all elements is completed, a second array switch configuration is implemented for the

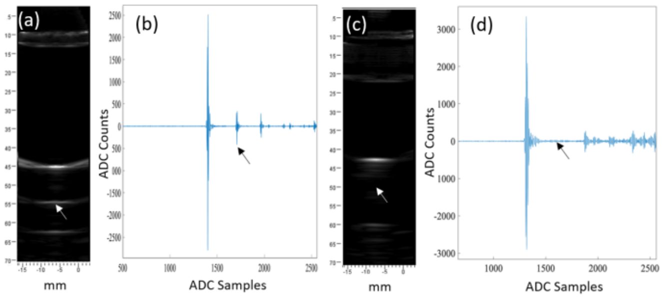

Figure 6: Imaging with (a)-(b) single first-generation and (c)-(d) single second-generation ASIC module demonstrating reduction in effects of switching transients in the image. (a) and (c) 75 mm thick quartz block at a depth of 43 mm, (b) and (d) time domain results for a single channel. Arrows show switching artifacts.

receive cycle. This switching scheme allows for a subset of the entire array to be actuated on transmit, followed by a different subset on receive which enables acquisition of all transmit-receive beamforming products that are necessary for achieving focussed beamforming on both transmit and receive for improved spatial and contrast resolution [8]. As described above, when the switches are actuated to change from the transmit to the receive array switch configuration, every element is stimulated by a switching transient. These transients all occur at the identical point in time which corresponds to a plane wave being transmitted by the array into the medium. Depending on the ratio of the number of elements and transmit voltage used for each synthetic aperture transmit vs. the number of switch transient elements, the resulting plane wave acoustic power can be large enough to generate important image artifacts for highly echogenic targets.

Figure 6 demonstrates the effect of the switching transients for a first-generation ASIC module interfaced to a 6×20 array of 2D elements. The results were obtained by imaging a 75 mm thick quartz block located at a depth of 45 mm below the array. As can be seen in Figure 6(a), there are three horizontal lines in the image. The brightest of these (at 45 mm depth) corresponds to the front face of the quartz block, and the third line (62 mm) is the rear face of the block. In between these two lines, there is a second line (55 mm) which is similar in intensity to the echo from the rear face of the block. This line was confirmed to be generated by the switching transients; when the transmit signal is reduced to a low voltage front and rear echos disappear however, the switching transient induced echo line remains. Figure 6(b) illustrates the RF signal for a single channel demonstrating the significant magnitude of this artifact.

Figure 6 (c)-(d) illustrate mitigation of the switching transients using the new low charge-injection architecture switch of Figure 3. As can be seen by comparing Figure 6 (a)-(b) and Figure 6(c)-(d), significant reduction of the switching artifact is achieved with the new switch architecture. As stated earlier, the magnitude of the switching artifact varies depending on the number of elements operating on transmit as compared to the number of elements experiencing the switching transient. For the tested arrays we observed a reduction in switching transients from the first- to second-generation ASICs of between -20 to -30 dB. These results also agreed with ASIC simulations.

IV. Conclusions

This paper presented results of fabrication and testing of first- and second-generation tileable modules of interface electronics and 2D PIN-PMN-PT ultrasound arrays for implementation of large area probes with improved image quality. Multiple first-generation arrays having high voltage multiplexing ASICs with on-chip buffers were tiled with 6×20 array elements each to realize a completed aperture of 240 elements which demonstrated improvements in lateral image resolution when operated as a linear array. A second-generation module was integrated with a prototype 2D array and used to acquire images for a highly echogenic target. The second-generation module benefited from a novel low charge-injection high voltage switch architecture ASIC and demonstrated -20 to -30 dB reduction in observed switching artifacts. Future work will integrate several of the second-generation modules to implement a large aperture 1.75D array with improved lateral resolution and reduced switching artifacts.

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