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An Ultrafast High-Frequency Hardware Beamformer for a Phased Array Endoscope

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***Abstract*— A ultra-fast high frequency ultrasound hardware based beamformer is described. The system was tested using a miniature 40 MHz 64 element phased array endoscope. The system used diverging wave beamforming with a total of 16 diverging waves in order to obtain a good beam profile at a 700+ Hz frame rate. Experimentally, the system was able to operate at a frame rate of 500 Hz, close to the implementations theoretical limit of 760 Hz. A novel technique was used to store 8.3 Million beamforming delays for 8 channels on a field programmable gate array (FPGA). The measured secondary lobe levels for the radiation pattern measurements were less than -35 dB and the main lobe had a beam width of 0.7 mm. Using field II, the simulated radiation pattern had secondary lobes suppressed to -50 dB and a beam width of 0.15 mm. Real-time images of wire phantoms were generated and displayed with custom developed imaging software.**

Keywords—Ultra fast, beamforming, high-frequency, ultrasound imaging, endoscope, phased array

I. Introduction

Ultra-fast ultrasound imaging also known as high framerate Imaging is proving to be an invaluable tool. The development of it has led to new imaging modes such as shear-wave elastography [1], functional brain imaging [2], real-time 3D Imaging [3], and super-resolution imaging [4]. These imaging modes require frame rates ranging from 500 Hz to 7 kHz. Shear-wave elastography measures the propagation of mechanical waves in tissue to determine their stiffness. This allows tumors to be easily identified due to them being stiffer than healthy tissue [1]. Functional brain imaging is used to map the functional response to stimuli. Due to the low cost and high portability of ultrasound, this could lead to significant breakthroughs in pre-clinical functional imaging studies and could eventually become a practical neurosurgical guidance tool [3]. These imaging modes, however, can only really become clinically useful if they are displayed in real time.

To achieve these high frame rates in ultrafast imaging, conventional line-by-line ultrasound imaging cannot be performed. Instead a synthetic aperture compounding approach must be used. In compound imaging, the entire image field-of-view is insonified with a defocused wavefront by either an individual element or multiple elements. Multiple elements can be used to create plane waves or diverging waves which increases the insonification energy and image SNR. Dynamic receive focusing is then performed using all the elements on the transducer. A single insonification suffers from poor SNR and beam profile, due to the lack of transmit focusing. These issues are combated by repeatedly insonifying the tissue with different wavefronts, either from other elements or groups of elements. By compounding each one-way focused frame from a different transmit wavefront, a synthetic transmit focus is achieved. More transmitted wavefronts and compounds will increase the SNR and beam-profile. The most common method of compound imaging, to date and likely the most straight-forward, is plane-wave imaging [5]. In plane wave imaging, multiple plane waves are transmitted at slightly offset angles. This is an ideal method of compounding for linear array transducers, since the image window is limited to the aperture of the array. For phased array transducers, the region of insonification is much larger than the aperture of the transducer and so diverging wavefronts are typically used instead of plane waves. Multiple diverging waves are transmitted from virtual point sources located behind the transducer. The image created by each diverging wave is then compounded together. To obtain comparable SNR to line-by-line imaging at least 32 diverging waves need to be transmitted [6]. In the work presented here diverging wave beamforming firmware has been developed for a miniature 40 MHz 64 element phased array endoscope.

Most Ultra-fast ultrasound systems implementing a compounding approach collect RF channel data and then perform the beamforming and compounding in software. Although relatively straightforward, performing beamforming in software is a computationally intensive process, and since there is so much channel data collected at very high speeds, real-time display of ultrafast imaging data is challenging. This has led to one group developing an Ultra-fast hardware beamformer for an 8 MHz linear array. Frame rates of 2 kHz were obtained for a transmission of 3 plane waves, where the maximum pulse repetition frequency (PRF) was 6000 Hz [7]. This system utilizes multiple FPGAs to partially beamform the RF data where the beamforming delay coefficients are stored on external memory. Digital signal processors demodulate the data and perform the final compounding of the data. The data was then sent to a PC through a USB 3.0 bus.

The work presented here takes a similar approach to the previously described hardware beamformer, however the system is designed for much higher frequencies (>30 MHz). The custom system was designed for a 64-element 40 MHz endoscopic ultrasound probe, miniaturized into a forward-looking endoscopic form factor [8]. The target application of this endoscope is for minimally invasive endoscopic surgeries. Implementing real-time ultrafast imaging on a high-frequency phased array system is extremely challenging due to the high data rates required for the increased bandwidth. For example, the required PRF to perform 16 diverging wave images at a capture rate of 700 Hz is 11200 Hz. This means the system needs to be able to beamform at a much faster rate than the system described in [7]. Additionally, for a phased array the number of required beamforming delays is much greater than a linear array since the beamforming delays cannot be reused for multiple lines. Due to the required beamforming speed, the beamforming delay profiles cannot be loaded onto the FPGA fast enough from external memory. The delay profiles must be stored internal to the FPGA. In this work, hardware beamforming for ultrafast diverging wave imaging has been achieved. All beamforming was performed on 8 parallelized FPGAs and this removes conventional bottlenecks preventing real-time display of ultrafast imaging modes by drastically reducing the amount of data transferred and processed by the PC.

II. System Design

A. Diverging wave compounding

In the first iteration of the hardware beamformer, we wanted to minimize the number of diverging waves required to achieve decent image quality. A low number of diverging waves will not only increase the ultra-fast frame rate achieved, but also lessen the number of beamforming delay profiles required on the FPGAs. Fig. 1 shows an impulse response simulation using Field II [9,10]. In this simulation, it can be seen that the beam profile for 16 diverging waves is still of a relatively high quality in comparison to 32 diverging waves and 64 diverging waves. It

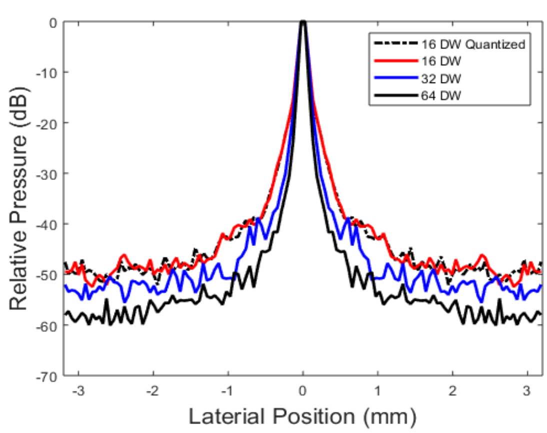

Fig. 2. The point spread function for 16, 32, and 64 diverging waves with the point source 6 mm away from the transducer face, ~0.15mm 6dB beam width

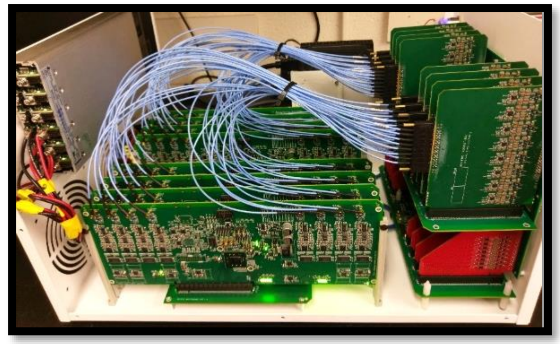

Fig. 1. The custom built ultrasound system

was also shown that 32 diverging waves approaches an equivalent beam profile to 64 diverging waves which is comparable to traditional line-by-line transmit-receive focusing. Transmitting 16 diverging waves results in secondary lobes that are approximately 10 dB higher. It was determined that 16 diverging waves was an acceptable sacrifice in image quality. Assuming a maximum pulse repetition frequency of 40 KHz, 16 diverging waves can achieve a maximum theoretical frame rate of 2500 Hz in comparison the 1250 Hz with 32 diverging waves.

B. System Architecture

The In The in-house developed 64-channel beamforming system was composed of 5 primary hardware components. The Transmit Mother Board, Transmit Daughter Cards, Receive Mother Board, Receive Daughter Card, and a 64-element high frequency endoscopic ultrasound transducer. Fig. 2 shows a photograph of the hardware beamformer. The system was setup to perform diverging wave compound imaging with 16 diverging waves transmitted by the transmit motherboard and daughter card. The 16 virtual point sources for the diverging waves were located 78 um behind the array and were spaced 38 um apart. The diverging waves were designed to insonify a 100 degree sector from each of the sub apertures. The RF signals were then received by the transmit daughter cards, amplified, and sent to the receive daughter cards. The receive daughter cards digitize the RF signals using a synchronized FPGA on each card. Each daughter card FPGA beamforms the received data for 8 channels and then transfers the beamformed data to the receive motherboard. The receive motherboard is the primary controller for the whole system triggering the transmit motherboard to send out 16 diverging waves and then collecting the beamformed data for the final compounding steps. The beamformed frames are then stored on the motherboard before being transferred to the PC for further processing.

C. Beamforming Algorithm

The 8 receive daughter cards each have their own FPGA (Kintex 7 XC7K160T-1FBG484C, Xilinx, San Jose Ca.). The control flow for each daughter card is shown in Fig. 3. Each card is responsible for collecting 1024 samples of RF data for 8 channels per insonification. The RF data is sampled at a rate of

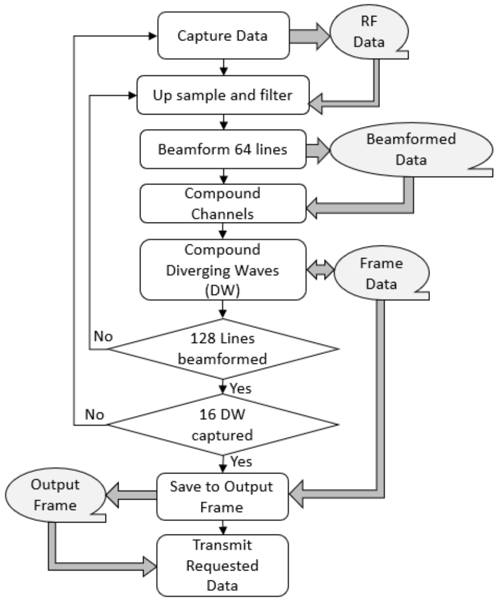

Fig. 3. The control flow implemented on the receive daughter cards

100 MHz and stored in block RAM on the FPGA. The data is then up sampled by a factor of 4 and sent through a finite impulse response (FIR) match filter on board the FPGA. The match filter was designed to match the transducer's frequency, bandwidth, and pulse shape. The causes it to act as a bandpass filter around the transducers center frequency. The up sampled data is then beamformed by the hardware using a novel approach for compressing the beamforming delays. The RF data is delay and sum beamformed initially for 64 image lines in the first pass, and then another 64 immediately following the first 64. Due to resource limitations on the FPGA, only 64 lines out of the total 128 lines can be beamformed requiring the interpolation and beamforming to be performed twice. As such, this limits the time required to beamform 16 diverging waves to 1.3 ms, when using a 100 MHz data clock on the FPGAs. This limitation comes from the interpolation process where 1024 samples are interpolated to 4096 samples. Since this happens twice the FPGA needs at least 8192 clock cycles to beamform the data. For 16 diverging waves this creates the frame rate bottleneck (760 Hz). Due to being unable to beamform all 128 lines at once, the ultrasound image has to be split up into 4, 32-line quadrants to make use of the beamforming algorithm described in the following section. This allows the first and last quadrant to be beamformed at the same time and then the second and third quadrant. Once all 128 lines are beamformed the next diverging wave is transmitted and the process repeats compounding the new beamformed lines with the old one. Once 16 diverging waves have been collected the motherboard is notified that data is ready and is then able to request data from the daughter card.

On each daughter card there are over 8.3 Million delays required to beamform all 8 channels for 16 diverging waves into a 128-line image with 512-focal depths. The beamforming algorithm quantizes the beamforming delays for each line where for an artificial sampling rate of 400 MHz the pixels can be quantized to a 7 or 8 clock cycle spacing. Limiting the pixel spacing to two values that are a factor of the clock frequency on the FPGA (100 MHz) allows the delays to be stored as a 1 or a 0. This significantly reduces the amount of memory required to store the beamforming coefficients. Additionally, the symmetry of the phased array transducer was exploited to half the number of delays required. This is because the delays for channel 1-64 for diverging wave 1 are the same as channel 64-1 for diverging wave 16. This is where the previously mentioned quadrants come into play. To utilize the algorithm the first and forth quadrant of the image must be beamformed together to allow the quadrants to be swapped when beamforming diverging waves 9-16. This also requires the hardware connections to be remapped where each daughter card needs access to the symmetric channels on the transducer. This means if a daughter card has access to channel 1-4 it needs access to channel 61-64 to utilize this symmetry. These two methods effectively reduce 8.3 Million delays down to 4.2 Million delays allowing the delays to fit on the FPGA. While the quantization for the beamforming delays inherently introduces errors for each pixel it has a negligible impact on image quality, as shown in Fig. 1.

The hardware beamformer does introduce some small limitations in the dynamic range of the beamformed data primarily due to the extreme utilization of the FPGA and the data bus size between the daughter card and motherboard being limited to 16-bits. The data is sampled at 12-bits and then gets interpolated up to 13-bits. Ideally this would be a much larger value to better represent the interpolated data. The channel data is then summed together causing the beamformed data to be 16-bits. The subsequent compounding of the 16-diverging waves requires 4-bits to be dropped from the beamformed data so that the compounded data does not exceed 16-bits. The data can then be sent to the motherboard where the 8 boards are compounded together bringing the final bit depth to 19-bits. Currently up to eight frames are stored on the motherboard before being sent to the PC for further processing. The PC is responsible for the demodulation of the beamformed data and image display.

III. Results and Discussion

After The ultra-fast high-frequency hardware beamformer image quality was compared to that of software beamforming. This was done by taking raw captured RF ultra-fast ultrasound data and simulating the beamformed image for the reception on one receive daughter card. The Vivado simulations showed promising results where the image was comparable to software beamforming. The dynamic range of the Vivado simulations appeared lower. This was most likely due to the differences in implementation of the interpolation filter. While both implementations capture 12-bit ADC data the software beamforming implementation passes the raw RF data from the FPGA to the PC for beamforming as such there is no issue with quantization of the RF data or beamformed data like there is on the hardware beamformer. Comparing the measured PSF from the hardware beamformer with Field II simulations shows worse results than expected. In Fig. 1 the PSF has a 0.15 mm beam width at the 6-dB mark while the measured beam width in Fig. 4 is 0.72 mm. The affects of quantized delay profiles and bit limited data are expected to slightly worsen the radiation pattern, but the effect is much worse than anticipated and cannot be the only cause. Additionally, the broad width of the PSF in Fig. 4 suggest the beamforming was being performed incorrectly on

Fig. 4. The point spread function when measuring a wire target at 6mm depth, ~0.7 mm 6dB beam width

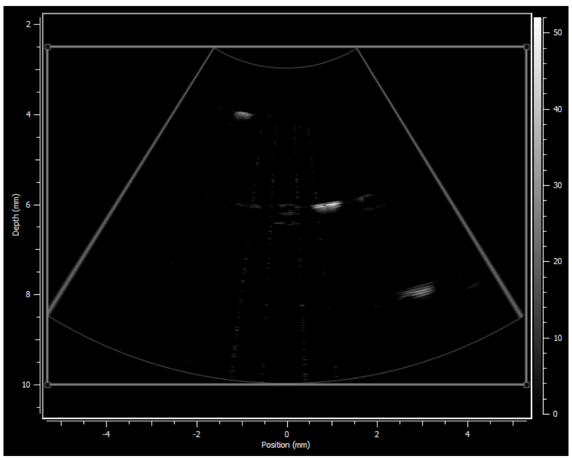

Fig. 5. Measurement of a wire phantom with 3 wire targets spaced apart displayed with 50 dB of dynamic range.

the receive daughter card. Likewise numerous artifacts are present in Fig. 5 that are not present during simulations or when beamforming using the software. These images suggest that the implementation of the beamforming algorithm on the receive daughter card was incorrect. It was also discovered that an increase in the single amplitude caused the signal to saturate. This was likely related to the interpolation process performed on the daughter card. If the filter was not properly interpolating the RF data, then this could cause the signal to saturate. This saturation of signal could also be the primary reason that the beam profile was not as expected. If the filter is clipping large signals running through the filter, the top portion of the main lobe in the radiation pattern would also be clipped off producing a beam profile similar to what was observed experimentally.

However, the beamforming performed well enough that 3 wire targets spaced by 1 mm depth and 1 mm laterally are distinctly visible in the imaging region in this image displayed with 50 dB of dynamic range.

IV. Conclusion

Ultra-fast high frequency beamforming has been implemented on a hardware beamformer. The beamformer is capable of imaging multiple wire targets at a frame rate of 500 Hz and at best achieves a PSF with a SNR of -35 dB. The results suggest that there are beamforming and signal processing errors present on the FPGA. Once these issues are resolved the hardware beamformer will be able to obtain SNR values comparable to the Field II simulations with a similar beam width. Additionally, the frame rate will be able to be pushed to at least 700 Hz. Once these issues are resolved the FPGA clock rate will be doubled to double the beamformer frame rate to 1400 Hz.

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