Charging-Free CMUTs with High Contact-Resistance ZnO ALD Film

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Background, Motivation and Objective

CMUTs have shown great potential for ultrasonic imaging arrays with highly integrated electronics. However, dielectric charging has remained a persistent challenge limiting long-term reliability and can result in device failure. Most isolation is MEMS devices is accomplished with insulating dielectrics. As an alternative MEMS isolation paradigm, we introduce high contact-resistance semi-conducting thin films. This could lead to CMOS-compatible CMUTs with long term reliability.

Statement of Contribution/Methods

In particular, we use Atomic Layer Deposition (ALD) ZnO thin films as a CMUT isolation layer. These films have compelling properties such as high breakdown voltage and enormous contact-resistivity but low bulk conductivity. Since the ALD ZnO film acts like a large resistor when a membrane collapses, it will mitigate unwanted shunt currents while mitigating charge trapping. We developed a new low-temperature adhesive bonding process with ZnO isolation. Fabrication starts by depositing a 20-nm PEALD ZnO thin film on a highly p-doped prime wafer with resistivity of 0.0001-0.005 Ohm-cm which acts as a bottom electrode. Cavities are formed in a thin BCB polymer layer spin coated on an SOI wafer with device layer resistivity of 0.0001-0.005 Ohm-cm. Then two wafers are bonded though adhesive wafer bonding. Handle and BOX layers of the SOI wafer are selectively etched to leave the device layer as the top membrane and electrode.

Results/Discussion

Contact resistance depended on ZnO deposition parameters and annealing times as well as contact materials but measured to be >50MOhm and as high as 50 TOhms in bulk sample testing. Capacitance-Voltage (CV) curves over multiple bias-voltage ramp cycles applied to fabricated devices revealed no charging in the ZnO layer, while enabling multiple actuation cycles. Fig. 1 (a) illustrates a fabricated array consisting of seven parallel cells and a cross-sectional view of the fabricated CMUTs with ALD ZnO layer. Fig. 1 (b) illustrates the central deflection of a 30 µm membrane with different applied voltages. Fig. 1 (c) presents the acquired CV data for four consecutive actuations up to the snap-down for the ZnO devices. In both figures, voltages are normalized to snap-down voltage which is 85 V. Preliminary results suggest charging-free and breakdown free operation should be possible enabling future CMUT-on-CMOS technologies.

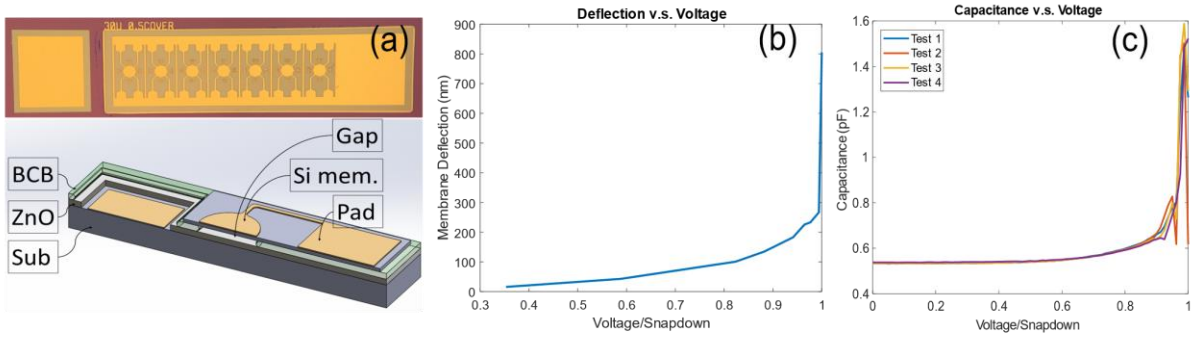

Fig.1 (a) Fabricated array and cross-sectional view of the ZnO CMUT devices (b) Deflection versus voltage changes measured by an optical profilometer. (c) Capacitive versus voltage changes measured with a Semiconductor Characterization System.