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Crosstalk Study of Large PMUT Array using FEA and Cloud HPC

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***Abstract*— This paper presents FEA analysis using high-performance computing for crosstalk study in a piezoelectric micromachined ultrasound transducer (PMUT) array. The array comprises 64 1-D elements which each element comprises 80 membranes. The simulation for 5120 membranes (64x80) takes about ~2 hours executed on Amazon Web Services (AWS), and consuming ~700 core hours with 2GB RAM. The crosstalk displacement for several elements has been simulated showing significant impact on adjacent elements that will be reduced when the wave travels farther. The simulation also shows crosstalk frequencies higher than the device center frequency. The effect of pitch size is also studied on crosstalk implying larger pitch mitigates the crosstalk effect.**

Keywords— Cloud simulation, finite element analysis (FEA), high-performance computing (HPC), PMUT array crosstalk, PMUT array simulation

I. Introduction

Micromachined ultrasonic transducer arrays have attracted great attention in recent decades as an alternative to traditional bulk piezoelectric transducer. Bulk piezoelectric transducers have been traditionally used in several technologies and applications including sensing, nondestructive evaluation, medical imaging, medical therapeutics [1]-[3], etc. MUTs can be excited by capacitive force in capacitive micromachined ultrasound transducers (CMUTs) or by the piezoelectric effect in piezoelectric micromachined ultrasound transducers (PMUTs). In both cases, the acoustic impedance of the membrane-based transducer is closely matched with the surrounding medium such as water or air and hence does not require matching layers associated with bulk piezoelectrics. Another advantage of MUTs is the ease of device fabrication using conventional micromachining processes enabling wafer-level array microfabrication. It also improves the fabrication process controllability, reducing cost, and provides the capability for direct integration with front-end electronics with CMUT-on-CMOS and PMUT-on-CMOS techniques.

PMUTs have several advantages over CMUTs, as a DC bias voltage is not needed for operation significantly increasing the device's reliability. In addition, thin film PMUT membranes are associated with a higher capacitance and a lower electrical impedance that allows low voltage electronics integration and direct connection to wiring with acceptable impedance match [4]. During the last decade, PMUT arrays have been used in several research and industry applications including fingerprint sensing, intracardiac echocardiography, intervascular echocardiography, rangefinding and wireless power transfer [4]-[6]. In order to design a large PMUT array suitable for an application, an accurate simulation for the entire array and a design process are critical to observe the performance of the device for metrics including time and frequency response, bandwidth, and directivity. The high number of the membranes (~5000) in an array and the coupled physics of the membranes and surrounding medium leads to a simulation with many degrees of freedom (>50M) requiring significant time and memory. The ability to run parametric simulation fast and in parallel is critical during the design cycle and product development.

With the expanding interest in high density PMUT arrays, the study of acoustic crosstalk among the membranes is needed to characterize the array response, behavior, and bandwidth. In fact, the bandwidth of interest should be free of sharp transitions or corners especially on the edges. For example, in imaging applications, the sharp features inside the device bandwidth lead to a substantial length of ringing after the main response signal, which can cause image artifacts and defective area in the image reconstruction process [7][8]. Consequently, sharp features due to acoustic crosstalk need to be carefully minimized during the PMUT array design process [9].

In this paper we use OnScale, an efficient FEA solver deployed on cloud HPC platform, for a 64-channel PMUT array (5120 membranes) simulation that takes ~2_hours for the entire simulation without applying symmetry boundary condition.

II. High Performance Simulation Executed on the Cloud

Piezoelectric micromachined ultrasound transducers (PMUTs) designers often must investigate structural mechanics and acoustic phenomena separately when using common finite element method (FEM) and hybrid finite element method-boundary element method (FEM-BEM) simulation tools. A single model where all physics are coupled would enable more accurate simulations and insight into the KPIs of transducers behaviors. Accurate membrane displacement, piezoelectric voltage, charge, output pressure and other important factors of a single transducer or an array would be derived from a single model which better captures the real-world behavior of the design. OnScale is software tool enabling PMUT design engineers to access the necessary computational power to run a full 3D PMUT simulation. PMUTs are usually designed in an array configuration comprising an enormous number of membranes (up to 10000). Considering 50-µm membrane lateral size and having a 5-µm structed grid mesh size, each membrane will be meshed with 100 elements. For an array with 5000 membranes and 10 meshing elements along the membrane thickness (Z direction), the array will contain 5M (10x10x10x5000) nodes. In order to obtain accurate results for a full 3D FEM-based acoustic model, for each of those 5M nodes, 3 mechanical degrees of freedom (X, Y and Z) plus 1 electrical must be solved at each frequency/time step. The entire array contains roughly ~20M (5Mx(3+1)) degrees of freedom (DoF) resulting in several weeks of simulation time and huge RAM storage requirement and a complicated data post-processing with legacy FEA software.

The OnScale platform empowers the modeling, design, and prototyping process by providing Multiphysics solvers combined with High-Performance Computing (HPC) capability executed on the latest cloud technology. The cloud HPC enables 3D simulation instead of typical simplified 2D approximations which typically result in inaccurate simulations due to the exclusion of second-order effects such as crosstalk. By using OnScale, designers are able to run a parametric model and thus explore a variety of design parameters to optimize device performance in several ways. In addition, high-performance computing enables the entire array simulation to be performed on a die with encapsulation and surrounding medium enclosure (including air, water, etc.) thus allowing the accurate simulation of acoustic beamforming, crosstalk, and other array behaviors that cannot be obtained by extrapolation of an individual element. OnScale can also combine different solvers such as acoustics and thermo-mechanical to include the effect of temperature on the acoustic behavior of the array, device packaging and CMOS-transducer integration.

In addition, several methods can be used to accelerate a simulation study by using less time and therefore increasing the coverage and understanding of a given parameter in the device design. One method is to run the simulation on the cloud using cloud computing to run a range of models in parallel, significantly reducing the runtime for batch jobs. Another technique is the use of parallel computing architectures through Message Passing Interface (MPI) that allows the partitioning of each simulation through domain decomposition and the sharing of computing resources. OnScale combines these two methods, resulting in substantial increases in modeling and simulation speed.

III. PMUT SINGLE ELEMENT, ARRAY DESIGN AND SIMULATION SETUP

The device that has been used for the crosstalk study is a 64-channel PMUT array with a 5-10-MHz center frequency in immersion suitable for catheter-based medical imaging applications such as intracardiac echocardiography (ICE). There are several handheld and catheter-based medical devices that have been developed using MUTs in R&D labs and at industry scale [10]-[11]. The device's lateral size is set to be roughly $\lambda/2$ to avoid unwanted grating lobes and to optimize the device directivity [7]. The lateral size for each PMUT element is set to be 100-µm, and each element comprises 4 membranes. The membrane gap height is designed to be 2-µm to ensure the membrane can freely vibrate and does not contact the silicon substrate.

TABLE I. PMUT MEMBRANE PROPERTIES

Parameter	***Value***
Silicon thickness	1.8-µm
AlN thickness	1-µm
Gap height	2-µm
Top electrode thickness	0.2-µm
Bottom electrode thickness	0.2-µm
Membrane size	46x46-µm^2
Electrode size	36x36-µm^2
Number of memranes in element	80 (Fig. 1-b)
Number of elemenst	64 (Fig. 1-c)

The membrane is a 1.8-µm silicon (Si) layer coupled to 1-µm aluminum nitride (AlN) layer. The bottom electrode (BE) is 0.2-µm copper (Cu) and the top electrode (TE) is 0.2-µm aluminum (Al). The device can be fabricated by stack deposition of Cu/AlN/Al over a cavity-silicon-on -insulator (CSOI) wafer followed by an etching step. It is worth noting that molybdenum (Mo) is usually used to enhance the adhesion between electrodes and the Si/piezoelectric layer. The membrane geometry (Table 1) with a 5-µm water enclosure is depicted in Fig. 1-a.

The entire device with water load is meshed with a 2-µm element size in order to accurately capture the membrane behavior. In addition to a structed grid mesh, keypoints are used for the critical points in space to accurately map out the dimensions of the geometry. For the geometries and layers

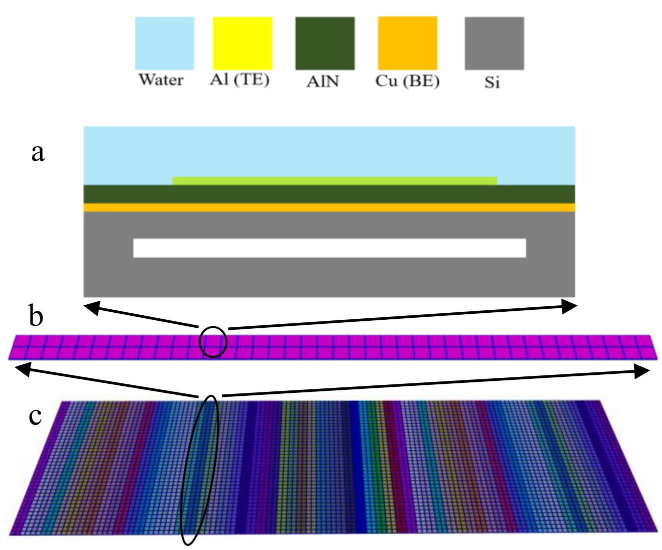

Fig. 1.a) Single membrane PMUT cross section. b) 1-D element consisting of 80 (2x40) membranes. c) A PMUT array comprising 64 1-D elements (64x80) membranes. Each 1D elements has a unique color.

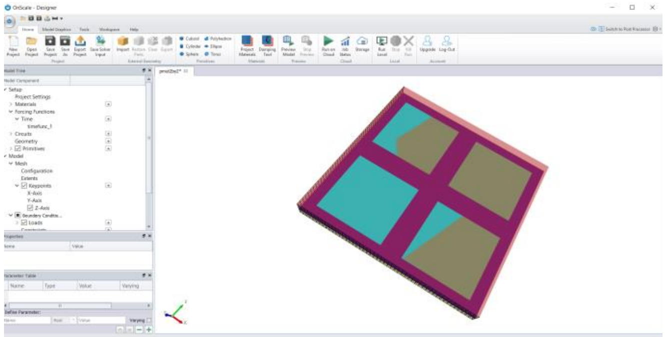

Fig. 2 The simulation setup in OnScale designer mode.

where physical dimensions have direct effect on resonant behavior such as the thickness of a piezoelectric layer or the gap height in electrostatic physics, we must ensure that the dimension is represented accurately. The array simulation is carried out in transmit (Tx) mode. The TE for all four membranes is connected to a circuit with a 50-Ω resistor excited by a tone burst signal of 1-cycle and 10-MHz center frequency. The bottom electrode is common ground. Six main boundary conditions are defined for the device; all the surrounding sides of the PMUT element (x_{min}, x_{max}, y_{min} and y_{max}) and bottom surface (z_{min}) are set to be fixed. The top surface is set to an impedance boundary condition. The 2x2 PMUT device in OnScale's designer mode is shown in Fig. 2.

The membrane displacement signal and FFT are depicted in Fig. 3-b and 3-c showing the device center frequency is around 10MHz with roughly 70% fractional bandwidth. The PMUT membrane vibrates in the Z-direction and based on flexural (d_{31}) mode behavior in PMUTs, the strain is perpendicular to the poling direction and electric field (Z-direction). The membrane displacement profile in Z-direction is also demonstrated in Fig. 3 showing that the maximum deflection happens at the center of the membranes.

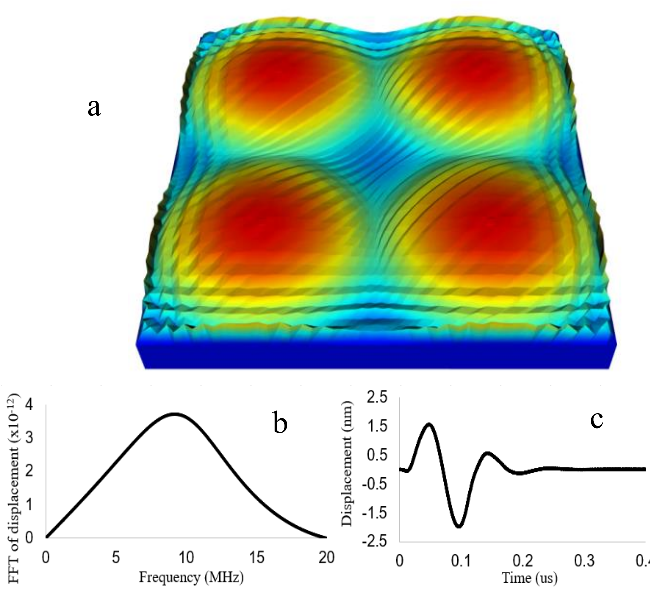

Fig. 3.a) Displacement profile of a single element (2x2 membrane) showing maximum displacement at the center of the membrane. b) FFT of the displacement of the membrane showing the PMUT has a center frequency around 10-MHz. c) Membrane vibration signal.

The simulation, which included ~120k degrees of freedom, took roughly 20 minutes on 16 cores (5 CHs) and 70 MB of RAM. It is worth noting since the 1 element simulation needs relatively small calculation memory, and MPI was not used.

IV. PMUT Array Crosstalk Study

After designing the single PMUT element for the bandwidth of interest, the 64-channel device (Fig. 1-c) is built in OnScale for FEA analysis. The device area is 2x6.4-mm^2 making it suitable for catheter-based medical applications such as ICE [2]. There are several ways to create the 64-channels (64x80=5120 membranes) in OnScale; the array command in designer mode, code-based array construction in analyst mode and cad file import from other platforms such as SoftMEMS [12]. SoftMEMS is a MEMS process modeling tool capable of applying fabrication processes to the GDS mask layers to generate a faithful 3D representation of a MEMS device after fabrication.

The bottom electrode is common ground for all 64 elements and each long 1-D element (Fig. 1-b) has a separate top electrode. In order to observe the widest crosstalk

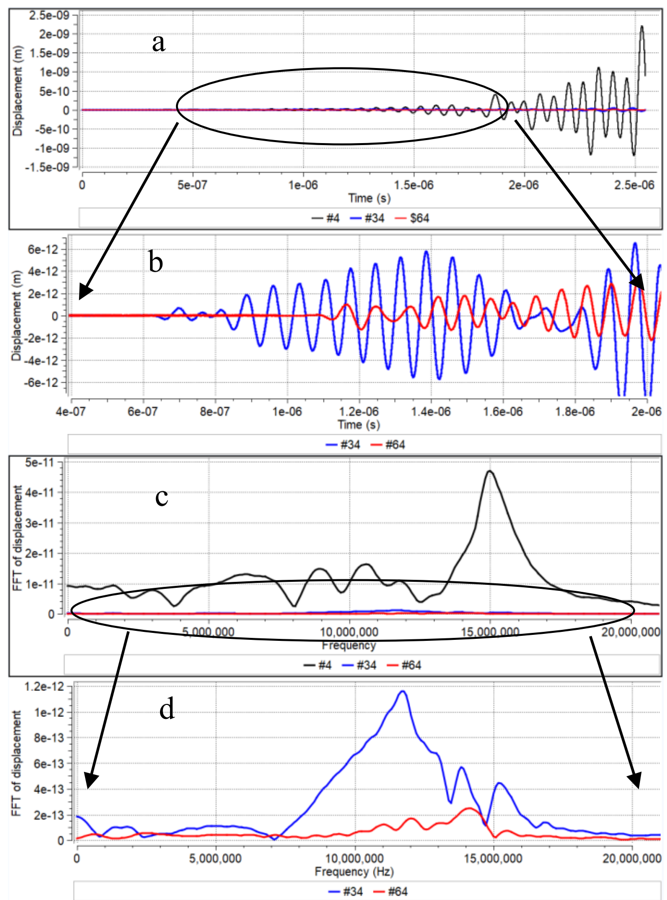

Fig. 4.a) The crosstalk displacement of one close element (#4), one middle element (#34) and the farthest element (#64) from the excited element (#1). b) The high-resolution displacement graph of #34 and #64 shows crosstalk effect partially suppressed when the acoustic wave travels. c) The FFT of displacement implying vibration in a higher frequency than device center frequency d) High-resolution graph for FFT of displacement (#34 and #64).

affecting the array behavior, a 1-V excitation signal at 10-MHz is applied on the first element (leftmost element in fig. 1-c) and the displacement and output voltage are calculated for several elements (4th, 34th and 64th). Fig. 4 demosntrates element displacement and its FFT for elements that have not been excited directly by an input voltage. The crosstalk displacement is larger on the closet neighbors of the excited element and becomes smaller over farther elements. The crostalk effect shows delay for each element as it takes time for the wave to travel across the layers. For example, by considering a shear velocity of 6000-m/s for AlN, it takes about 1-µs for an acoustic wave to travelse the distance from the first element to the last element (64th). The crosstalk for the closest elements are significantly higher (black curves in Fig.4-a and 4-c) than middle (#34) and the last (#64) element. It is also clear that crostalk begins later for farther elements. Fig. 4-c and 4-d show that crosstalk typically occurs in higher frequncies deteriorating the device response and having a negative impact on image resolution. It can additionally affect other areas of device performance and MEMS-CMOS integration that are susceptible to high-frequency noise.

The entire simulation was run on 640 cores and took roughly 2 hours for a 2.5 µs simulation time. The simulation used about ~2 GB RAM and had 20 million degrees of freedom. There are several ways to reduce the acoustic crosstalk in an array [13]-[14]. One common technique is to increase the pitch size by increasing the distance between neighboring membranes in order to mitigate the effect of the travelling surafce wave. Fig. 5 compares the crosstalk in element #34 and #64 when the distance between each membrane is increased by 3-µm. In this case, the crosstalk amplitude is reduced by 3x.

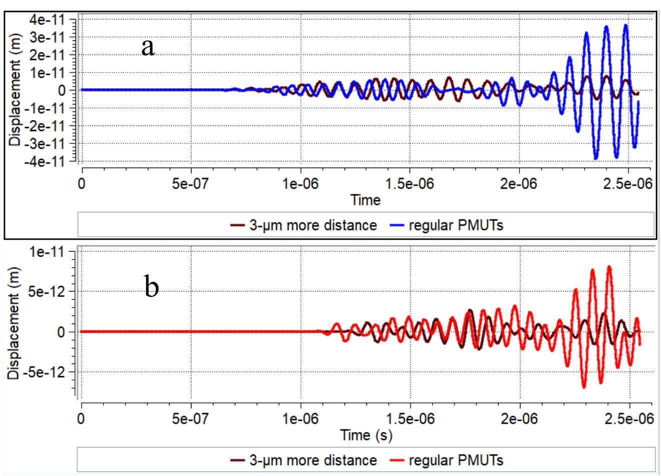

Fig. 5.a) The crosstalk displacement is significantly reduced when the distance between each membrane increases for element #34 and b) The effect of increasing pitch size for element #64

V. Conclusion

OnScale is used as a high-performance computing (HPC) platform for the large-scale simulation of a 64-channel PMUT array comprising 5,120 membranes suitable for an ICE catheter. The individual element shows a 10-MHz center frequency with 70% fractional bandwidth. Element #1 is excited with a 1-V tone burst signal of 1-cycle at 10-MHz and the displacement of element #4, #34, and #64 have been simulated showing crosstalk occurs at higher frequencies than device center frequency. The crosstalk effect is reduced for elements farther from the excited element, as expected. The effect of pitch size on crosstalk is also simulated showing that a larger pitch size reduces crosstalk and improves device performance.

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