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High Degrees of Series Capacitors in Bulk Power Transmission Systems Need Special Protection Principles

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***Abstract*— The paper describes relaying problems in transmission systems with a high degree of series compensation. The usability of and limits for the use of distance protection will be discussed and experiences gained from real-time tests are presented. The possibilities offered by modern relays, so called two-in-one relays, consisting of communication based differential protection combined with backup distance protection will be shown. By the use of these modern relays, very low fault clearing times like required in protection codes for highly loaded transmission systems can be fulfilled.**

***Index Terms*—Transmission system, series capacitor, voltage reversal, current reversal, distance protection, differential protection, communication, trip time reduction**

I. INTRODUCTION

SERIES compensation is widely used to improve the transmission capability of long distance overhead transmission lines and the overall network efficiency /1,2,3/. These capacitors do not only influence the operational behavior of the power system, but also the behavior during short circuits. Effects like voltage inversion are well known and covered in distance protection relays by determining the direction of the fault with memorized voltages. Depending on the location of the capacitor, its size, the protection level of the platform protection, and the impedance of the source, current inversion is also possible. If this current inversion occurs, new problems arise for the protection scheme. High resistive earth fault protection, fault locator and also the differential protection will be affected in different ways. This was proven by RTDS real-time simulation tests. The paper explains theory and shows the different protection principles.

II. INTRODUCTION

Modern techniques for differential protection to be applied in long transmission lines have been recently developed using new communication standards eliminating the myth that this technique could only be used for transmission lines shorter than 100km, /9/.

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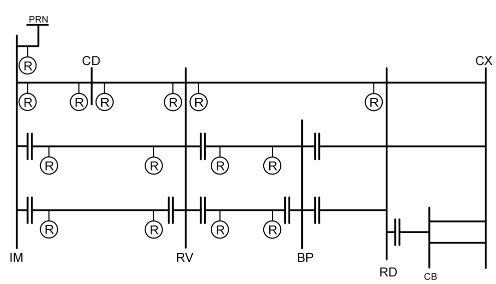
A practical experience has been tested where a differential protection was used to protect a 230kV line, 202km long, and 70% series compensated, located in a complex system.

The test case used for this paper is the line Itumbiara-Rio Verde (IM-RV) 230kV, circ.2, 70% series compensated, 220km long. Adjacent to this line there are other parallel series compensated lines, making it difficult for the conventional distance and overcurrent protections.

The reason to choose the line mentioned above is that the system where the line is located is a very complex one. In the middle 1970´s there was only one 138kV line interconnecting the power systems of four different Companies, CELG, FURNAS, ELETRONORTE, and CEMAT, and gradually was strengthened over the years, being 3 circuits of 230kV, and one of 138kV in the early 1990´s, and finally in 2006 with a 500kV line in parallel connecting Itumbiara and Cuiabá substations.

In order to make it possible for the power to flow in the 230kV lines, even in some contingencies of the 500kV circuit, the use of series compensation was considered necessary along these lines.

Due to the implementation of these compensations the existing protection schemes, many with inadequate relays for compensated lines, needed to be substituted by appropriate protection systems.



® Relays under test

Fig. 1. Simulated 230kV FURNAS and Eletronorte network

According to the specifications the new protection system was supplied with distance and directional overcurrent functions appropriate for series compensated lines. Considering the power system of Fig. 1, the new protection systems were evaluated through a series of simulation tests using the Siemens Real Time Digital Simulator (RTDS), in Erlangen, Germany.

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Fig. 1 shows, that line Itumbiara-Rio Verde, 230kV (IM-RV), circ. 2, has 70% compensation at the Itumbiara (IM) side. The high degree of compensation, concentrated in only one terminal, is one of the most severe cause of problems. Especially resistive or phase to phase faults close to the capacitor did not lead to operation of the bypass of the series capacitor. Only with the delayed reach of MOV's thermal limit and thus bypass operation, distance protection could trip the fault. So the total fault clearing time was higher than 150ms, which is the maximum for a 230kV line according to the Protection Code of the Brazilian National System Operator ONS. Therefore, it was agreed between customer and vendor that the distance protection 7SA6 should be replaced by the differential protection 7SD5 which additionally has a distance backup function. An optical communication link to be used between both terminals in addition to the latest functional resources of the 7SD5 will make it possible to communicate over a distance of 220km.

III. Series Capacitors

A. Locations of capacitors and instrument transformers

Series capacitors can be located with:

- high compensation in the middle of the line
- low compensation at both ends of line
- high compensation at one end of the line
- any compensation on an adjacent line

When capacitors are placed in the substation, the position of CTs and VTs is also important. We find

- CTs and VTs line side
- CTs and VTs busbar side
- CTs busbar side and VTs line side

of the capacitor. If CTs and VTs are on different sides of the capacitor, the effective measuring position is the position of the VT.

B. The protection level of series capacitors

Normally the protection level is selected that we expect no gap and bypass operation for external faults. As a consequence, most but not all internal low resistive faults lead to a bypass, whereas high resistive faults limit the fault current to an amount, where the capacitor remains in service. Whenever the bypass operates, the line is uncompensated /6/.

C. Effects of series capacitors on the short circuit

With series capacitors the following issues can occur:

- reduced fault impedance
- increased fault impedance
- voltage inversion
- current inversion
- overvoltage

1) Reduced fault impedance

Whenever the capacitor is between the measuring location and the fault, a wrong impedance is measured. This and the effect of subsyncronous frequency are described in detail in /8,10/. Care must be taken with capacitors on adjacent lines, where an intermediate infeed can intensify the effect of fault impedance reduction.

2) Increased fault impedance

When a capacitor is between the measuring location and the fault, and the remaining inductive impedance is smaller than the capacitive impedance, it may be necessary to increase the zone reach to a value higher than the capacitor's impedance. This may be interesting for reverse zones to see busbar faults when VTs are located line side.

3) Voltage inversion

When a capacitor is between the measuring location and the fault, and the remaining inductive impedance is smaller than the capacitive impedance the measured impedance is capacitive. This leads to a voltage inversion. As described in /7,8/, determining the direction with memorized voltages can solve this problem, unless current inversion occurred.

4) Current inversion

When the complete short circuit loop has a resulting capacitive impedance, the short circuit current is capacitive, what is called current inversion. Current inversion occurs mainly, if capacitors with high impedance (used for long lines with a high compensation degree) are placed at one of the ends of the line. Together with strong sources, a short circuit can change from the typical ohmic-inductive to an ohmic-capacitive nature, so that the short-circuit current depends on and is limited mainly by the series capacitor. Depending on the protection level of the MOVs and gaps, the capacitors will not be bypassed immediately after short-circuit inception, which can result in a wrong direction determination using memorized voltages.

5) Overvoltage

The series capacitor and line and source impedance behave as an oscillating circuit where the resonant frequency is tuned by the line impedance between the capacitor and the fault location. Unexpected overvoltages may occur.

IV. Distance Protection on Series Compensated Lines

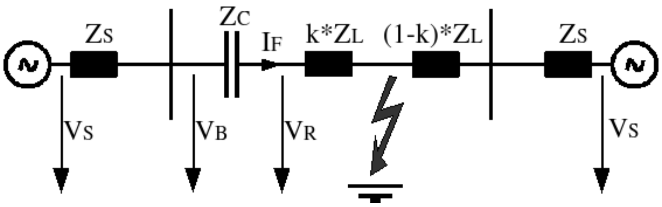
In Brazilian networks we can find large series capacitors at the beginning of lines. Together with strong sources this leads to current inversion. Normally we would expect these fault currents so high that the capacitor is bypassed immediately. During the TNA tests we found some situations, especially 2 phase faults and some resistive faults close to the capacitor, with currents small enough, not to trigger the bypass.

A. Current inversion

In the examined network, current inversion without bypass breaker operation occurred, which was not observed before.

Chapters IV.A.1 to IV.A.5 show clearly, that distance protection, independent of the installation point of the VTs, can not be used for series compensated lines, if the possibility of current inversion will exist.

1) VTs line side and faults in forward direction



V_S source voltages
V_B busbar voltage
V_R relay voltage
V_M memorized voltage
I_F fault current

Fig. 2. Simplified short-circuit case under no load condition, fault in forward direction

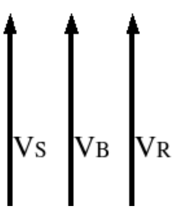


Fig. 3. Voltage phasors pre to fault under no load condition

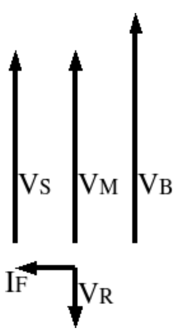


Fig. 4. Voltage phasors during fault and fault current IF

Fig. 3 shows the voltage phasors pre to fault under no load condition. The source voltage V_S, the busbar voltage V_B and the relay voltage V_R are in phase.
Fig. 4 shows the voltage phasors during fault. The memorized voltage V_M is always identical to the relay voltage V_R pre to fault. Due to the capacitive short-circuit current, the relay, that makes the directional decision with actual short-circuit current and memorized voltage (V_M, I_F), will see the forward fault in reverse direction.

2) VTs line side and faults in reverse direction

In this case we see the classical voltage inversion, so the memorized voltage has to be used. Otherwise busbar faults behind the capacitor would be seen forward.

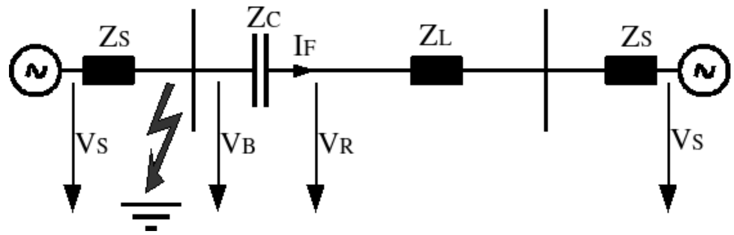


Fig. 5. Simplified short-circuit case under no load condition, fault in reverse direction

3) VTs busbar side and faults in forward direction

From the phasor diagrams acc. to Fig. 3 and 4, it can be seen, that the pre-fault voltage and thus the memorized voltage at bus side is the same as on line side. Also in this case, the memorized voltage will lead to a wrong directional decision.
For faults in the middle of the line and a source which is more weak due to a changed switching state, we have the classical voltage inversion situation:
$X_C + k * X_L < 0$
$X_S + X_C + k * X_L > 0$
Here we will need the memorized voltage and non-memorized voltage is also not a solution.

4) VTs busbar side and faults in reverse direction

For this case, the relay can operate with memorized voltage and in case, that there is no capacitor somewhere reverse, also with non-memorized voltage.

5) VTs line side, faults between the capacitor and the CTs

For faults between CT and the capacitor, the relay will see fault current I_{F1} , but a voltage of
$V_R = X_C * I_{F2}$
The measured impedance will be
$X_M = V_R / I_F = X_C * I_{F2} / I_{F1}$
which has nothing to do with any real impedance. We can assume that $I_{F1} > I_{F2}$, so that the absolute value of the measured impedance is smaller than X_C and smaller than the overreach zone Z1B. Since the directional decision is made with the memorized voltage, the fault was always seen forward and we observed a trip in all cases.

B. The choice of zone reach settings and use of teleprotection schemes

The first requirement for the possible use of distance protection in series compensated networks is, that current inversion can be excluded as shown in chapter IV.A.
Regarding typical zone reaches in uncompensated networks a zone reach of Z1 of 80%-90% of the line length will be used. For series compensated networks, the reach has to be reduced dramatically. Even in cases where there is no capacitor in front of the relay on the protected line, capacitors on adjacent or parallel lines demand a zone reduction.

As a consequence, a teleprotection scheme is absolutely necessary and the distance protection function is reduced to a pure directional comparison function. Trip times for any fault position on the protected line are 35 to 45 ms including signal transmission time.

V. Directional Earth Fault O/C Protection on Series Compensated Lines

A. Making the directional decision

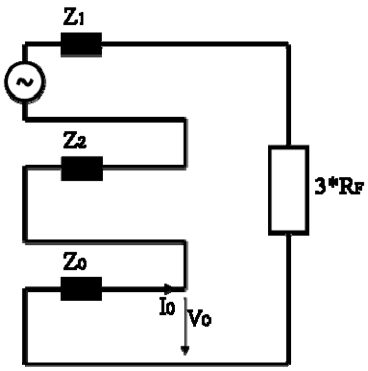
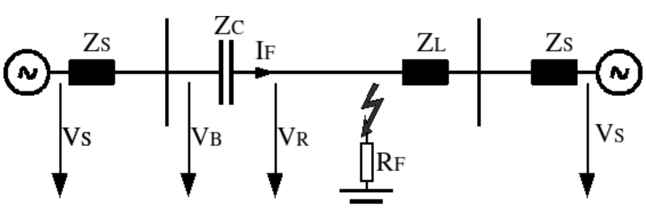


Fig. 6. Equivalent circuit in symmetrical components for earth faults

The directional earth fault overcurrent operates mainly with zero sequence voltage and current.
The equation
$Z_0 = - V_0 / I_0$
gives us the source impedance, not the fault impedance. If the fault is in reverse direction, the current I_f changes its direction. As a result, the measured impedance has negative reactance. Or the other way around: If the measured impedance has positive reactance, the fault is forward. In case of negative reactance, the fault is reverse.

B. Series compensated lines and VT line side

Figure 7 shows the circuit as single line in original components and in symmetrical components. Even if the capacitors are not in the ground path, they have a zero sequence impedance and
$Z_{C1} = Z_{C2} = Z_{C0} = Z_C$.
With high resistive faults, fault currents are low and bypass operation is not expected.



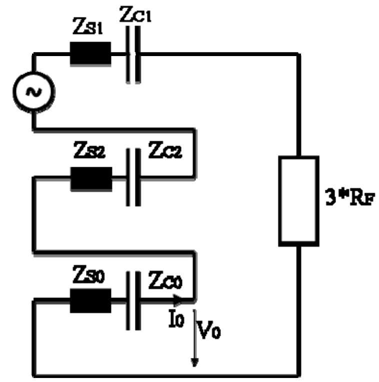


Fig. 7. Simplified short-circuit case with a high resistive forward earth fault with VT line side and representation in symmetrical components.

1) Low source impedance and high compensation degree

In some cases, especially at high compensation rates, the capacitive impedance can be higher then the inductive source impedance. Grounded transformers, connected to the busbar, lower the zero sequence impedance also. So it may happen, that the resulting zero sequence impedance is capacitive (even when positive and negative sequence impedance are inductive).
In this case the protection will measure forward faults always as reverse!

On the other hand, if the fault is really reverse, the effective source $Z_L + Z_S$ is line side and inductive and the calculated impedance therefore is negative inductive. This means, the fault is measured correctly reverse.

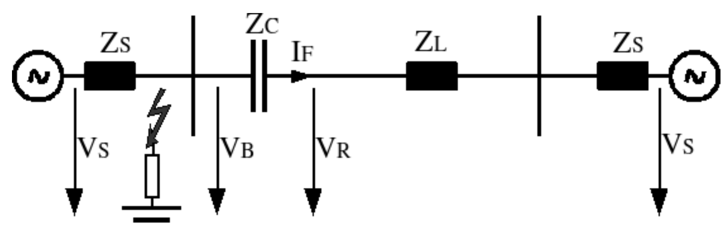


Fig. 8. Simplified short-circuit case with a high resistive reverse earth fault with VT line side

2) High source impedance and low compensation degree

As long as the resulting impedance is considerable inductive, everything operates correctly.

C. Series compensated lines and VT busbar side

In this case, we see the left source clearly inductive. The resulting source impedance for reverse faults is always reactive, since the complete line impedance is higher than the capacitive impedance. The directional overcurrent earth fault protection will operate correctly.

VI. Overvoltage Protection

A common design rule for the capacitor bank protection is the aim, not to trip for external faults.

At the line side a voltage, calculated as follows (neglecting the ohmic parts of the impedances) will occur:

$V_R = I_F * X_L$

$V_{S1} = I_F * (X_{S1} + X_C + X_L)$

$V_R / V_{S1} = X_L / (X_{S1} + X_C + X_L)$

As an example we use:

$X_{S1} = 0.1 * X_L$

$X_C = -0.7 * X_L$

$V_R / V_{S1} = 1 / (0.1 -0.7 + 1) = 2.5$

In this example the voltage rises to 250%. This may be dangerous for the equipment. If an overvoltage protection with standard settings is connected to a VT line side, it may trip instantaneously at an external fault.

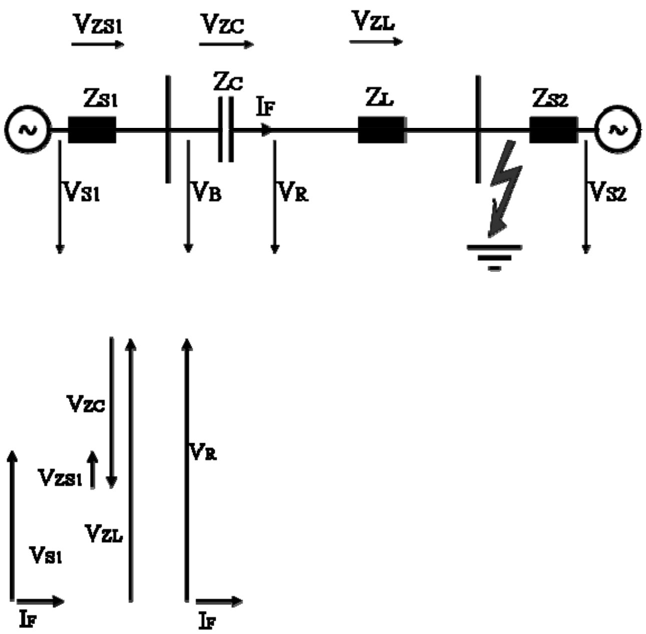


Fig. 9. Simplified short-circuit case with external fault and corresponding phasor diagram

VII. Differential Protection

In a lot of discussions between protection engineers one can can hear statements, that differential protection is not suitable for series compensated lines, because current inversion on one side leads to a capacitive short circuit current. With inductive fault current on the other side the resulting fault current at the fault location and thus the differential current will be zero and the relay will not trip.

The following chapters VII.A to VII.C will answer the two main questions:

- Is zero short circuit current possible and what would be the conditions for?
- Is it possible to find differential protection characteristic for operation on all internal metallic faults?

A. Is zero short circuit current possible?

Can it happen, that the capacitive short circuit current on one side has the same size as the inductive fault current on the other side?

Acc. to Fig. 10, we assume the same source voltage V_S on both sides

$I_{F1} = -I_{F2}$

$V_S / (X_{S1} + X_C + k*X_L) = - V_S / (X_{S2} + (1-k) * X_L)$

$X_{S1} + X_C + k*X_L = -X_{S2} -X_L + k*X_L$

$X_C = -(X_{S1} + X_{S2} + X_L)$

So the capacitor must not only compensate 100% of the line impedance, but also both source impedances. This is not realistic, so zero short circuit current is not possible.

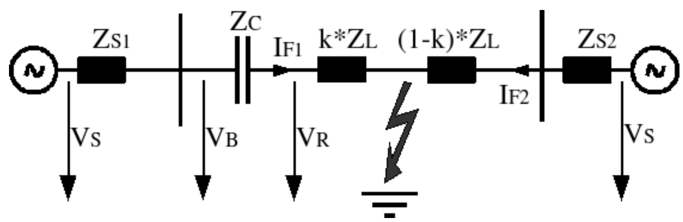


Fig. 10. Simplified short-circuit case with fault on the line

B. Check of slope of differential protection characteristic

We will check, if there is any point on the line where the stabilization current is too high compared to the differential, so that no trip can happen.

Although there are differential protections from many manufacturers, that calculate the stabilizing quantities on different principles, the differential current is always calculated according to Kirchhoff's law. For a rough calculation we use for STAB the most classical

$STAB = k_{STAB} * (|I_{F1}| + |I_{F2}|)$.

See the currents on different points on the line. The most critical point is on the line side of the capacitor with k=0. Here the capacitive current

$I_{F1} = V_S / (X_{S1} + X_C + k*X_L)$

is minimum and increases rapidly as a hyperbola to theoretically infinite at the resonant point of capacitor and line section plus source. The inductive current

$I_{F2} = V_S / (X_{S2} + (1-k) * X_L)$

is also minimum and increases like a hyperbola but the asymptote is theoretically inside the source, so that the increase is not so rapid.

with k=0:

$I_{F1} = V_S / (X_{S1} + X_C)$

$I_{F2} = V_S / (X_{S2} + X_L)$

with $X_{S1} = X_{S2} = 0.1 * X_L$ (as an example for strong infeeds) and $X_C = -0.7 * X_L$ we find

$I_{F1} = V_S / X_L * (1 / (0.1 - 0.7)) = -1.66 * V_S/X_L$

$I_{F2} = V_S / X_L * (1 / (0.1 + 1.0)) = 0.91 * V_S/X_L$

$DIFF = | -1.66 + 0.91 |* V_S/X_L = 0.75* V_S/X_L$

$STAB =(| -1.66 | + | 0.91 |)* V_S/X_L = 2.57* V_S/X_L$

$k_{STAB} < 0.75 / 2.57 < 0.29$

In this case, a fault can be tripped if the slope is lower than 0.29. Of course, this must be checked for 1, 2 and 3-phase faults, with the correct formula of the relay and the necessary safety margin. Here it should be mentioned, that moving the fault position towards right, will increase I1, which will finally lead to a trip of the capacitor protection and a bypass of the capacitor. For this case, and faults on the right side of the line, only inductive currents appear, which is the standard situation without problems.

Especially in networks with high compensation degree and strong infeeds with small source impedances, the point close to the capacitor lineside must be checked, that the slope of the differential protection is low enough. If this is the case, the differential protection will trip all faults without any delay.

C. High resistive faults

Looking at high resistive faults, we see that the voltage drop at the fault position is negligible, and so the fault current and thus the differential current is determined only by the resistor. The contribution of the fault current from left and right is not known, but they are superposed to the load and we can say with the general formula

$| a + b | =< | a| + | b |$

$DIFF = | I_F |$

$STAB < | I_L | + | I_L | + | I_F |$

$DIFF > k * STAB$

$| I_F | > k * (| I_L | + | I_L | + | I_F |) > k * STAB$

$| I_F | / | I_L | > 2k/ (1-k)$

As an example, the bias k of 20% will allow a fault current of 50% of load current. There are modern differential relays on the market which allow a bias of less then 5% in the range of normal load current. So these relays are as sensitive as an overcurrent earth fault protection relay.

Of course, also here the exact formula of the relay applies with the necessary safety margin.

VIII. Fault Locator

A correct working fault locator is evident especially for the protection of long lines, as the location must be inspected after the fault. But fault locators based on impedance measurement are using faulty voltages and are influenced by the capacitive impedance.

A fault on the left busbar is indicated at the right relay by 70% forward. 70% is the impedance of the capacitor and 'forward' the result of the wrong directional measurement. The right relay however measures correctly forward and sees the fault at 30%, since the capacitor stays in service for external faults. So the results are plausible, but nevertheless wrong.

The fault localization can be improved by using a fault locator which uses data from both line ends.

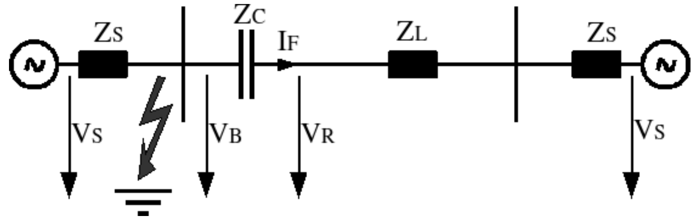


Fig. 11. Simplified short-circuit case with external fault

IX. Transient Network Analyzer (TNA) Tests

The TNA test laboratory in Erlangen, Germany is equipped for protection testing with a Real Time Digital Simulator RTDS for protection testing with 2 racks. The considered network as shown in Figure 1 was simulated with more than 10 lines and 9 series capacitors. Hundreds of tests were made during many weeks with distance and differential protection to verify settings and to document the operation.

X. CONCLUSION

We have seen, that the combination of distance and directional earth fault overcurrent is useful, especially for all faults, where bypass operation occurs. Nevertheless both systems need a communication system, eg. PLC. If a modern communication system with 64kBit (128kBit recommended, 512kBit optimum) is available, a differential protection could clear all metallic and resistive faults in 10ms to 20ms and high resistive faults in less than 40ms.

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XII. Biographies

Volker Henn, born 1958 in Germany received his Dipl.-Ing. degree in Electrical Engineering from the University of Karlsruhe, Germany in 1985. He worked as System and Development Engineer at Siemens AG, Erlangen/Berlin from 1985 to 1990. Since 1991 he works as a Consultant and Senior Expert for Power Technology at Siemens Energy. His main interests are real-time simulation, relay testing and fault analysis.

Rainer E. Krebs, born 1958 in Germany (member of VDE, CIGRE, IEEE, IEC and DKE), received his Dipl.-Ing. degree from the University of Erlangen in 1982. From 1983 to 1990 he worked as an assistant professor at the Institute for Electrical Power Supply at the same University. In 1990 he received his Dr.-Eng. degree in Electrical Engineering. 1990 he joined Siemens AG, Power Transmission and Distribution, System Planning Department. Since 1998 he is director of the System-Protection and System-Analysis Tools Department and since 2006 he is ‘Principal Expert for Power Technologies’. In parallel he started in 2003 as lecturer at the University of Magdeburg. Since 2008 he is honorary Professor for System Protection and Control at the same University.

Gustavo Arruda, was born in Recife, Brazil, in 1957. He received a BSc in Electrical Engineering from Federal University of Pernambuco in 1980. Since 1982 he has been with CHESF where he is presently the manager of the Protection and Control Division. His main interests are digital simulations for testing relay schemes, and the application of software based tools for the investigation of relay performance.

Ricardo Dutra, born 1956 in Brazil, received his Dipl.-Ing. degree from the IME – Instituto Militar de Engenharia in 1979. and has been working by FURNAS since 1980. He also applies classes the post graduated course at Rio de Janeiro Federal University. He works as supervisor, consultant and project manager at the Protection and Control Division. He has a great experience on design, settings, commissioning and operating protection systems. His main interests are on applications of digital relay schemes and on software tools for evaluate relay performance.

Paulo Cesar G. Campos, received his BSc in Electrical Engineering in 1981, postgraduate in Power System Automation from Federal University of Bahia in 1996 and postgraduate in Power System Protection from Federal University of Itajubá in 2003. He has been working at Eletronorte since 1986 at the Protection, Control and Automation Department. His main interests are digital simulations for relay scheme tests and the application of protection.