Paper accepted for presentation at 2009 IEEE Bucharest Power Tech Conference, June 28th - July 2nd, Bucharest, Romania

Power System Reconfiguration Based on Multilevel Graph Partitioning

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***Abstract*—Area partitioning that splits a power network into self-sufficient islands is an emergency control to stop the propagation of disturbances and avoid cascading failures. This paper provides a survey of the state-of-the-art of power system islanding techniques and proposes the application of a multilevel graph area partitioning algorithm that are applicable to very large power grids. As an emergency control, network partitioning enhances the capability of a power system to withstand extreme and vulnerable operating conditions. The proposed algorithm has been simulated on two test systems, one with 200 buses and the other with 22,000 buses. The results indicate that the proposed algorithm is highly efficient.**

***Index Terms*—Emergency control, Power system islanding, Multilevel graph partitioning, Cascading events**

I. INTRODUCTION

An analysis of recent large scale blackouts in North America, Europe, and other countries shows that following the initiating contingencies, cascaded events may occur, leading to catastrophic power outages. It is important to take proper remedial actions to alleviate the vulnerable operating conditions in a power system in order to avoid a catastrophic outage. Reconfiguration can be viewed as an emergency control against cascading events. In anticipation of a worsening operation condition, the power network can be partitioned into two or more subsystems. When a major problem occurs in a subsystem, the remaining systems can still operate in an acceptable condition. Such a network reconfiguration strategy can enhance the capability of a system to “absorb the shock” and avoid catastrophic failures.

A partitioning algorithm is proposed in [1]. An automatic islanding approach that determines the islands from the identified slowly varying coherent groups of generators is reported in [2]. A partition strategy using minimal cut sets with minimum net flow is proposed in [3]. A graph theory-based islanding approach that combines the slow-coherency-based generator grouping algorithm is given in [4]. A framework for a centralized and proactive controlled islanding strategy can be found in [5]. A three-phase method utilizing ordered binary decision diagrams (OBDDs) to find proper islanding strategies is proposed in [6].

An important objective in partitioning a power network is to identify optimal cut sets of the sub-networks while the electrical interdependency between sub-networks and the power imbalance within sub-networks are minimized. By graph theory, this task involves partitioning of a weighted graph into several smaller graphs with evenly distributed weights and minimized edgecut. Since a power network can be viewed as a weighted graph with buses and transmission lines being vertices and edges, respectively, reconfiguration can be formulated as a graph partitioning problem. Several graph partitioning-based system islanding approaches have been proposed [6-9]. Most graph-theoretic islanding approaches involve a graph simplification stage for a large scale power system in order to reduce the computational complexity. However, the simplification process also leads to a loss of useful information, further reducing the accuracy of partitioning.

In this paper, a highly efficient area partitioning algorithm is proposed which is inspired by the multilevel partitioning technique from the VLSI field. With the proposed area partitioning algorithm, two islands of a 22,000 bus power system can be identified in 0.1s without simplification of the power network. The fast computational speed of the proposed algorithm makes it feasible to determine the partitioning strategy and identify the new network configuration in a real-time environment. A conceptual architecture for the proposed area partitioning algorithm is also proposed.

The organization of this paper is as follows: Section II provides an overview of the multilevel graph partitioning algorithm, the proposed graph theoretic area partitioning scheme, and the architecture of the proposed control system. Section III gives the simulation results using a 200-bus and a 22,000 bus power system model. Section IV provides the conclusion and a discussion of the future work.

II. GRAPH THEORY BASED AREA PARTITIONING

A. *Multilevel Graph Partitioning*

The graph partitioning problem is known to be NP-complete and it has many applications in scientific and engineering areas. Many graph partitioning algorithms have been developed. However, some of the algorithms are expensive for large graphs in terms of CPU time . The multilevel graph partitioning scheme [11] is the state-of-the-art technique that significantly reduces the computation time while generating high quality partitions.

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978-1-4244-2235-7/09/$25.00 ©2009 IEEE

The multilevel partitioning scheme does not partition the original graph directly. Rather, it first reduces the size of graph through a number of levels by collapsing vertices and edges. Then, the condensed graph is partitioned. Finally, a procedure is used to propagate and refine the solution through successive levels to the original graph.

Consider a weighted graph $G_0 = (V_0, E_0)$. The three stages of a multilevel partitioning scheme, as shown in Fig.1, are summarized here.

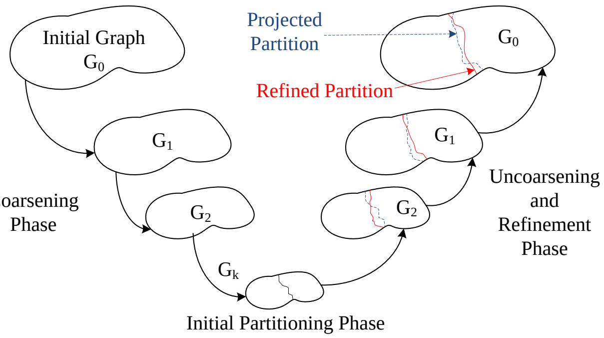

Fig. 1. Multilevel graph partitioning

1. Coarsening Phase. The initial graph G_0 is transformed into a sequence of smaller graphs G_1, G_2… G_k such that $|V_0| > |V_1| > |V_2| > \ldots > |V_k|$. A simple way to obtain the coarse graph is to group the vertices of the graph into disjoint clusters and collapse the vertices of each cluster into a single vertex.

2. Partitioning Phase. A partition P_k of the coarsest graph $G_k = (V_k, E_k)$ that minimizes the edge cut and satisfies the balancing constraints is computed. Since the size of coarsest graph G_k is small, various partition algorithms, e.g., recursive bisection, can be used to obtain the partition P_k.

3. Uncoarsening and Refinement Phase. The partition P_k of the graph G_k is successively projected back to the original graph G_0 by going through intermediate graphs G_{k-1}, G_{k-2}… G_1, G_0. At each step of the uncoarsening phase, the partition is further refined to reduce the cut set and improve the quality of solution.

B. *Graph Theory Based Area Partitioning*

Based on the multilevel graph partitioning scheme discussed above, an efficient power network area partitioning algorithm is developed. The proposed algorithm involves two stages.

At the first stage, the network is modeled as an edge-weighted graph. Each bus of the power network is a vertex of the graph, each transmission line on the one-line diagram is an edge. The weight of an edge is the absolute value of the MW power flow on the transmission line. The basic graph structure of the power network can be constructed off-line. The final graph can be further updated with information of the topological changes and weights for the edges. Since line flows resulting from contingency analysis are used to determine the islanding configuration, the proposed area partitioning algorithm has the ability to determine the next configuration based on vulnerability considerations.

At the second stage, a multilevel recursive bisection algorithm is used to partition the weighted graph into several isolated areas. In this stage, a circuit partitioning tool, pMETIS that implements a multilevel recursive bisection algorithm is utilized [12]. pMETIS is a professional graph partitioning software tool that has been widely used in VLSI design and its performance in terms of the cut size and computational time is excellent. As an example, it is capable of partitioning a graph with 15,606 vertices and 45,878 edges into 256 subareas with minimum cut set in 3.13 second on a PC [12]. With the fast computational speed, the proposed area partitioning algorithm has the potential to compute the system islanding configuration on-line.

The optimal number k of isolated areas is selected from several area partitioning scenarios ranging from two isolated areas to k^{max} isolated areas, where k^{max} is the largest acceptable number of isolated areas that a system can be divided into. The optimal k area partitioning is the one with minimum loss of load among all acceptable partitions. If load shedding is combined with this area partitioning algorithm, the optimal k area partitioning minimizes load shedding compared to all other acceptable partitions.

C. *Controlled Islanding Architecture*

The controlled islanding actions can be initiated by a special protection system (SPS). A conceptual relaying system for controlled islanding is illustrated in Fig. 2.

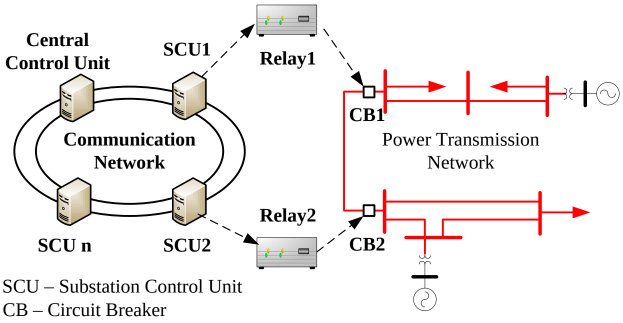

Fig. 2. A conceptual relaying architecture for controlled islanding

This system consists of one central control unit (CCU) and several substation control units (SCUs). CCU acquires system data such as topology and power flows from SCUs and generates the system separation strategy using the proposed area partitioning algorithm. Power flow data can be obtained from on-line Energy Management Systems (EMSs). SCUs receive the system separation command from CCU and send the breaker opening signals to specific auxiliary relays. These relays then send the tripping signals to the appropriate circuit breakers. To ensure reliable and fast information transfer between CCU and SCUs, a dedicated communication network, such as a synchronous optical network (SONET), would be needed.

D. *Emergency Control with Area Partitioning*

The proposed partitioning scheme consists of a controlled islanding scheme and a load shedding scheme. After the system is separated into islands, load rich or generation rich islands may exist. At a generation rich island, if the system frequency violates the operating constraint, the excess generation can be removed by a rapid response of the speed governor or generator tripping. At a load rich island, load shedding is required to avoid a frequency decline caused by generation shortage [10].

In response to the disturbance, the optimal configuration and the corresponding boundaries for the islands will be determined by the proposed graph theoretic area partitioning algorithm. If a load rich island exists in the new configuration, a power flow study on the islanding configuration can be used to determine the amount of load to shed.

The procedure shown in Fig. 3 demonstrates how the proposed configuration control system can help to absorb a shock, block the propagation of disturbances, and avoid a catastrophic failure. Assume the system is initially operating in a normal state. When a major problem occurs in the system, a cascading sequence of events including line tripping, overloading of other lines, protection system malfunctions, and generator tripping events might be triggered. If it is triggered, the system may enter a vulnerable state. If the controlled islanding strategy along with load shedding is applied according to the real time vulnerability assessment result, the impact of disturbances can be isolated to within one island and the remaining system will survive the shock without losing too much load.

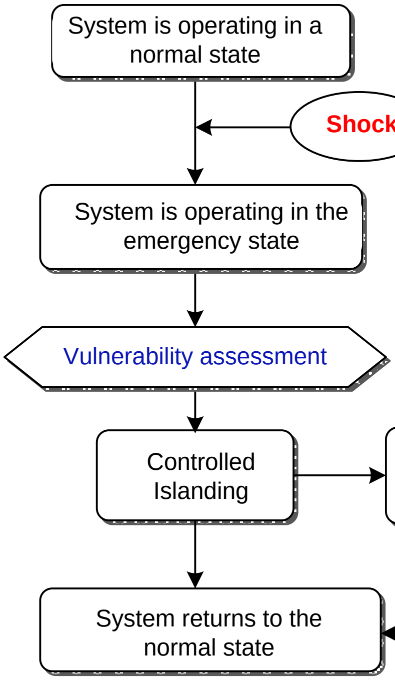

Fig. 3. Emergency control procedure

III. SIMULATION RESULTS

A. *Simulation with a 200-bus System*

In order to evaluate the performance of the proposed power network partitioning algorithm, a cascading scenario is created on a 200-bus test system, which is shown in Fig. 4. This test system is a variation of the simplified model of the western interconnection in North America. The system is operating under a peak load condition with a total generation of 64,410.4 MW, 16,597.6 MVar, and a total load of 63,510.41MW and 15,893.25 MVar. The simulation is based on PSS/E power flow solutions and PSS/E time-domain simulation results. The sequence of cascading events is as follows,

1) At t=0 second, three transmission lines are out-of-service.
2) At t=60 second, line 72-197 is de-energized due to the line fault.
3) At t=120 second, line 78-196 is de-energized due to the line fault. Generator G70 at bus 70 become overloaded.
4) At t=240 second, generator G70 is tripped by over-excitation protection.

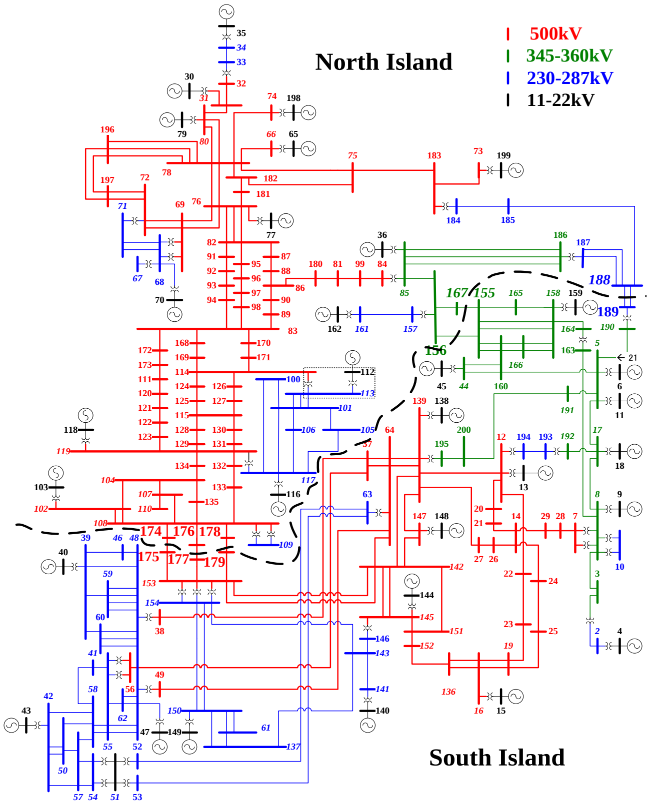

Fig. 4. 200-bus system

In this cascading scenario, successive tripping of the lines leads to power flow rerouting and overloads. After the tripping of generator G70, power swings become poorly damped. At about 260 second, the power system collapses. Bus voltages at 20 load buses during this cascading process are given in Fig. 5.

In order to prevent the impending blackout, the system is separated into two areas, i.e., North Island and South Island, using the proposed area partitioning algorithm. System islanding is initiated at 1s after the tripping of generator G70.

The edge cut set and generation-load condition is shown in Table I. The two islands are shown in Fig.4, the dotted line is the boundary of the two islands.

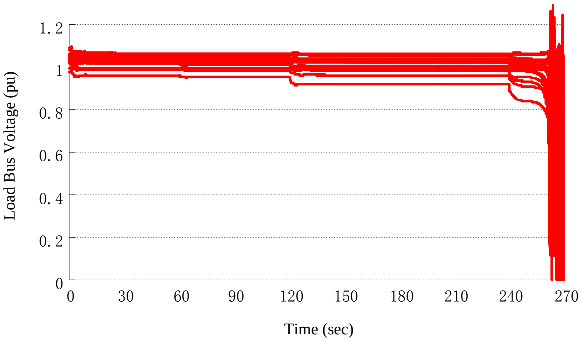

Fig. 5. Load bus voltages without islanding strategy

TABLE I
CUT SET AND GENERATION-LOAD CONDITION

Cut Set	Load-Generation (MW)
Bus 174-175, 176-177, 178-179, 155-156, 155-167, 188-189(1,2)	North: Gen=37,862, Load=37,104 South: Gen=24,517, Load=23,794

There are two transmission lines between bus 188 and bus 189.

As shown in Table I, the optimal islanding strategy results in generation and load balance in both islands. All loads in the system are served. The load shedding scheme is not necessary. The islanding strategy successfully prevents a voltage collapse of the system. Fig.6 and Fig.7 show bus voltages with and without islanding at two representative buses, bus 71 at North Island and bus 143 at South Island. The bus voltage at bus 71 is stabilized at 0.96 pu after islanding, and the bus voltage at bus 143 is stabilized at 1.01 pu after islanding. This example demonstrates that the proposed power network islanding strategy enhances the grid's shock absorption capability.

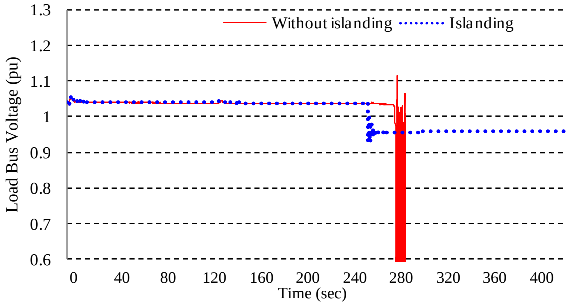

Fig. 6. Load bus voltage at bus71 at North Island

B. *Simulation with a 22,000-bus System*

In order to evaluate the computational efficiency of the developed area partitioning algorithm, it is also tested with a 22,000 bus system. After converting this power network into a weighted graph, 22,000 vertices and 32,749 edges are obtained. To partition this graph into 2, 3, 4 islands, the computation time based on 2 GHz Pentium CPU and 1GB RAM is 0.07s, 0.081s and 0.09s, respectively. The number of edge cuts is 299, 312 and 500 for islands 2, 3 and 4. The computational speed of the proposed algorithm is expected to meet the real time requirement. Further study is being conducted to perform a comprehensive evaluation of the algorithm for large interconnected power systems.

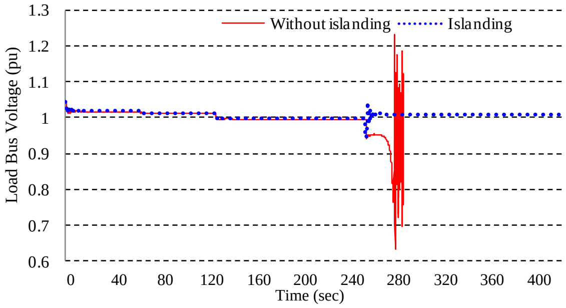

Fig. 7. Load bus voltage at bus143 at South Island

IV. CONCLUSION

Controlled separation of the power network is an emergency measure that involves partitioning of the power network into self-sufficient islands. The proposed area partitioning algorithm can be combined with a load shedding scheme to achieve a "smart grid" technology that enhances the robustness of the system and minimizes the impact of cascading events. There are important issues that need to be addressed in the future:

- More detailed simulations including dynamic simulations should be conducted on very large systems, such as the 22,000 bus system to validate the proposed algorithm.
- Since the boundaries identified by the proposed area partitioning algorithm are not always identical with company boundaries, the partition needs to take into account practical considerations.
- More work is needed to determine the wide-area protection and control system needed for implementation of the proposed method.

V. ACKNOWLEDGMENT

This research is sponsored by Power Systems Engineering Research Center (PSERC).

VI. REFERENCES

[1] H. Li, G. Rosenwald, J. Jung, and C.C. Liu "Strategic Power Infrastructure Defense," *Proceedings of the* IEEE, vol. 93, no. 5, pp. 918–933, May. 2005.

[2] H. You, V. Vittal, and X. Wang, “Slow Coherency-Based Islanding,” *IEEE Trans. Power Syst*., vol. 19, no. 1, pp. 483–491, Feb. 2004.

[3] X.Wang and V.Vittal, “System Islanding Using Minimal Cutsets with Minimum Net Flow,” *Proceedings of the* 2004 IEEE PES *Power System Conference and Exposition,* New York, October, 2004.

[4] Bo Yang, et al. “A Novel Slow Coherency Based Graph Theoretic Islanding Strategy”. 2007 IEEE PES General Meeting, 24-28 June, Tempa, Florida, USA. Paper No. 001373.”

[5] N. Senroy and G. T. Heydt, “A Conceptual Framework for the Controlled Islanding of Interconnected Power Systems,” *IEEE Trans. Power Syst.*, vol. 21, no. 2, pp. 1005-1006, May 2006.

[6] K. Sun, D. Zheng, and Q. Lu, “Splitting Strategies for Islanding Operation of Large-scale Power Systems Using OBDD-Based Methods”, *IEEE Trans. Power Syst.*, vol. 18, no. 2, pp. 912-923, May 2003.

[7] T. Bi, Y. Ni, C. M. Shen, and F. F. Wu, “Efficient Multiway Graph Partitioning Method for Fault Section Estimation in Large-scale Power Networks”, *IEE Proc-Gener. Trans. Distrib*, vol. 149, no. 3, pp. 289-294, May. 2002.

[8] J. S. Thorp and H. Wang, Computer Simulation of Cascading Disturbances in Electric Power Systems, Impact of Protection Systems on Transmission System Reliability Final Report, PSERC Publication 01-01. May 2001.

[9] Q. Zhao, K. Sun, D. Zheng, J. Ma, and Q. Lu, “A Study of System Splitting Strategies for Islanding Operation of Power System: A Two-phase Method Based on OBDDs”, *IEEE Trans. Power Syst.*, vol. 18, no. 4, pp. 1556-1565, Nov 2003.

[10] H. You, V. Vittal, and Z. Yang, “Self-Healing in Power Systems: An Approach Using Islanding and Rate of Frequency Decline-Based Load Shedding,” *IEEE Trans. Power Syst*., vol. 18, no. 1, pp. 174–181, Feb. 2003.

[11] B. Hendrickson and P. Leland, “A Multilevel Algorithm for Partitioning Graphs”, Tech. report SAND93-1301, Sandia National Laboratories, Albuquerque, NM, 1993.

[12] G. Karypis and V. Kumar, “A Fast and High Quality Multilevel Scheme for Partitioning Irregular Graphs”, *SIAM Journal on Scientific Computing*, vol.20, no. 1, pp. 359-392, 1998.

VII. BIOGRAPHIES

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