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Current Differential Relay with a Power-Current Spectrum Blocking for Transformer Protection

Hatem A. Darwish, Matti Lehtonen

***Abstract*-- In this paper, a combined power-current spectrum blocking for current differential protection of power transformer is proposed. The proposed algorithm can exclusively classify the internal faults associated with transformer inrush currents. This combination is assessed based on the individual analysis of differential power and power spectrum releasing functions and second harmonic current blocking considering modern design of power transformer. The investigation involves both theoretical and experimental studies in order to validate the new algorithm. Also, the scheme stability and sensitivity boundaries are obtained covering broad band of operational and fault conditions.**

***Index Terms*— Transformer protection, Inrush current, Power differential concept, EMTP simulation, DSP hardware.**

I. Introduction

POWER transformer is a class of vital component in the power system. If a transformer experiences a fault, it is necessary to isolate it as soon as possible so that the damage is minimized and period of unplanned outage is reduced. Accordingly, high demands are imposed on the transformer protections. The operating conditions of power transformer, however, do not make the relaying task easy. Thus, protection of power transformers still requires more emphasis. Many publications concerned with power transformer protection have been reported [1]-[13]. Most of the papers are concerned with the transformer differential relay supervised by the percentage of the second harmonic to either block or restrain the relay operation during inrush periods [1]-[3].

However, second harmonic would undesirably restrain the relay operation during incident internal faults associated with inrush periods, turn-to-turn, and turn to earth faults [4]. This is considered as a disadvantage of this restraining in spite of its long history in transformer protection. Also, modern transformers have lower percentages of the second harmonic during inrush, which increases possibility of false tripping. Recent relays based on different principles such as flux linkage, transformer model, Kalman filtering … etc are suffering from mathematical complexity [5]-[9]. Also, the boundaries between the normal and fault zones are not quite distinguished, which make the relay settings apparently difficult. Similar conclusions can be also obtained for relays based on the artificial intelligence including the ANN [10]-[13].

Voltage and waveform restraints seem to be solid competitive to the second harmonic restraining. However, it would also have a delayed operation during internal high impedance faults (HIF) or faults associated with inrush periods. On the other hand, a standalone instantaneous power algorithm for transformer protection has been reported [9]. However, issues of this algorithm have not been addressed yet because of the doubts on a further possible realization. With the revealed effectiveness of the power differential concept for line protection [14]-[15], it seems worthy to emphasize this concept for power transformer. For all the abovementioned schemes [1]-[13], detection of internal faults associated with transformer switching still represent a problem.

In this paper, a combined power-current spectrum blocking for the current differential relay is introduced. Suitability of the instantaneous power and differential current spectrums are assessed considering modern power transformer designs. Various faults are applied for transformer fed directly from the supply or via a transmission line. The proposed combined blocking scheme efficiently refines the classification of internal faults associated with the transformer switching. Stability and sensitivity boundaries of the new blocking scheme are addressed. Theoretical/experimental verification of the proposed scheme performance is achieved.

II. Concepts for Power Spectrum Applications

Three different concepts in applying the power differential rules will be addressed in this paper. These are:

- A straightforward application of the standalone power differential rule previously described in [9].
- Utilization of the differential power to release the percentage current differential relay during inrush conditions.
- Application of the instantaneous power spectrum as an alternative releasing module to the current differential relay.

A typical three-phase power transformer with 120 MVA, 220/70 kV, earthed star/earthed star connection is used in this study. This power transformer is deliberately selected because it is characterized by a small magnetizing current (0.0011 pu) and low second harmonic content in the inrush current. These characteristics have been realized in the EMTP model using the non-linear hysteresis element type-96 [16]. Considerable efforts involving regression analysis have been directed to obtain the B-H characteristic of the hysteresis element (shown in the Appendix) that fulfills this design. Then, the protection schemes are analyzed considering systems-*a* & *b* shown in Fig. 1. With reference to system-*a*, the transformer is fed directly from the source with a static load connected to the 70 kV side. However in system-*b*, a transmission line is included between the transformer and the supply. The parameters of the transmission line are also given in the Appendix.

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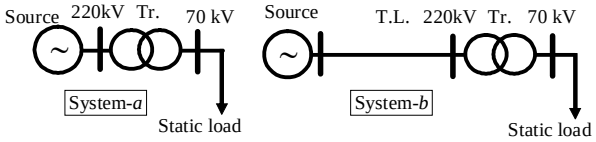
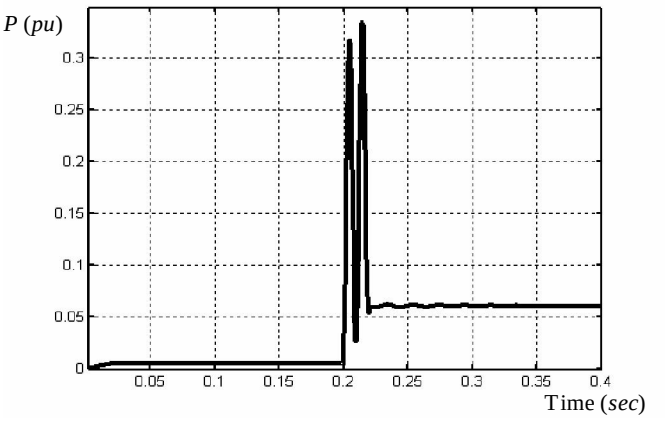
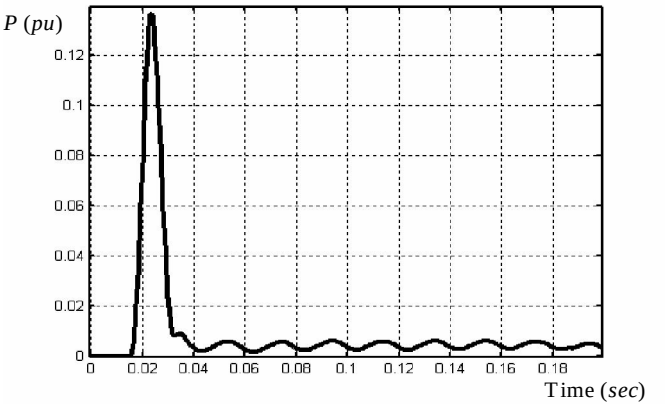


Fig. 1. Simulated systems.



a. internal L-G fault in the secondary side.



b. During inrush current.

Fig. 2. Power detector response considering system-*a*.

The transmission line is included in order to account for the interaction of line transients with the protection scheme [9]. Thus, the transformer protection would be subjected to a sort of critical tests.

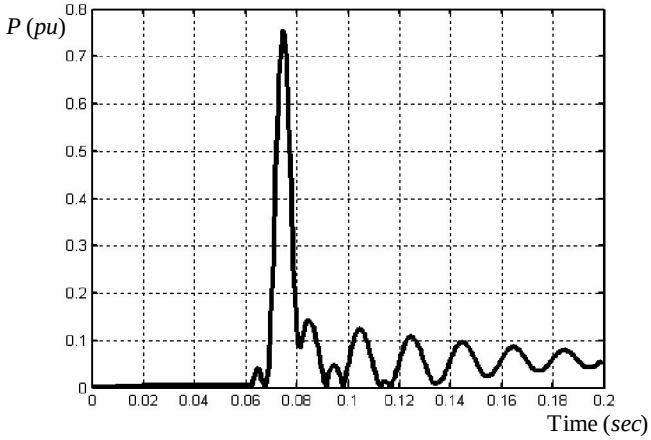
A. Conventional Power Differential Algorithm:

The conventional power differential algorithm deals with the power flow diagram of the power transformer in order to detect transformer internal faults as in the form [9]:

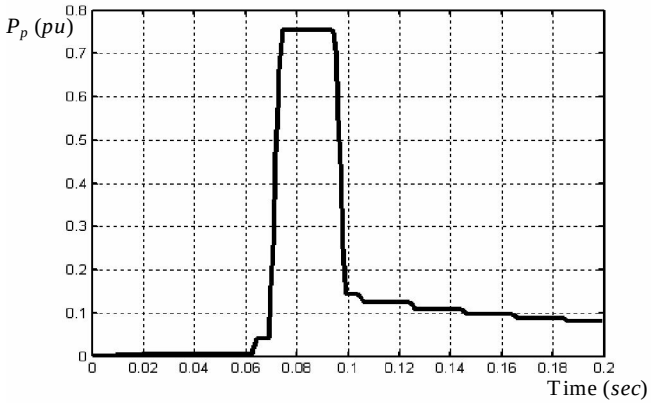
$$p(t) = \sum_{a,b,c} v_p i_p + v_s i_s - i_p^2 r_p - i_s^2 r_s \qquad (1)$$

$$P = \left| \sum_{a,b,c} \int v_p i_p + \int v_s i_s - \int i_p^2 r_p - \int i_s^2 r_s \right| \qquad (2)$$

where $p(t)$ and P are the sum of the differential instantaneous and absolute average power values for the three phases, respectively. Also, (v_p, i_p, and r_p) and (v_s, i_s, and r_s) are the instantaneous voltage, current, and winding resistance for both primary and secondary winding, respectively. Note that, the sign of the integration $v_s i_s$ is related to the dot rule of the magnetic circuit. During normal operation and external fault, the integration result P is very small. However for internal fault, P has a considerable high value. So, internal faults can be detected. Inrush current produces temporary high values of P and afterwards it drops to the normal operation low level. So, a suitable delay time (1 to 2 cycles) should be added.



a. Without applying the peak-hold method.



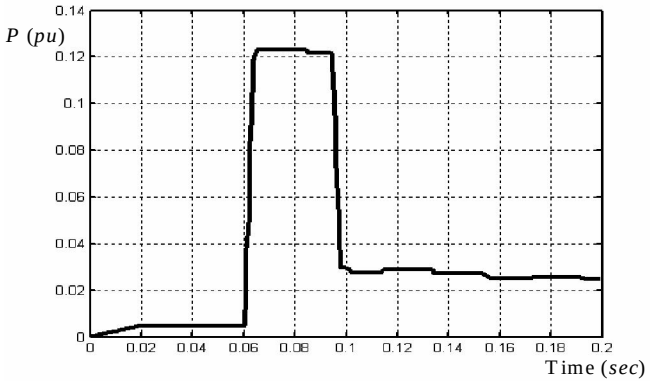
b. After applying the peak-hold method.

Fig. 3. *P* detector response for internal L-G fault at 70-kV side for maximum dc decaying.

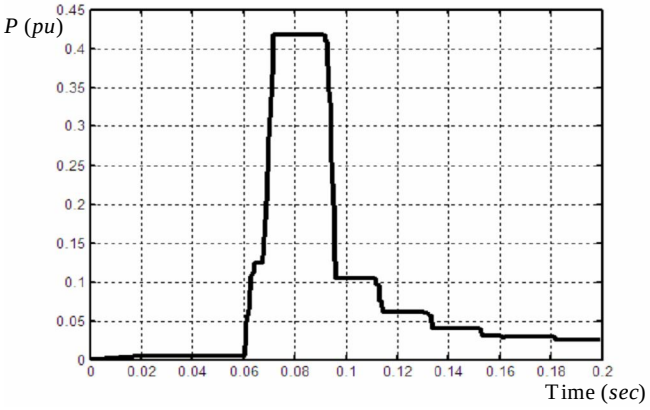
P responses for internal L-G fault and inrush current are computed as shown in Fig. 2 considering system-*a*. From Fig. 2, *P* has large values during fault than that of inrush current (approximately 10 times). This is obviously true if the produced peak value in the first 20 ms period of the inrush current is neglected. Thus, possibility of using *P* for internal fault classification is apparently verified. On the other hand, Fig. 3 illustrates the performance when the fault current includes a considerable dc decaying component. There exists a large oscillation in the average power as shown by Fig. 3.a. These oscillations are attributed to the contribution of the low frequency component of the dc decaying current spectrum. Thus, performance improvement of the *P* detector can be obtained by holding the peak value over the cycle time as shown in Fig. 3.b [9].

The *P*-detector and the related improvement have two critical issues when it is applied to System-b as shown in Fig. 4. For internal L-G, *P* has a low level approaching the inrush current equivalent power as shown in Fig. 4.a. This may be attributed to the reduction in the transformer terminal voltage due to the voltage drop over the transmission line in the infeed

side. Note that, longer transmission line would yield successive reduction in the values of *P*, which complicate the selection of the setting threshold. Also, *P* may increase for external fault such that it may produce higher values than that of internal faults especially when phase faults are applied on system-*b* as shown by Fig. 4.b. This feature absolutely prevents the standalone implementation of the *P* detector as it should be arranged with another scheme to classify the internal faults from the external one. Thus, the *P* detector operation would be restricted to the classification of the inrush currents from internal faults as will be described below. Note that, this problem is not well-addressed in [9].



a. internal L-G fault.



b. external L-L-G fault.

Fig. 4. *P*-detector response considering system-*b*.

B. Proposed P for blocking Percentage Differential Relay:

Fig. 5 shows the performance of the conventional second harmonic restraining integrated with the current percentage differential relay (87). In which, excellent selectivity of the internal faults is obtained even with high fault resistance up to 200 Ω. However in case of inrush current, the percentage differential relay failed to discriminate these conditions for a broad band of the switching angles as shown in Fig. 5. This is attributed to the low second harmonic contents in the inrush current of this transformer. Thus, the differential power *P* appears as an alternative permissive function in order to discriminate between internal fault and inrush currents.

If *P* is used as a blocking scheme for the percentage differential relay, the unsecured operation of the standalone *P* detector response to the external fault (shown by Fig. 4.b) will be also eliminated. In addition, this arrangement has a good sensitivity for high resistance faults and a good discrimination for faults associated with inrush periods as shown in Fig. 6. In Fig. 6.a, the proposed arrangement can efficiently discriminate internal faults with fault resistance up to 200Ω with an acceptable margin considering maximum possible power produced during inrush periods. However, Fig. 6.b shows the *P* behavior for solid L-G fault associated with inrush period. The high value of *P* indicates fault occurrence and possibility of detection. However, the problem of small differences between *P* values for the inrush and solid internal faults considering system-*b* still existing as previously shown by Fig. 4.a. This problem would be tolerated if other power spectrum components can produce more selective values.

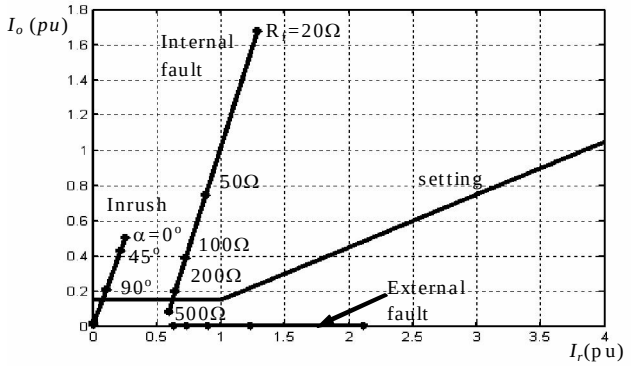
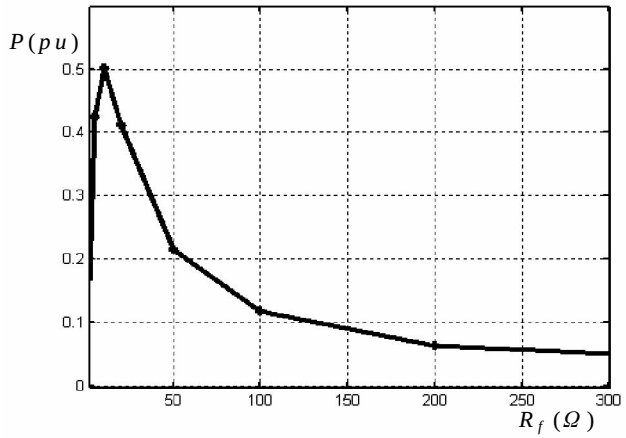
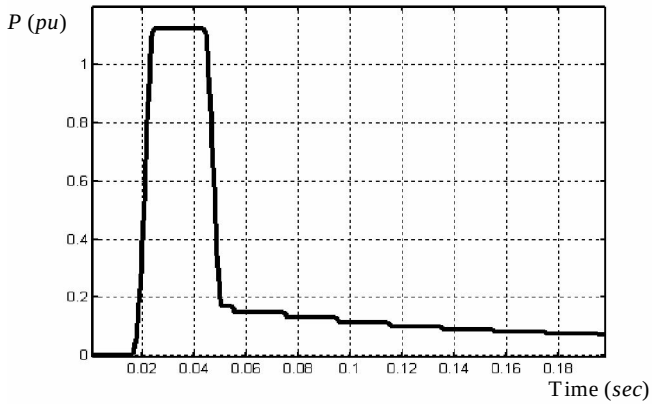


Fig. 5. Sensitivity boundaries for the 70-kV side faults and inrush conditions.



a. Average power magnitude versus R_f for system-*b*.

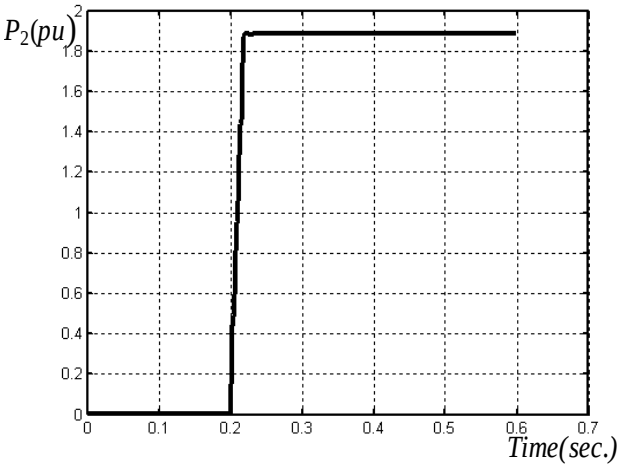


P detector for solid L-G fault accompanied with inrush period.

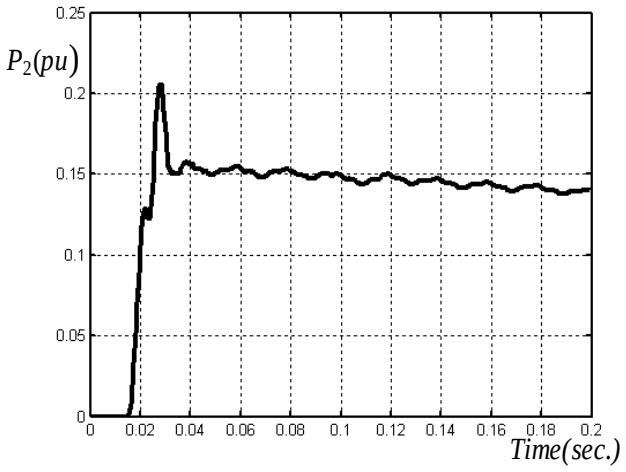
Fig. 6. P detector sensitivity.

C. Proposed p(t) Spectrum for Blocking relay 87:

Spectrum analysis of $p(t)$ has been processed to examine the behavior of each individual power component of the instantaneous power. That is in order to measure its suitability as a blocking for relay 87. Then, an appropriate component would be proposed to replace the average power P. The study covers the $p(t)$ spectrum up to the fifth harmonics. It is found that the second harmonic of the instantaneous power (P_2) in particular has shown a competitive performance to P. Thus, P_2 is extracted and used as a permissive signal. P_2 is obtained via a parallel optimized DFT filter fed by $p(t)$ samples [18]. Response of P_2 for internal L-G fault and energization cases are shown in Fig. 7. As can be seen from this Fig., P_2 level during fault is more than 15 times its level during inrush. This represents a superior performance over P, as the ratio was only 10 times considering the P detector for the same conditions.



a. Response for an internal single L-G fault at the 70 kV side.



b. Response of highest P_2 value for an inrush condition of system-*b*.

Fig. 7. Performance of P_2.

In addition, P_2 shows its highest selectivity for solid L-G fault versus minimum sensitivity of P for the same conditions. Also, the magnitude of P_2 itself is much higher than its corresponding values of P for fault and inrush conditions. Note that, P_2 is in the level of 0.16 pu compared with 0.006 pu for P during inrush conditions. Thus, if P_2 is used as a releasing to relay 87, discrimination between internal fault and inrush currents will be processed with its highest selectivity ever. Unfortunately, the value of the P_2 sensibly drops to small value with the increasing of R_f as shown in Fig. 8 for a single L-G fault. Only R_f values up to 100 Ω can be efficiently discriminated. In brief, P_2 has a distinguished performance during internal fault associated with inrush conditions with a slightly limited performance for high resistance faults. Testing of the second harmonic current blocking is worthy examined considering the same power transformer model.

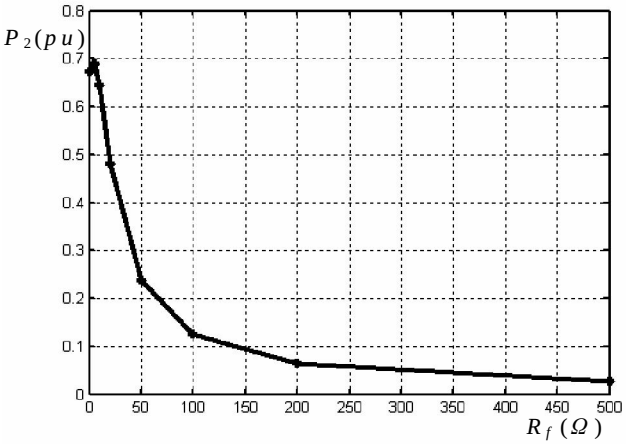


Fig. 8. P_2 magnitude versus the fault resistance for a L-G fault for system-*b*.

III. Second Harmonic Current Blocking

Percentage differential relay (87) with second harmonic restraining is widely used for transformer protection. During inrush periods, the second harmonic content of the difference current usually has values around 70% of the fundamental component and does not go below 16%. On the contrary, a small percentage of the second harmonic is usually recorded during internal faults. Thus, it is commonly used for restraining/blocking relay 87 operation during inrush conditions. Unfortunately, the second harmonic may be generated due to winding faults, CT saturation, or the presence of the capacitance of long HV transmission line/cable [4], [9]. In certain circumstances, the magnitude of the second harmonic during an internal fault may be close to or greater than the presented one in the inrush current.

These issues will be addressed considering two alternatives of second harmonic blocking concepts namely average and common second harmonic expressions.

A. Average Second Harmonic Blocking

In which, sum of the absolute values of the second harmonic is compared with sum of the absolute fundamental values extracted from the difference currents of the three phases considering a specific threshold; usually 15% to 35% [9]. The average second harmonic blocking method inherently increases the probability of false tripping as the second harmonic is not normally distributed over the three phases due to the relative difference in the switching angles. It is found that the average second harmonic content would be 11% during inrush period of the modeled transformer. Almost the same level of second harmonic (8%) has been observed during internal fault. Thus, a real difficulty in discrimination between inrush and internal fault exists.

TABLE I

DIFFERENT RELAY BEHAVIOR CONSIDERING MODERN DESIGNS OF POWER TRANSFORMER.

Relay Blocking Function	*Internal Solid Fault*	*External Solid Fault*	*Internal HIF on 70-kV side*	*External HIF*	*Inrush*	*Internal Fault with inrush*
✓ ***Relay 87 with no restraining***	Sensitive	Stable	Up to 200Ω	Stable	Fail	Sensitive
✓ ***Standalone P concept***	Limited sensitivity	Fail	Up to 200Ω	Fail	Stable	Sensitive
✓ ***Relay 87 with P releasing***	Limited sensitivity	Stable	Up to 200Ω	Stable	Stable	Sensitive
✓ ***Relay 87 with P_2 releasing***	Sensitive	Stable	Up to 100Ω	Stable	Stable	Sensitive
✓ ***Relay 87 with average 2nd har. Blocking***	Sensitive	Stable	Up to 200Ω	Stable	Limited Stable	Delay
✓ ***Relay 87 with common 2nd har. Blocking***	Sensitive	Stable	Up to 200Ω	Stable	Stable	High delay

B. Common Second Harmonic Blocking:

Alternatively, taking the block decision considering the percentage of the second harmonic current on a single phase basis is the common harmonic blocking scheme. Whenever the percentage of the second harmonic of any phase difference current exceeds the threshold, the tripping unit will be blocked for the three phases. It is evident from the previous analysis that relying on the common second harmonic would rectify the security issue of the average second harmonic blocking. Note that, the percentage of the second harmonic is permanently higher than the minimum threshold (15%) at least for one phase among the transformer three phases during inrush conditions.

The major drawback of this concept is attributed to the unacceptable delay of the trip signal for inrush current associated with internal fault conditions. The second harmonic of the sound phases will block the relay trip unit as they usually experience a high value of second harmonic. Therefore, a reduction in the selectivity is resulted versus the gained security.

IV. PROPOSED POWER-CURRENT SPECTRUM BLOCKING

The test results of this extended study are summarized in Table 1. Around two thousands of test cases are applied covering normal operation, inrush, and internal and external fault conditions. Also, wide range of switching and fault inception angles are studied considering the system arrangements; Fig. 1 (*a* and *b*). It is evident from Table 1 that no a single blocking signal can efficiently fulfill all requirements and constraints associated with power transformer protection. That is in spite of P_2 shows a good fulfillment to most requirements. However, it has a lower sensitivity for internal HIF compared to other blockings. Also, the sensitivity limit for all alternative blockings did not occupy the same zone of the relay operation plane. When the P_2 sensitivity limit for HIF is low, the second harmonic and *P* sensitivities are high. However for solid faults associated with inrush currents, sensitivity of different blockings acts in the other way around. Also, when *P* is not efficient in detecting internal solid L-G fault and classifies it as an inrush case, P_2 is at its highest fault discrimination capability. Thus, combining different blocking to produce the highest sensitivity for the differential relay without violating a considerable stability margin can be conveniently approached.

The proposed power-current spectrum blocking combines the blocking of the second harmonic current and the releasing of the average power and second harmonic of the instantaneous power in a novel arrangement along with the percentage current differential relay (87). The logic diagram of this arrangement is given by Fig. 9. In which, releasing flags of *P*, P_2, and the common second harmonic current blocking are ORed to constitute the overall Release/Block signal. This flag is ANDed with the trip signal of relay 87 in order to produce a secured and selective relay decision. Note that, the power flags should active low and the second harmonic current is active high to block the relay operation.

The basic advantage of this novel algorithm module is the complement actions of power and current flags. For example, the shortcoming of the common second harmonic current blocking during inrush associated with internal fault is tolerated by the power flags. In the contrary, the less selective performance of the power detectors with some internal solid L-G fault is tolerated by the second harmonic current flag. Also, *P* flag is included along with P_2 to utilize its high selective behavior during high impedance faults (HIF). Performance of the proposed blocking is worthy examined via an experimental setup.

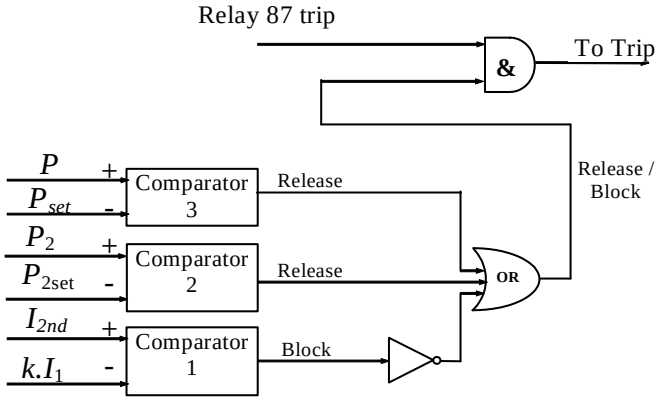


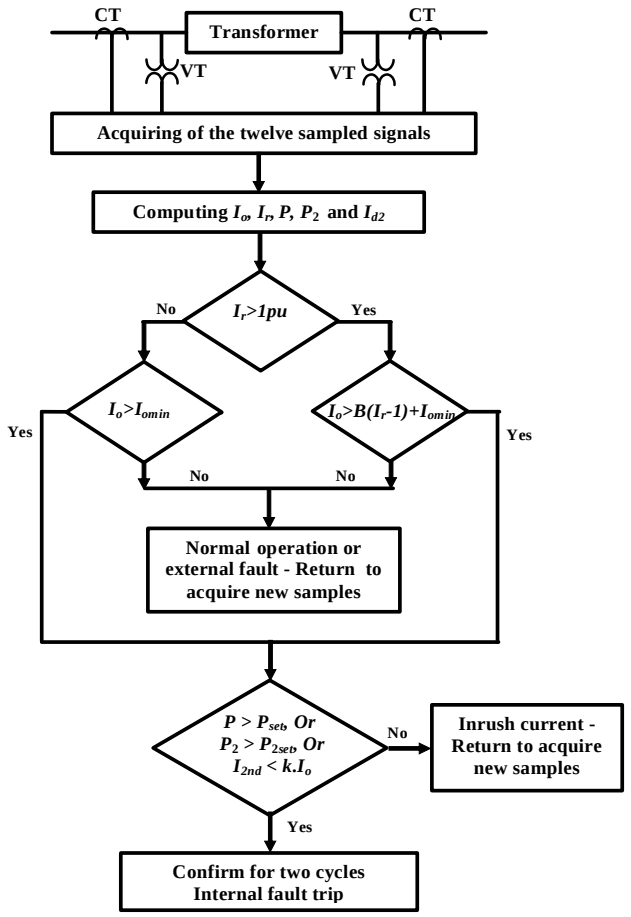
Fig. 9. The proposed power-current blocking logic diagram.

V. EXPERIMENTAL TESTS OF THE PROPOSED SCHEME

A. Laboratory Test Setup

Fig. 10 shows a laboratory set-up and DSP-based implementation flowchart of the proposed relay. In Fig. 10.a, the experimental set-up consists of laboratory 3-phase 2-winding transformer with primary winding rated at 250 V, 2.9 A, 287 turns with a tapping point at turn 187. However, the secondary winding has 5 taps at 12, 24, 48, 64, and 138 turns with 2.9 A current rating. The transformer is connected to a resistive load via a transmission line module with 5 sections; PI representation. The transformer currents and voltages are measured using 20 hall-effect transducers; 10 units for the currents with 25 A primary rating and 10 voltage units with 600 V primary rating. The output of both units are voltage signals to be calibrated via 20 potentiometers to keep the output signal within ±10 V peak value, which matches analog input channel rating of the DS2201 in order to avoid A/D converter saturation.

a. Experimental DSP-based setup of the laboratory transformer.



b. The flowchart.

Fig. 10. Practical implementation of the relay 87 with the proposed blocking.

The twelve output signals of the transducers are forwarded to the analog input channels of the multi input/output (I/O) board DS2201. This I/O board is interfaced with the digital signal processing (DSP) board DS1003 via the Peripheral High Speed 32-bit bus (PHS-bus). Details of these boards and interfacing procedure could be reviewed in [19], [20]. A PC is employed as a host machine of the relay program for editing, modification, compilation, and finally down loading to the DS1003. Also, further monitoring and tracing of the relay variables are accomplished using a Trace software package running on the PC [20]. Note that, the bi-directional data transfer between the standalone DS1003 and the PC is running via a dual port memory. A sampling rate of 32-sample/cycle is adopted, which implies a 312.5 μs sampling interval. Thus, the acquisition of the 12 channels, data processing, digital filters, power expression, flags extraction and logic should be processed in this tide time. This reflects the distinguished computation capabilities of this board for executing such complicated algorithms. Only 210 μs was required to execute this algorithm during real-time.

B. Proposed Relay Algorithm

The proposed relay algorithm can be explained with the help of Fig. 10.b considering the percentage differential relay shown in Fig. 5 along with the proposed blocking logic diagram of Fig. 9. The primary and secondary current and voltage signals are acquired, sampled, manipulated, and then different required values are computed to feed different algorithm modules. The through and difference currents are obtained and the fundamental and second harmonic components are calculated using the DFT filter. These values are used to evaluate the percentage differential relay rules and the common second harmonic flag. However, the current and voltage samples are used for calculating the power flags, P and P_2. Note that, P is obtained based on (2) and P_2 via spectrum analysis of $p(t)$ of (1) using the optimized parallel DFT filter [18]. This new DFT filter exclusively insures robust execution of the recursive DFT formulae and eliminates any numerical instability that may appear with float-point central processing units (CPU). Then, the following algorithms steps are accordingly processed.

1. If the fundamental component of the difference current I_o is lower than the through current I_r considering relay 87 characteristics of Fig. 5, the operation is either normal or external fault. No need for carrying out any check on the blocking flags.
2. Otherwise, an internal fault or inrush condition took place. Thus, the three flags must be scanned.
3. In inrush periods, the three ORed flags will be identical indicating clearly that the case is an inrush current.
4. However during internal faults, the three ORed flags will active high to provide a trip permissive signal.
5. If the three flags differ from each other, which is expected in some circumstances, a trip signal will be also released as it quite clear the three blocking signals have different sensitivity zones in the operation plane.

C. Experimental Evaluation

Hundreds of experimental test cases including normal operation, switching, internal and external faults, and internal faults associated with switching have been carried out. In fact, the relay performance during the experimental phase of tests has shown a better performance over that obtained during the simulation phase. This is attributed to the ordinary design of the laboratory transformer (around 70% average second harmonic in the inrush currents) and the slightly higher winding resistance. This reflects higher P and P_2 values for all internal fault cases including winding to ground and inter-turn faults. In spite of the experimental scheme confirms the applicability of the proposed blocking, it was obvious that any of the three ORed signals especially P and P_2 was sufficient to individual-

ly provide the desired blocking as the transformer is of ordinary laminated iron core. Nevertheless, the experimental results could not explicitly confirms the high value added to the power transformer protection. Fortunately, the superiority of this new blocking has been confirmed via the simulation phase, which modern power transformer designs had been addressed. However, the experimental implementation provides evidence of the execution time of the algorithm modules.

VI. Conclusion

In this paper, a novel combined power-current spectrum blocking for power transformer current differential protection is proposed. The proposed algorithm can exclusively classify the internal faults associated with transformer inrush currents. This combination is assessed based on the individual analysis of the second harmonic current, differential power, and power spectral blockings. The investigation involves both theoretical and experimental studies. The simulation results have been carried out on 220 kV/70 kV, 120 MVA, 50 Hz, earthed star/earthed star connection of modern design power Transformers. However, the experimental phase is incorporated using a laboratory ordinary transformer with 2 kVA rating. It is found that, a novel ORing gate fed by the common second harmonic blocking, negated power differential output, and negated second harmonic power output have revealed a superior blocking performance of the traditional current differential relay. More than 2000 test cases have been applied where the proposed blocking has been examined. Also, the relay was sensitive for all internal fault associated with the switching operation as 40 ms intentional delay is included. A sensitivity limit of 200 on the 70 kV side has been measured. Also, it is stable for all external faults.

VII. Acknowledgment

An acknowledgement is to Dr. Nagy I. Elkalashy and Eng. Hesham Ali for the discussion and submission.

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IX. Appendix A

A simplified system consists of 120 MVA, 220/70 kV power transformer with star-star connection and the star point solidly earthed. The transformer EMTP model is provided with a non-linear reactor type-96 and connected to the low tension side to account for inrush and over-excitation current representations. A considerable effort has been given to obtain the core hysteresis characteristic shown by Fig. 11, which produces low second harmonic and complies with the transformer steady state no load current of 0.0011 pu. However, the transmission line is modeled using the distributed parameters to account for unsymmetrical fault representation with parameters:
R_o=0.04612 Ω/mile, L_o=2.6574 mH/mile & C_o=4.3 nF/mile.
R_1=0.01537 Ω/mile, L_1=0.88588 mH/mile & C_1=13 nF/mile.

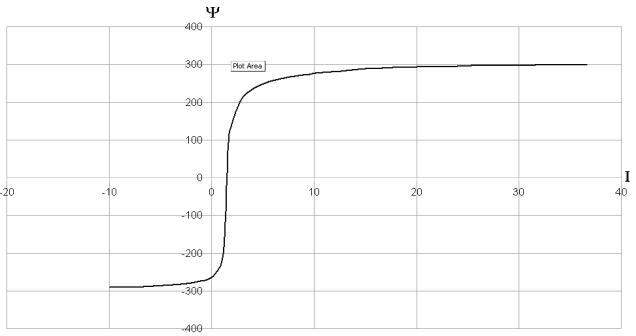

Fig. 11. Adapted hysteresis characteristics of the magnetizing branch.