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Active Islanding of a Current-Controlled Converter-Interfaced DG

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***Abstract*—Islanding of a voltage source converter (VSC) equipped DG unit is considered in this paper. Some internal controller signals are implemented in the islanding detection method in order to provide a robust operation. Particularly, the estimated frequency of the grid voltage along with a point of common coupling (PCC) voltage regulator and a dynamic reference-current limiter are proposed for islanding detection algorithm. Using a PCC-voltage regulator adds the active, or dynamic, property for the detection algorithm and increases its reliability. Moreover, implementing a dynamic current limiter, a robust operation is achieved. Through the proper design of the current limiter, the DG unit can have the ability to ride-through voltage dips with magnitudes above a certain limit, which can be set according to the grid codes, and detect islanding if the voltage decreases beyond that limit. The algorithm has also been verified for the case of island motor loads, which is considered as the worst case since dynamic loads affect the grid states in the case of islanding.**

***Index Terms*—Distributed generation, Dynamic current limitation, Intentional islanding, LCL-filter, PLL, Voltage source converters, Vector control.**

I. Introduction

Although the integration of distributed generation (DG) has many driving forces, it still has many challenges [1]. Islanding, due to utility outage, is one of the problems that can cause improper operation of a DG unit, and its connected loads, if it is not correctly detected.

There are two types of islanding detection techniques; namely passive and active [2]. In the passive techniques, the sensed grid states (voltage, frequency …etc.) are compared with their nominal values and the deviations are used to identify the islanding condition. Although they are simple to implement, the passive techniques suffer from a certain non detectible zone (NDZ), which represents the amount of the active and reactive power mismatch between the DG and its local loads at which the passive detection algorithm fails [2], [3]. Incorporating the active detection techniques, the NDZ becomes negligible. An active detection technique could typically be incorporated in the main controller of the DG, using active disturbance injection into the grid [4].

If the grid is disturbed, the passive detection starts to react to identify the islanding condition.

The problem of islanding can be more crucial with the application of the DG in a weak grid, where the grid states are not robust [5]. That implies that the active detection techniques that tend to disturb the grid are not adequate. Instead, active techniques that tend to improve the power quality at the grid might be more adequate.

The steady state performance of different passive detection algorithms regarding the reduction of the non-detectible zone (NDZ) has been studied in literature [2][3]. The under/over frequency has been found to have an NDZ that is independent on the active power mismatch and dependent on the quality factor of the load. To overcome this dependency, an under/over frequency passive detection algorithm has, in this paper, been incorporated within an active detection technique. The detection technique consists of three parts: a passive detection algorithm, a PCC voltage regulator, and a dynamic reference-current limiter. The dynamic performance and robustness of the proposed active islanding detection are studied regarding the voltage dips at the grid and the load dynamics.

II. System Description

A. Investigated Network

The system in Fig. 1 is considered for the demonstration, where Z_s is the Thévenin impedance of the grid as seen by the point of common coupling (PCC), and E is the Thévenin equivalent voltage. The voltage E is assumed to be equal to 1 p.u. during normal operation. The voltage at the PCC (U_{PCC}) is affected by the feeder voltage drop and the load dynamics. The feeder has an X/R ratio of 10, and its inductance is 6.15 mH per phase. The island-loads consume power that is assumed to be lower than the DG-injected power, implying the directions of the active and reactive power mismatches (ΔP and ΔQ) as designated in the same figure. The island loads will be set (models and parameters) later in order to investigate the ability of the islanding detection method for various cases.

The grid loads are assumed to be static loads that have rated power of 0.2 p.u. based on the DG nominal rating. The DG unit is a voltage source converter (VSC) based system that is connected through an LC-filter and a transformer to the PCC, as shown in Fig. 2. The nominal data of the DG unit are reported in Table I.

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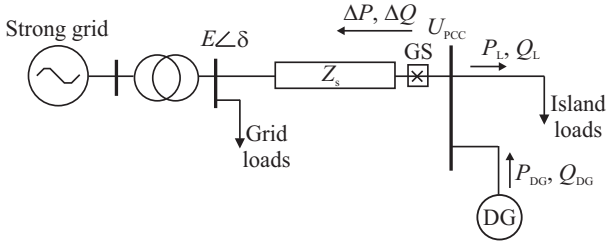

Fig. 1. System considered for islanding study.

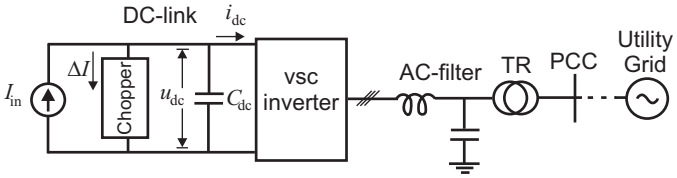

Fig. 2 Converter-interfaced distributed generation.

TABLE I
DG SYSTEM DATA

Symbol	Quantity	Value
E_{PCC}	Nominal RMS line AC voltage at PCC	0.4 kV
I_{DG}	Nominal RMS current	0.1 kA
f	Nominal grid frequency	50 Hz
U_{dc}	Nominal DC-link voltage	0.65 kV
I_{dc}	Nominal DC-link current	0.107 kA
L_1	VSC-side filter inductance	0.52 mH
R_1	VSC-side filter-inductor resistance	1.6 mΩ
L_2	Transformer equivalent inductance	0.2 mH
R_2	Transformer equivalent resistance	0.6 mΩ
C_f	Filter capacitance	138 μF
L_{dc}	DC-chopper inductance	0.1 mH

The main part of the DG system, which is considered here, is a PWM voltage source converter (VSC), which represents the front end of an energy source. The latter is modeled as a constant current source I_{in}, since the variations in the input power are considered slow compared to the transient response of the VSC controller. The LC-filter is implemented on the AC-side of the VSC to prevent harmonic current injection into the grid.

B. DG Main Current-Controller

The DG controller is implemented in a rotating *dq*-frame that is synchronized with the grid-voltage angular-frequency using a phase locked loop (PLL). The PLL estimates the angular frequency of the grid voltage $\hat{\omega}$ using a PI-controller [6]. In the case of island operation, the output of the PLL is set to the reference angular frequency ω^*. The grid states (voltages and currents) are measured and transformed into vectors in the *dq*-frame, where the transformation algorithm sets the *q*-component of the grid voltage to zero, while the *d*-component represents the amplitude of the line voltage. A DC-link voltage regulator is also incorporated, by using the DC-link current chopper, in order to maintain a constant DC voltage value. The DC-regulator is implemented as a PI-controller that outputs a DC current reference i_{dc}^*, which reflects the amplitude of the active current injected at the PCC. The DC-chopper is incorporated on the DC-side of the VSC in order to store the extra power that is produced during island operation by the energy source. This provides a fast control of the power to be injected into the PCC. Further storage or control over the primary energy source will be also required as a backup to provide longer island operation. It is worth to note that the chopper control can also provide more ancillary services at the grid during normal operation (e.g. compensating the fast active power oscillations at the PCC) [8].

1) Vector Current Controller:

The different blocks of the converter current-controller are depicted in Fig. 3. The VCC is basically a PI-controller that compares the reference current vector $\underline{i}_{dq}^*$ with the actual injected current vector $\underline{i}_{dq}$. The error is then used to modify the reference voltage vector $\underline{u}_{dq}^*$, and a reference voltage limit is applied in order to avoid the saturation of the pulse width modulator (PWM). The delay block in the figure represents the inherited one sample time delay of the digital controller and is compensated for through the controller within the delay-predictor block. The reference voltage vector $\underline{u}_{dq}^*$ is then transformed into three-phase quantities and then used in the pulse width modulator (PWM) to generate the switching pattern that would change the injected current in a way to remove the error. The plant block in Fig. 3, represents the PWM, VSC, AC filter, and transformer. This controller can also be described in both negative and positive sequence frames for a proper operation in case of grid voltage imbalance. More details about the controller are given in [11].

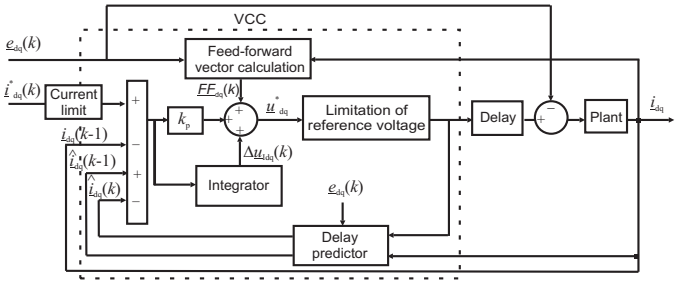

Fig. 3 Current controller for VSC-DG.

2) Vector Voltage Controller:

A reactive power controller will generally be activated in case that the voltage at the PCC deviates from its set value. The controller is implemented in the *dq*-frame. The instantaneous reactive power generated by the DG at the PCC is described as

$$q_{(PCC)} = e_{q(PCC)} i_d - e_{d(PCC)} i_q \quad (1)$$

Where e_d represents the voltage amplitude at the PCC, e_q reflects the error in the voltage angle that is assumed here to be zero, i_d is the active current component, and i_q is the reactive current component. Hence, the reactive current reference is generated to compensate the error in the voltage amplitude using a PI-controller, as follows

$$i_q^*(k) = k_{pr}\varepsilon_e(k) + \frac{k_{pr}T_s}{T_{ir}}\sum_{n=1}^{k}\varepsilon_e(n-1) \quad (2)$$

$$\varepsilon_e(k) = e_d(k) - e_d^*(k) \quad (3)$$

Where k is the sampling instant, k_{pr} is the proportional gain of the PCC-voltage regulator, T_{ir} is the integral time, and e_d^* is the set value of the amplitude at the PCC.

3) Dynamic Current Limit:

A dynamic current-limit that prioritizes the reactive current injection is implemented as explained in Fig. 4, where two main limitations are introduced. First, the limit over the reactive current is introduced in order to differentiate between the voltage dips and the grid outage conditions. The second limit is set over the maximum energy that can be stored in the chopper inductance. The latter is reflected in the figure by the maximum allowed active current reduction; ξ.

The reactive current limit is set for the lowest voltage dip that the DG should ride-through and not to detect an islanding condition, as

$$I_{q,limit} = I_{q,n} + I_{q,dip} \quad (4)$$

The current $I_{q,n}$ is the measured reactive current amplitude that is injected during the normal operation (assumed zero). The second term in (4), $I_{q,dip}$, is the reactive current that is calculated to ride through a certain value of the remaining voltage during voltage dips (V_{dip}), and is calculated as

$$I_{q,dip} = -k_{pr}(1 - V_{dip})U_{PCC} \quad (5)$$

Where V_{dip} is in per unit, U_{PCC} is the nominal voltage at the PCC, and k_{pr} is the reactive power controller proportional-gain.

The reactive current limit is used to set the DC-current chopper size as illustrated by Fig. 4. For instance, in case of a voltage dip magnitude that is less than the value used for the reactive current limit calculation, a current vector that lies at b will result but it will be limited to d where the maximum allowed reactive current is set. The proper chopper size, ξ in per unit, can easily be calculated from the figure and (4); assuming $I_{q,n}$ is zero and U_{pcc} equals 1 p.u. as

$$\xi = 1 - \sqrt{1 - k_{pr}(1 - V_{dip})} \quad (6)$$

The lower V_{dip} is set in (6), the higher ξ is and more robust operation is introduced.

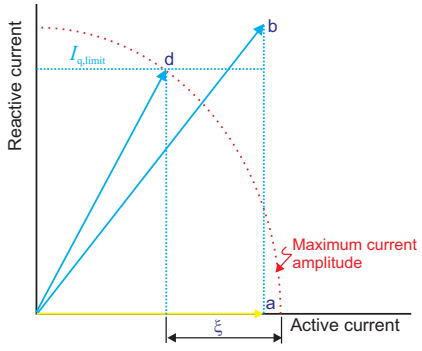

Fig. 4 Current limitation for both the reactive current and the total current.

III. Active Islanding Detection

The islanding detection that is proposed here is composed of three parts; a frequency based passive detection algorithm, an active PCC voltage regulator, and a dynamic current limiter. The passive detection algorithm is the main decision maker. It outputs a signal that changes the state of the controller from grid connected to island operation or vice versa. In some cases, for instance when the DG reactive power output matches the load reactive power consumption, the passive detection might fail to detect islanding, as shown later. Hence, a PCC voltage regulator is used to generate a reactive power mismatch in case of a change in the grid voltage. Moreover, to differentiate between voltage dips and a grid outage a current limit is set for the minimum voltage dip magnitude that the DG should ride-through without islanding. The three parts are explained in more details below.

A. Passive Detection Algorithm

The passive detection algorithm is shown in Fig. 5. Starting from the parallel (or grid-connected) operation, where the DG is aiming at controlling the active and reactive currents injected into the grid, the detection algorithm will be activated to detect the grid outage. The algorithm uses the deviation between the estimated frequency signal, which is produced by the PLL, and the nominal value. A time threshold t_s is also incorporated to avoid false tripping due to load dynamics. This time threshold is set equal to the settling time of the PLL, which could be calculated using the PLL gain as follows [7]

$$t_s = \frac{\ln 50}{k_{pll}} \quad (7)$$

where k_{pll} is the proportional gain of the PLL.

Once the islanding condition is detected, the DG starts an island operation mode where its aim is to hold the voltage and frequency at their nominal values as well as to adjust the injected active and reactive powers to support the island loads. The grid switch GS, shown in Fig. 1, is used to disconnect the island from the utility grid for safety operation. The DC chopper is also activated to consume the extra power that could be coming from the energy source in a way to adjust the input power to match the island loads need. Moreover, in this mode, the grid recovery detection is activated where the voltage on the grid side is sensed. Once the utility grid is recovered, the synchronization between the DG voltage and the grid voltage is carried out using an extra PLL on the grid side. The connection to the grid is then done by enabling the GS. At the same time the DC chopper is disabled, and the controller starts the parallel operation mode.

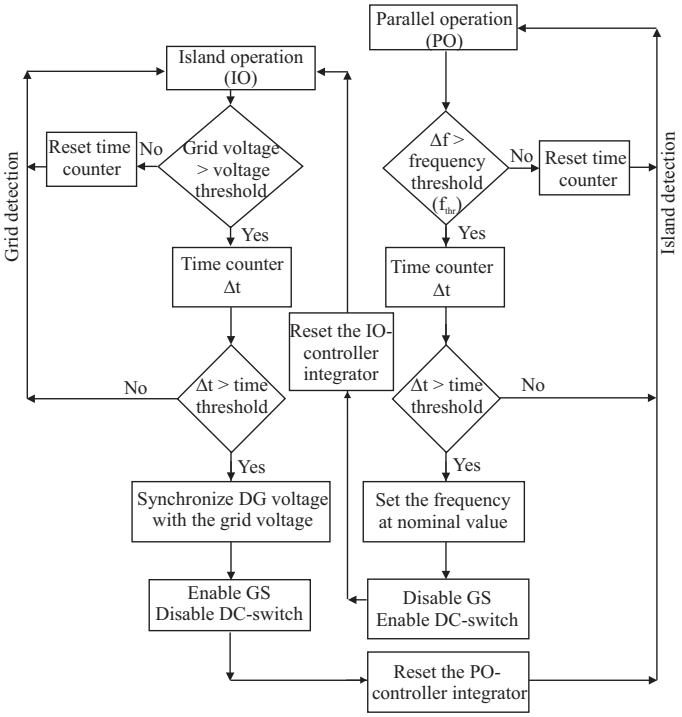

Fig. 5 Islanding and grid recovery detection algorithm.

B. PCC-Voltage Regulator

As it has been mentioned above, the PCC-voltage regulator is incorporated as a part of the islanding detection algorithm since it reduces the non detectable zone where the passive detection would fail. This is investigated by introducing island loads that are quadratic voltage dependent and result in an active power mismatch (ΔP) of 0.15 p.u. and zero reactive power mismatch ($\Delta Q = 0$). The PCC-voltage regulator is first deactivated. The estimated frequency, which is the output of the PLL, is shown in Fig. 6(a) by the dashed line. A grid outage has occurred at 0.8 s due to a fault in the grid. The estimated frequency has a constant increase after 0.8 s due to a small change in the reactive power of the load that is in turn resulting from the increase of the PCC voltage, as shown in Fig. 6(c). This increase in the estimated frequency could be relatively small and, depending on the frequency threshold in the passive detection algorithm, it might not successfully detect the islanding condition. By activating the PCC-voltage regulator, the estimated frequency will continue to increase, as shown in Fig. 6(a) by the solid line, after the grid outage at 0.8 s, due to the continuous increase in the DG injected reactive current that is shown in Fig. 6(b).

C. Case Study

A general case is set to study the operation of the proposed DG controller. The island loads are modeled as an aggregated quadratic voltage dependent load with a nominal active power mismatch (ΔP) of 0.55 p.u. and a reactive power mismatch (ΔQ) of 0.2 p.u.

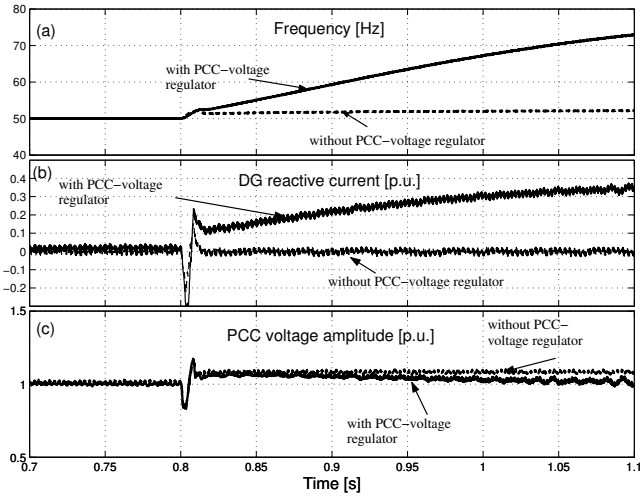

Fig. 6 Grid outage at 0.8 s, for zero reactive power mismatch ($\Delta Q = 0$) and active power mismatch (ΔP) of 0.15 p.u., with and without the PCC-voltage regulator. (a) The estimated frequency. (b) The DG injected reactive current. (c) The PCC voltage amplitude.

The PCC-voltage and estimated frequency are shown in Fig. 7 for the operation of the DG before, during, and after islanding. The grid is disconnected at 0.3 s, where the voltage *dq*-components start to increase in value. When the *d*-component of the PCC-voltage $u_{d(PCC)}$ reaches the voltage limit, that is set by the controller, at t_1, its constant-limited value is maintained (until t_2). The estimated frequency will start to increase at t_1, due to the constant value of the voltage *q*-component, until the island is detected at t_2 where the value of $t_2 - t_1$ is equal to the time threshold that is set by (7). At t_2 the detection signal is activated, resulting in transferring the controller from grid-connected mode to island-operation mode. The frequency is reset to its nominal value, and the DG injected power is adjusted to match the load requirements (the DC chopper is activated to dissipate the excess power).

When the grid voltage is recovered at t_3, a time threshold is also encountered before the synchronization of the grid voltage and the DG voltage starts at t_4. This is done by using an extra PLL that is implemented for the voltage before the grid switch GS from the utility grid side. At t_4, the phase angle of the DG voltage is set equal to the phase angle of the grid voltage. This could be seen from the change of the frequency signal in Fig. 7 from t_4 to t_5. After about one cycle of the PCC-voltage, the island is connected back to the utility grid at t_5. The DC-chopper is left in operation to buck the over-voltage that could occur at the starting of the grid-connected controller mode, until the PCC-voltage is stabilized. It is then deactivated in order to inject the nominal DG power into the grid.

At t_5, where the grid connected current controller starts, $u_{d(PCC)}$ drops to a value that represents its normal amplitude in case of deactivating the PCC-voltage regulator. This is mainly due to the PCC-voltage regulator transient time, which has been set slow enough to stabilize the overall DG controller. In spite of the decreased value of the voltage during this time, the duration is very small compared with the clearing times that are set by the grid codes (e.g. a clearing time of 2 s for a

decreased voltage down to 50% is set by the IEEE-std 1547-2003). After the transient time of the PCC-voltage regulator, the PCC-voltage amplitude will regain its nominal value. In addition, the DG injected power and currents will regain the values that are set for the nominal grid connected operation.

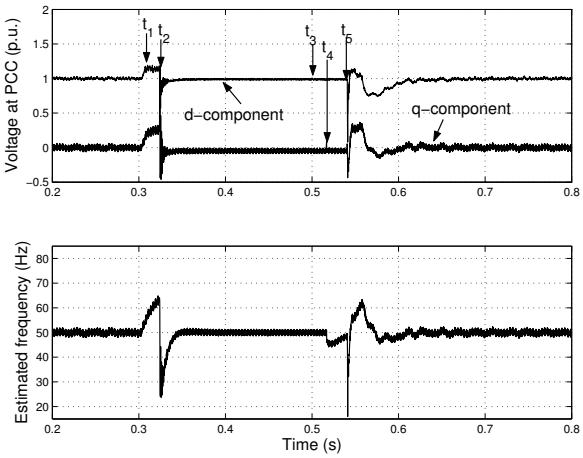

Fig. 7 Voltage in *dq*-frame (upper) and estimated frequency (lower) at the PCC for grid outage at 0.3 s and grid recovery at 0.5 s.

IV. Islanding Detection Reliability

The islanding detection method should differentiate between the grid outage condition and other grid dynamics by producing the correct detection signal. The focus here is set on testing the proposed detection method in case of voltage dips that might appear at the DG connection point due to a remote fault at the grid. Since the voltage at the connection point could also be affected by the local load, the load behavior should be included in the study. Active loads that could affect the state of the grid are assumed as the worst case. Hence the following discussion is carried out assuming that an induction motor (IM) load is connected at the PCC. The motor load data are reported in Table II.

TABLE II
Induction Motor Data

Symbol	Quantity	Value
U_m	Nominal RMS line AC voltage	0.4 kV
P_m	Nominal power	45 hp
f	Nominal frequency	50 Hz
R_s	Stator resistance	0.0389 Ω
$L_{s\lambda}$	Stator leakage inductance	952 μH
L_m	Mutual inductance	23.6 mH
R_r	Rotor resistance	0.0347 Ω
$L_{r\lambda}$	Rotor leakage inductance	1595 μH
J_m	Motor inertia	0.4 kg.m^2

Generally, dynamic loads that have a power consumption that is dependent on the state of the voltage at the grid cannot be treated using the steady state analysis that has been presented for static loads (e.g. in [3] and [4]). The reason for that is the variable power mismatch that is dependent on the load characteristics. Hence, the dynamic (or active) approach that is proposed here for the islanding detection is to be investigated with two different load inertias. In particular, the effect of changing the reactive current limit is tested in case of voltage dips at the PCC.

1) $J_L = 0.6$ and $\Delta P = 0.4$ p.u. (high inertia load):

First the load inertia J_L is set to 0.6. The active power mismatch (ΔP) is equal to 0.4 p.u. in steady state. The current limit (11), should be set so that the islanding detection method does not produce a detection signal during the voltage dips that the DG should ride-through. If the PCC-voltage decreases below a certain value, islanding should be detected. A remaining voltage amplitude (V_{dip}) of 0.3 p.u. will be considered here as a threshold value between the ride-through operation and the islanding operation of the DG. Hence, $I_{q,dip}$ has been set for this value of V_{dip}.

The detection algorithm has been tested for the case of grid outage and for different voltage dips at the grid. The main signals are shown in Fig. 8, where the power quality phenomenon occurs at 0.8 s.

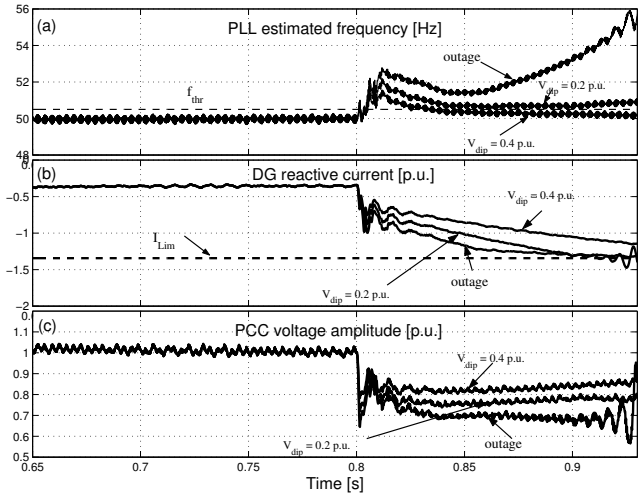

Fig. 8 Estimated frequency (a), DG injected reactive current (b), and PCC voltage amplitude (c) for different amplitudes of the remaining voltage at the PCC (V_{dip}) with IM load (J_L = 0.6).

From the estimated frequency signals, that are shown in Fig. 8(a), it is shown that the detection algorithm will successfully detect islanding for V_{dip} lower than 0.3 p.u. since they are higher than the threshold value f_{thr}. The estimated frequency signal for V_{dip} = 0.4 p.u. (and higher) is below the frequency threshold f_{thr} that is set in the passive detection algorithm, implying that the DG will ride-through this dip. When the DG reactive current, shown in Fig. 8(b), hits the limit (at 0.9 s) for V_{dip} = 0.2 p.u., the PCC voltage, which is shown in Fig. 8(c), will keep a reduced value causing the estimated frequency to increase. On the other hand, for V_{dip} = 0.4 p.u. the current limit is not reached; hence the PCC voltage will continue to increase in a way to regain its nominal value leading to keeping the estimated frequency signal under f_{thr}.

2) J_L = 0.1 and ΔP = 0.2 p.u. (low inertia load):

In this case the load inertia constant is set to 0.1, and the active power mismatch is 0.2 p.u. The effect of changing the current limit is examined regarding the reliability of the detection algorithm in case of a voltage dip of 0.3 p.u. remaining magnitude that occurs at 0.8 s. I_{Lim2} is set for the

detection algorithm to ride through voltage dips lower than 0.3 p.u., while I_{Lim1} is set for a respective value of 0.2 p.u. Using I_{Lim2}, the DG injected reactive current will reach the limit at 0.95 s, as shown in Fig. 9(b). However, due to the constant decrease in the PCC voltage, shown in Fig. 9(c), the IM will draw an increased current leading to an increased estimated frequency, as shown in Fig. 9(a). Hence, the islanding detection will start the island operation at 1.05 s. On the other hand, using I_{Lim1} will not start the island operation, in the considered time scope, due to the slow dynamics of the system. Hence, regarding the grid codes, where the low values of voltage dips should be either cleared, or the DG should disconnect after a relatively short period (e.g. small and medium sized power plants should disconnect after 0.22 s for a 0.22 p.u. voltage dip to comply with the ride-through demand of Svenska kraftnät the national TSO in Sweden [10]), the operation using I_{Lim2}, is preferred.

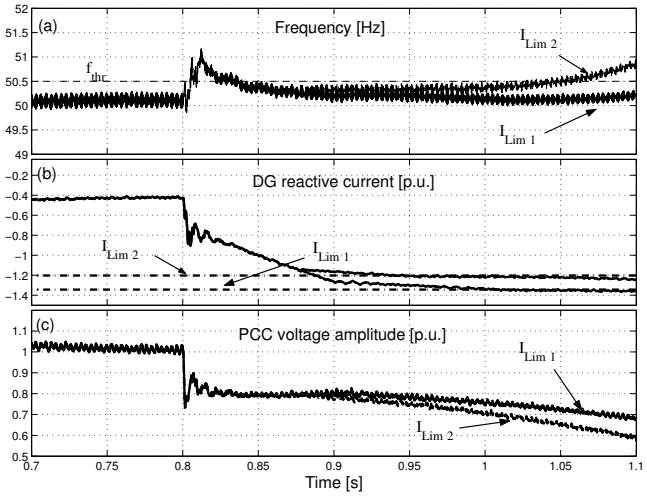

Fig. 9 Estimated frequency (a), DG injected reactive current (b), and PCC voltage amplitude (c) for two values of the current limit with IM (J_L= 0.1).

V. Conclusions

In this paper an active islanding detection method has been proposed. It consists of three parts; a passive detection algoritm that utilizes the estimated frequency signal, a PCC voltage regulator and a dynamic current limiter. The detection algorithm is devoted to a converter interfaced DG operation and can be implemented in both a strong or a weak grid, where the weak grid states are not stiff. Its robustness has been tested against voltage dips at the PCC, where an induction motor load represented the island loads. It has been shown that by setting the proper current limit, the detection algorithm is robust. Moreover, for lower remaining voltage at the PCC and slow dynamics (e.g. due to the load inertia) a trip signal will result after a relatively long period. This is a required practice since it allows time for the fault clearing, and in case of the fault is not cleared the island operation starts (as recommended by the grid codes).

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VII. Biographies

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