Advanced System Level ESD Scanning

How much margin do you have?

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System ESD Architecture
PROBLEM 1: Hard System Fails

When ESD **Hard** Failures Occur...

(System Qualification Fails / Field Returns)

**WHO IS AT FAULT?**

Hard Failures and EOS at the chip level are *usually* obvious, but the solutions at the system level are not!

Examples:
* Secondary Discharges
* Snapback Devices unloading bypass capacitors
* Induced Cable Discharge Events

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Figure 7: SEM image of the fully-silicided I/O buffer with Nwell ballasting technique on the buffer NMOS after 4.5kV ND-mode ESD stress.
PROBLEM 2: Soft Failures

When Non-Destructive Soft Failures occur, or latent ESD damage accrues...

...how to identify the right system nodes to begin analysis on?

Figure 9: cross section and close-up of CUT A
Bridging the Chip ↔ System Gap

ASIC Vendor
ESD Pad Design $$$/Time

System Designer
Limited ESD/EMI Resources

END SYSTEM ROBUSTNESS
Hard Failures? Soft-error/Upsets due to ESD? Root cause?

TVS Vendor
Band-Aids
## System ESD Event Analysis Techniques

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<td>( I_{\text{residual}} ) Current into DUP</td>
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System Transient Event Analysis Tools

- Several tools are now available to the EMC engineer to help resolve EMC issues, insure better reliability and future EMC compliance. These include:
  - ESD/EMC Immunity scanning
  - RF Immunity Scanning
  - EMI Emissions scanning with Phase Measurements
  - Resonance Scanning
  - Current Spreading scanning
1st Order ESD Analysis

1) Obvious Entry Vector

2) Obvious Shunt Path

3) Clear Failure Criteria

> GFTDS
**2\textsuperscript{nd} Order \( I_{\text{residual}} \) ESD Analysis**

KCL Current split between TVS and “Protected Device”/ASIC

Inductive Current Probe Measures "Secondary" shunt current on the node in question (i.e. USB D+)

This assumes, however, that the "problem current" is in the I/O node of interest. What about elsewhere?

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**Diagram Notes:**
- TVS
- PCB GND
- O-scope
- ASIC
- Core
- SOC GND

**Legend:**
- Color scale (0.003 to 0.35)

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ESD Simulation Concept

Accurate Modeling required to predict system level robustness with simulated ESD pulse applied

IT'S ONLY FOCUSED ON A SINGLE I/O LINE AT A TIME
ESD Susceptibility Scanning

**Susceptibility Scanning setup**

**STEP 1:**
Inject an X*Y Array of Increasing step-test ESD pulses Into a moving loop probe (1kV, 2kV, 3kV etc at each point until failure)

**STEP 2:**
Log the ESD "fail level" in the step test where the system malfunctions, and plot it with a color enhanced 2D image to show ESD "hot spots"
Probe Resolution (Transmit)

- Hx/Hy/Hz fields must be considered or combined
- E fields can distort unshielded probe readings
- Don't take levels for granted...they have a spatial component
  (Steps integrate levels)

Modified TLP *Induced* Voltage in PCB
Modified TLP applied *Probe* Voltage
Failure Criteria for Susceptibility?
(BER? Eye degradation? Catastrophic failure?)

LVDS port with TVS

LVDS w/ TVS after IEC testing; 500V steps thru 5kV; Then 12kV 3 times
Susceptibility Scanning

- **Soft** Failure Analysis of running system

- Inverse of EMI Scanning, same fixture

- Modified TLP (or HMM) pulse is directly applied to I/O Ports, time domain EMI scan of PCB

- 2D representation vs. time movie possible showing where the charge goes

* Images Courtesy API
“Relative Susceptibility” Example
(Different Chip Versions, same Function)

* Images Courtesy API
ESD Current Reconstruction Scanning
Probe Resolution (Receive)

- Hx/Hy/Hz fields must be considered or combined
- E fields can distort unshielded probe readings
- Don't take levels for granted...they have a spatial component

(Steps integrate levels)

Modified TLP Recorded Voltage in PROBE

Modified TLP applied NODE Voltage
**Current Reconstruction setup**

**STEP 1:**
Inject a series of low-level ESD pulses into a particular I/O port of interest...

**STEP 2:**
Log the data from a scanning loop probe above the board, and plot it with a color enhanced 2D image to show ESD "hot spots"
Consider a small PCB section with an applied transient pulse……

Note each trace is 16 samples deep…..
…and there are 3x3 points scanned.
Overlay the Susceptibility map to find localized Hotspots

Susceptibility does NOT necessarily imply Vulnerability!
Now slice up these scans into the depth of each scope capture.

Each frame is 9 points (3x3). There are 16 frames from t=1 to t=16.

Note: Trigger accuracy is critical!!!!!
Data Visualization of both methods.

Take Current Reconstruction... ...mask with Hotspots... ...and **NOW** you have potential vulnerabilities identified.

Note that the most critical System vulnerability in this case (right) was NOT the most susceptible area on the PCB (top).
Scanner Probe Traversing DUT

TLP/HMM Injection (USB)
Example of USB strike causing Ethernet soft error…

(1) ESD pulse is injected into USB port (Units in A/m)

(2) ESD Clamp shunts majority of pulse to ground plane

(3) Residual Current shunted by clamps inside ASIC

(4) Some energy coupled into nearby nodes (Ethernet port) causing upset
Imagine debugging this "USB-caused Ethernet upset" without this tool!
ESD Scanning: Characterization vs. Qualification
Characterization vs Qualification

- We can see susceptibilities relative to previous "known good boards"
- We can quantify differences between good and problem boards and characterize an apparent margin
- This could be used to gauge a relative Figure of Merit for a new/unknown design.
Current Reconstruction Analysis of a System Board

Susceptibility Scanning (Moving Probe Inductive Stimulus)

- PING/“Alive/Upset” Detect
- Sensitive Hotspots Found
- Post Process
- Modified TLP
Current Reconstruction
(External I/O Stimulus)
Current Reconstruction
(Internal Node Stimulus)
Upset Root-Cause Analysis
Which System Level Discharge Path Causes ESD Upset Event

Sensitive Hotspots Found

Hotspot Which is Vulnerable to Likely ESD Entry Vectors

Add TVS Protection to this node or route discharge path away from this node on the PCB!
3D Reality
Of 2D
Analysis
Of 1D Nets

"Be the Charge, Danny."

Consider how the crowd enters and exits a stadium.
System vs. Module vs. Component Domains

What is the extent of your concern?

HBM/CDM = Component Assembly

??? = “Module”

HMM/IEC = Whole System Used by Operator
Potential Transient Types and Entry Vectors

ESD, EOS, EFT, Surge

System    Module    Component
Next Generation:

PEAT Embedded ESD Scanning

Pragma ESD Analysis Tool
SOLUTION: Pragma ESD Analysis Tool
2nd Generation I\textsubscript{residual}
→ 4th Generation Embedded Scan
Using PEAT

1* Set IEC gun voltage at a low, non-error inducing level
2* Read JTAG PEAT status registers after each Zap
3* Increase gun voltage and repeat 2-3

Susceptibility level and entry vector may be extracted from this dataset.
System Debug/Co-Design Example

PEAT3: PRAGMA ESD ANALYSIS TOOL
© PRAGMA DESIGN 2011, ALL ZAPS DESERVED
INITIATING COMMUNICATION WITH DUT
SUCCESSFUL!
ENTERING ESD ANALYSIS LOOP
READING JTAG REGISTERS....
3 DEVICES DETECTED
NO ESD EVENTS CURRENTLY LOGGED.
0022 LIFETIME ESD EVENTS LOGGED FOR THIS SYSTEM
ENTERING MONITOR LOOP 1/5/2013 09:08:43
APPLY ESD SIMULATOR NOW.
......*TRIGGER*
ESD NMI EVENT DETECTED
READING JTAG REGISTERS....
3 DEVICES DETECTED
2 DEVICES REPORT ESD ACTIVITY
#0023: [DEVICE 2] PIN A7 STAGE2
#0024: [DEVICE 2] PIN A8 STAGE2
#0025: [DEVICE 2] PIN B6 STAGE3
#0026: [DEVICE 3] PIN 12 STAGE4 <-PERMANENT DAMAGE? (IO=0)
#0027: [DEVICE 3] PIN 13 STAGE2
0027 LIFETIME ESD EVENTS LOGGED FOR THIS SYSTEM ENTERING MONITOR LOOP
1/5/2013 09:12:18
APPLY ESD SIMULATOR NOW.
......
For more info....

Current Reconstruction Animation

Susceptibility Scanning Animation

Questions and Actual Scan Videos, email:
  info(at)pragma-design(dot)com
For more info....

Scanning System Hardware:
Amber Precision - http://amberpi.com/

Other Pragma Design Services:
http://wwwpragma-design.com/pd/index.php/services