IEEE SSCS Lehigh/Princeton/Columbia Chapters Present

Distinguished Lecture Colloquia, October 2014

October 16, 2014, 1:30–2:45 pm

On-Chip Voltage and Timing Diagnostic Circuits

Frank O'Mahony, Intel

Abstract: This talk introduces a set of practical and powerful techniques and circuits to observe and characterize on-die circuitry. Measuring voltage and timing information on the chip itself alleviates the bandwidth and noise limitations associated with bringing signals off-chip to be measured. Specific applications of these techniques include measurement and characterization of power supply noise, power delivery impedance, clock skew, phase interpolator linearity, I/O eye margins, waveform capture, RX voltage noise and hysteresis, and RX clock-data jitter. Because the measurements are fully integrated, the rest of the system can be automatically adapted based on these metrics in a stand-alone manner. Best of all, many of these techniques leverage existing circuitry and are highly digital.

October 16, 2014, 3:00–4:15 p.m.

Millimeter-wave and Terahertz Integrated Circuits in Silicon Technologies: Challenges and Solutions

Prof. Payam Hedari, University of California Irvine

Abstract: The vastly under-utilized spectrum across millimeter-wave (mm-wave) and terahertz (THz) bands has generated great deal of excitement to investigate futuristic systems for 10+ gigabit short-range wireless as well as wideband sensing/imaging applications. Simply put, the shorter wavelength associated with the mm-wave/THz band is appealing since the physical dimensions of the antenna and associated electronics are reduced in size, making it possible to design multi-antenna structures to achieve beamforming, spatial diversity and multiplexing.

Owing to aggressive scaling in feature size and device fT/fmax, nanoscale (Bi)CMOS technology potentially enables integration of sophisticated systems at THz frequency range, once only be implemented in compound III-IV semiconductor technologies.

This talk will give an overview of recent advances in designing silicon-based integrated circuits will be capable of operating close to the maximum operation limits of silicon-based transistors. The talk then will discuss in depth about two case studies designed in UCI's Nanoscale Communication Integrated Circuits (NCIC) Labs; namely, the world's highest fundamental frequency fully differential transceiver in CMOS at 210 GHz, and the world's highest frequency PLL-based Synthesizer in Silicon at 300GHz with a wide tuning range.

October 16, 2014, 4:30–5:45 p.m.

Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design

Prof. R. Jacob Baker, University of Nevada, Las Vegas

Abstract: This work proposes a novel DRAM module and interconnect architectures in an attempt to improve computing energy use and performance. A low cost advanced packaging technology is used to propose an 8 die and 32-die memory module. The 32-die memory module measures less than 2 cm3. The size and packaging technique allow the memory module to consume less power than conventional module designs. A 4 Gb DRAM architecture utilizing 64 data pins is proposed. The DRAM architecture is inline with ITRS roadmaps and can consume 50% less power while increasing bandwidth by 100%. The large number of data pins are supported by a low power capacitive-coupled interconnect. The receivers developed for the capacitive interface were fabricated in 0.5 µm and 65 nm CMOS technologies. The 0.5 µm design operated at 200 Mbps, used a coupling capacitor of 100 fF, and consumed less than 3 pJ/bit of energy. The 65 nm design operated at 4 Gbps, used a coupling capacitor of 15 fF, and consumed less than 15 fJ/bit and order of magnitude smaller consumptions than previously reported receiver designs.

Contact Info: Nagi Naganathan, nagisub@gmail.com or Kaushik Sengupta, kaushiks@princeton.edu

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Speaker: **Frank O'Mahony**
Intel

Title: **On-Chip Voltage and Timing Diagnostic Circuits**
Date: Thursday, October 16, 2014
Time: 1:30 – 2:45 p.m.
Location: Princeton University, Department of Electrical Engineering
Engineering Quadrangle, Room B205
Olden Street
Princeton, NJ 08544

Abstract: This talk introduces a set of practical and powerful techniques and circuits to observe and characterize on-die circuitry. Measuring voltage and timing information on the chip itself alleviates the bandwidth and noise limitations associated with bringing signals off-chip to be measured. Specific applications of these techniques include measurement and characterization of power supply noise, power delivery impedance, clock skew, phase interpolator linearity, I/O eye margins, waveform capture, RX voltage noise and hysteresis, and RX clock-data jitter. Because the measurements are fully integrated, the rest of the system can be automatically adapted based on these metrics in a stand-alone manner. Best of all, many of these techniques leverage existing circuitry and are highly digital.

Bio: Frank currently leads the I/O Circuit Technology group within Advanced Design at Intel in Hillsboro, Oregon, where he is a Principal Engineer. His group develops the first wireline I/O circuits for each new CMOS process technology at Intel. From 2003 until 2011 he was a member of the Signaling Research group in Intel's Circuit Research Lab. His research interests include high-speed and low-power wireline transceivers, clock generation and distribution, equalization, analog circuit scaling, and on-die measurement techniques. Frank received the BS, MS, and PhD degrees in electrical engineering from Stanford University. Frank is a member of the ISSCC Wireline Subcommittee and previously served as an Associate Editor for TCAS-I. He is a past recipient of the ISSCC Jack Kilby Award and TCAS Darlington Best Paper Award.

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Bio: Payam Heydari received his B.S. and M.S. degrees (Honors) in Electrical Engineering from Sharif University of Technology in 1992 and 1995, respectively. He received his Ph.D. degree from the University of Southern California in 2001. He is currently a Professor of Electrical Engineering at the University of California, Irvine.

His research covers the design of terahertz/millimeter-wave/RF/analog integrated circuits. He is the (co)-author of two books, one book chapter, and more than 110 journal and conference papers. He has given Keynote Speech to IEEE GlobalSIP 2013 Symposium on Millimeter Wave Imaging and Communications and served as Invited Distinguished Speaker to the 2014 IEEE Midwest Symp. on Circuits and Systems. He is the Distinguished Lecturer of IEEE Solid-State Circuits Society.

Dr. Heydari is recipient of the Distinguished Engineering Educator Award from Orange County Engineering Council. He is the recipient of the 2010 Faculty of the Year Award from UC-Irvine's Engineering Student Council (ECS), the 2009 School of Engineering Best Faculty Research Award, the 2007 IEEE Circuits and Systems Society Guillemin-Cauer Award, the 2005 IEEE Circuits and Systems Society Darlington Award, the 2005 National Science Foundation (NSF) CAREER Award, the 2005 Henry Samueli School of Engineering Teaching Excellence Award, and the Best Paper Award at the 2000 IEEE Int'l Conference on Computer Design (ICCD). The Office of Technology Alliances at UCI has named Dr. Heydari one of 10 Outstanding Innovators at the university. He is the co-recipient of the 2009 Business Plan Competition First Place Prize Award and Best Concept Paper Award both from Paul Merage School of Business at UC-Irvine. He was recognized as the 2004 Outstanding Faculty in the EECS Department of the University of California, Irvine. His research on novel low-power multi-purpose multi-antenna RF front-ends received the Low-Power Design Contest Award at the 2008 IEEE Int'l Symposium on Low-Power Electronics and Design (ISLPED).

Dr. Heydari currently serves on the Technical Program of International Solid-State Circuits Conference (ISSCC). He served as the Guest Editor of IEEE Journal of Solid-State Circuits (JSSC), and Associate Editor of IEEE Trans. on Circuits and Systems - I, and served on the Technical Program Committees of Compound Semiconductor IC Symposium (CSICS), Custom Integrated Circuits Conference (CICC), and ISLPED. He served on the Technical Program Committees of and Int'l Symposium on Quality Electronic Design (ISQED), IEEE Design and Test in Europe (DATE) and International Symposium on Physical Design (ISPD). He is the director of the Nanoscale Communication IC (NCIC) Labs.

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Bio: R. Jacob Baker is a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas. His research interests lie in integrated electrical/biological circuits and systems, interfacing CMOS to Silicon Photonics, and the delivery of online engineering education. He has extensive industry experience and is the author of several circuit design books. Additional information can be found at http://CMOSedu.com.

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