An overview of mixed-signal IC Verification with Behavioral Models

Date: December 2, 2010 (Thursday)

Time: 6.00 -6.30 pm - Networking/ Refreshments
6.30 - 7.30 pm -Talk
7.30 - 8.00 pm - Q&A

Place: CoRE 538
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SPEAKER: DR. ROBERT PERUZZI

Abstract:

Integrated circuit geometries continue to shrink and the cost of fabrication masks can cost millions of dollars. The probability of human error going undetected coupled with the high cost of mask revision as well as the cost of sales opportunities lost during months of revision makes IC verification imperative.

Digital, analog and RF electrical circuits were at one time kept on separate chips, and their verification methodologies evolved down three separate paths (Digital Chips, Analog Chips, Radio-Frequency Chips).

All was well when they were kept separate. But there was market share to be grabbed and lots of money to be made by combining them all into one chip, now called a "**System on a Chip**" or **SoC.** Like squirrels at a bird feeder, engineers found a way past physical barriers to combine the three circuit types, but doing so made debugging them impossible with any one of the three existing verification methodologies.

The best solution so far is to make the verification of ICs with analog and RF sub-circuits compatible with digital verification by substituting behavioral models for the analog and RF sub-circuits. Behavioral models make it possible to verify large circuits at all levels, by making analog and digital circuitry compatible with the mature and effective digital verification methodology. Doing so increases the likelihood of successful design – and can save millions of dollars by eliminating human errors. Without behavioral models the interaction between analog and digital functional areas of the chip cannot be verified, resulting in a significant risk exposure.

In this tutorial talk I present several analog functional blocks and show examples of their behavioral models written in the **Verilog-AMS** language, including a testbench coded in Verilog-AMS and a Verilog-AMS driver/monitor model which drives the input signals and monitors and tests the output signals

Speaker Bio:

Robert Peruzzi is president and sole employee of R. Peruzzi Consulting, Inc. As a PE-licensed electrical engineering consultant he specializes in behavioral modeling and verification of RF, Analog and Mixed-Signal IC and SoC Designs.

He moved to the Lehigh Valley in 1990 to work as an ATE test developer for AT&T Bell Labs, where he took advantage of their tuition assistance plan and earned his Ph. D. in 2005 after what seemed like an eternity of part time study. He stayed on as that company evolved into Lucent, Agere, LSI and Infineon. As opportunities arose he crossed between departments, working in analog and mixed signal design. Along the way he picked up expertise in Verilog-AMS, VHDL-AMS, Simulink and other design and verification skills, which have turned into his engineering passion and a nice niche for private practice.

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