A Seminar on Advanced Nano CMOS finFET Technology

Intended for all IEEE members, including faculty and Students in Computer Engineering, Electrical and Microelectronic Departments at RIT

Date and Time: February 6, 2015 12:00 noon to 12:50 PM

Place: Xerox Auditorium, KGCOE, Rochester Institute of Technology

Pizza and Soft drink will be served immediately at the end of talk in the Gordon Atrium

Cosponsors:

RIT Departments of Computer Engineering, Electrical and Microelectronic Engineering, and IEEE RIT CS Student Branch Chapter, IEEE Electron Devices Chapter and IEEE Joint Chapter of Computer and Computational Intelligence Society in IEEE Rochester Section

For further information, contact Dr. Ken Hsu, kwheec@rit.edu

Topic: Overview of FinFET technology at 14 nm node and beyond

Abstract:

The bulk-FinFET technology is continuously progressing to 14 nm node as the 2nd generation of bulk-FinFET technology continuously driving CMOS scaling and Moore's law for ***low-power/SOC mobile electronics.*** The new bulk-FinFET features active fin profile control, solid source sub-fin doping(for suppression punch-through leakage), fully depleted fin channel (for minimizing variations of Vt), and advanced BEOL interconnect with air-gap and self-aligned dual-patterning. The doping diffusion control by C or F is needed in order to prevent the sub-fin doping into the channel. The multi-Vt scheme can be implemented by multi-fin-width, or mlti-Vcc or Lg scheme, or by multiple fin slopes for low power applications. Finally, the self-aligned contact and gate metals provide new knobs (in addition to the usual stressor S/D epi) for strain engineering for FinFET toward higher performance at lower Vic and power.

Biography: Dr. Min-hwa Chi (min-hwa.chi@globalfoundries.com)

Dr. Min-hwa Chi received his BS, MS, and Ph.D. in EE at National Taiwan University (1974), University of Rhode Island (1977), and University of California-Berkeley (1982) respectively. He has served VLSI Industry in Intel (1982-1988), KFI technology (1988-1994, and National Semiconductor (1994-1997) in NVM, CMOS-Imager, and module process development. He served foundry industry for TSMC, Taiwan (1997-2005) as Sr. Dir. (R&D in DRAM and CMOS Logic and SOC Technology) and SMIC, China (2006-2011) as Sr. VP (TD in NVM, Logic and SOC Technology). Since Oct'11, he joined GLOBALFOURNDRIES, USA as Sr. Fellow and Dir. Advanced programs in TD. He was a guest professor at Peking University (2010-2011) and honorary professor at Fu-Dan University (2008-2010) in China. He is an IEEE Sr. Member (2001). He has 137 US Patents granted, 1 book and 89+ technical papers published in areas of CMOS Logic, Flash memory, Imager, DRAM, and Power devices.