Redefining IC packages with super-thin Substrates

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Abstract

In an industry which demands for continuous innovation and perfection, we are constantly deriving new processes and solutions to break the technological limits which will set us apart. We are striving to achieve denser integrated circuits for better performance as Moore's law perceives and also redefining the word, "Thin". Driven by cost and in order to achieve thinner IC packages, we have created an innovative solution which enables us to produce ultra-thin substrates. This technology allows us to make use of conventional materials such as PICs(photo imagable coverlay) and merging them with substrates to create products as thin as 25um. Our aim is to showcase the advantages of our Super-thin substrates versus the Molded interconnect substrates in terms of process and capability. This project is done and carried out in QDOS Interconnect.

1. Introduction

Substrates and leadframes are the key foundation layer to chip packaging. They are the layer of interconnect that connects the die which carry electrical signals from the terminals to the electrical circuit board that the chip is mounted on. Both substrates and leadframes are used in almost all semiconductor packages, ranging from power management devices, radio frequency packages to small diode packages. There are significant contrast between the advantages and disadvantages of both substrates and leadframes. Substrates are able to produce fine line packages but the typical package thickness is higher compared to leadframe. On the other hand, leadframes are able to produce very thin packages but is limited to a single layer. To find the sweet spot between these two different technologies, MIS (Molded Interconnect Substrates) was created. MIS is able to produce fine pitch and high density thin packages for high performance applications. There are some limitations to this technology as well. The thin packages are prone to micro cracks the typical package thickness for MIS is ranging from 95um-120um for a single layer. To further enhance and improve on this, Qdos Interconnect is evaluating on certain materials and processes in order to produce super-thin and robust substrates. This study would explain further on the approach on how we will achieve to produce our super-thin substrates.

2. Material Selection and Process Flow

This section would explain on the typical 1-layer MIS (molded interconnect substrate) and material selection with the process steps to develop the new super-thin substrate.

Diagram 2.1 – Cross-section view of 1-Layer MIS

Utilising the build-up technology, fully filled vias, and embedded copper traces, MIS is capable of producing fine line and high density circuitry. The overall package thickness is also reduced further with these features. As the name describes, EMC (epoxy molding compound) is used to embed the traces has a very similar properties which matches the second molding or encapsulation of the package.

The super-thin substrate has nearly similar construction and process. There are several key elements and materials used to create such a substrate. The initial cross-section structure of the super-thin substrate is as below:

Diagram 2.2 – Cross-section view of super-thin substrate

There are primary two main direct materials used to produce this product. 1) PIC Film & 2) Carrier. The PIC (Photo imagable coverlay) film is laminated, exposed and develop before going for the trace copper plating process.

There are several key components in choosing the PIC film. CTE (Coefficients of Thermal Expansion) & Tg (Glass Transition Temperature) values plays a huge role in determining whether there is a mismatch between the substrate and the PIC Film which would cause the substrate to warp out of shape after reflow. PIC is made of polyimide substance which is known for thermal stability, good chemical resistances and mechanical/electrical properties [1].

For this super-thin substrate, the following PIC Film was selected along with it's properties;

Test Item	Test Condition	PIC Film	MIS EMC
Glass Transition Temp	TMA (Tg)	>250°C	~170°C
CTE value	TMA(30~200°C)	<20ppm/°C	Alpha 1= 8 ppm/°C Alpha 2 = 30 ppm/°C
Decomposition Temp	TGA(T_d5%)	>400°C	N/A
Tensile	ASTM D882	>5	N/A

modulus			
Elongation at break (%)	ASTM D882	6.3	N/A
Adhesion	PIC TeMask(um)	50	N/A

Table 2.1 – Test conditions and values for PIC film versus MIS EMC.

These two materials are fundamentally different in both structure and composition. Comparing the PIC film to the typical MIS EMC (Epoxy molding compound), we can observe the differences especially on the glass transition temperature.

In the fabrication of MIS frames, the carrier acts as a solid foundation to support the package that is built up on top on it. During the end process, this carrier would be chemically etched off to expose the copper trace layer which was built on it for die attachment purposes. The carrier must be robust enough to withstand certain temperatures and chemical processes throughout the fabrication of the frames. Typically steel is the main material used for the carrier. The carrier remains unchanged for developing the super-thin substrate and will be etched off once the die has been attached and encapsulated.

The copper plating process is essential in creating a super-thin package as it requires the plating variations to be minimal. This can be achieved by using flat-top copper plating process to produce a consistent plating height and without the plating "mushroom" phenomenon with is typical in common electrolytic copper plating processes. This will not only improve the quality of the copper plating process, but will also have significant impact on the cost.

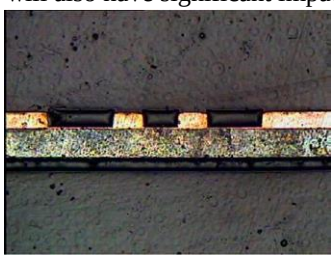

Diagram 2.3 – Cross section of product using flat-top copper plating.

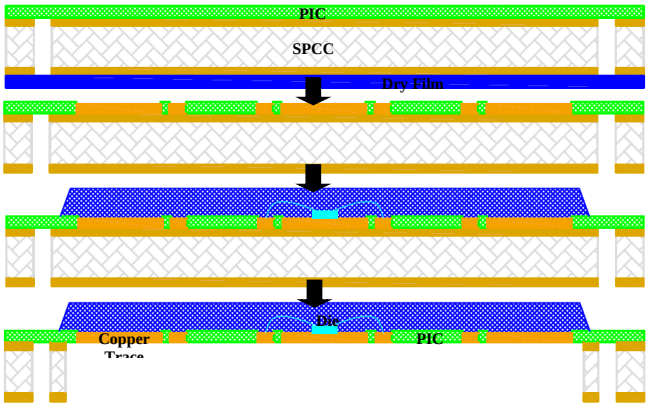

Diagram 2.4 – Super-thin substrate process flow

The super-thin substrate process flow is similar with the typical one-layer MIS process. The main differences are that instead of using molding compound, we replace it with the PIC film. The process is also shortened as we only have a trace copper layer to plate. A layer of surface finishing chemicals is applied on the surface of the unit for bonding purposes. The frames are then sent for die-attached and encapsulation before doing the window opening to expose the trace layer for board mounting purposes.

Item	MIS	Super-Thin Substrate
Warpage	<1.5mm	<1mm
Crack	Prone to crack	More robust due to PIC material
Substrate Package Thickness	~95um	<50um
Line to Line Space	Fine Line (<20um)	Fine Line (<20um)

3. Test Results

To test out the plating consistency, copper plating tests were conducted and the readings were measured and recorded.

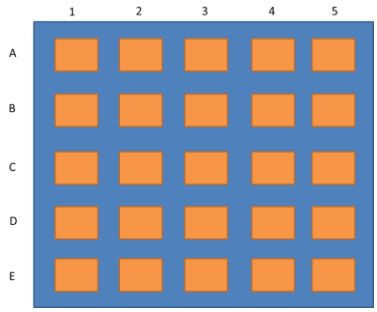

Diagram 3.1 – Panel and unit locations

No.	1	2	3	4	5
A	32um	29um	32um	33um	32um
B	31um	30um	30um	32um	31um
C	28um	27um	28um	29um	32um
D	33um	29um	31um	30um	29um
E	32um	31um	30um	31um	29um

Table 3.1- Values Measured from Test Panel

From the values obtained, we observed that the plating consistency to be consistent with a max plating value of 33um and min plating value to be 27um (30um±3um). The cross section results are as below:

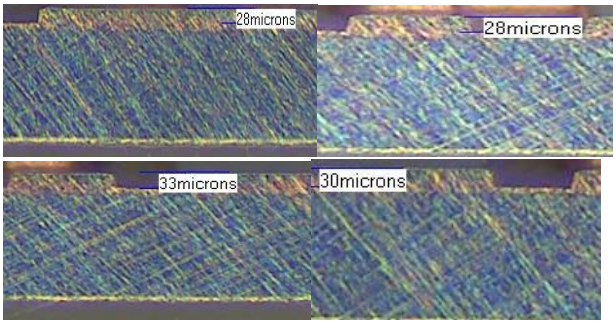

Diagram 3.2 – Cross section of super-thin substrate.

With lesser plating variations we are able to achieve the plating thicknesses desired. The super-thin substrate centers on this main component to be consistent.

4. Conclusions

Compared to MIS, the super-thin substrate is still in the initial stages of development and there are still plenty of room for improvements. The main objective is to create a substrate that is robust and able to achieve very thin packages (25um). Further evaluation is needed to enhance on the process and to be able to create a robust and high performance product.

Acknowledgments

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References

1. https://en.wikipedia.org/wiki/Polyimide 2.