Centre for Research in Image & Signal Processing

MASSEY UNIVERSITY
TE KUNENGA KI PŪREHUROA
UNIVERSITY OF NEW ZEALAND

IEEE
IEEE NZ Central Section

Image Processing in VHDL on FPGAs

Joint Massey University / IEEE NZ Central Section Workshop

Palmerston North
4-6 April, 2018

Course information:

About the Workshop

Field Programmable Gate Arrays (FPGAs) are increasingly being used as an implementation platform for real-time embedded image processing applications because their architecture is able to exploit spatial and temporal parallelism. Unfortunately, simply porting an algorithm onto an FPGA often gives disappointing results, because most image processing algorithms have been optimised for a serial processor. Therefore it is necessary to transform the algorithm to efficiently exploit the parallelism inherent within the algorithm. This course introduces a design approach for FPGA based imaging system development, highlighting the significant differences between hardware and software based design. Through lectures and hands-on laboratories, the basic tools for FPGA based development are introduced, and used for implementing a range of fundamental image processing operations.

Who should attend?

This course is aimed at engineers and scientists who need to understand basic concepts of FPGAs, and how they may be applied to image processing. It is targeted particularly for those who are entering this field, or are looking at using FPGAs for an image processing application. Participants are expected to have some background in basic electronics, mathematics, and programming. A basic understanding of image processing concepts would be helpful, although prior background in FPGAs is not required.

About the Presenter

Professor Donald Bailey has over 35 years of experience in image processing and machine vision. Over the last 15 years he has conducted extensive research in mapping image processing algorithms onto FPGAs. He is the author of many publications in this field, including the book "*Design for Embedded Image Processing on FPGAs*."

Workshop content

Day 1:	Day 2:	Day 3:
Image processing and FPGAs	FPGA based design and algorithm implementation	Geometric transformation Laboratory: Lens distortion correction
VHDL Primer Laboratory: Using Intel's Quartus Prime tools	Histogram processing Laboratory: Histogram display, and histogram equalisation	Colour processing Laboratory: Colour enhancement, and object detection
Image capture Laboratory: Image capture and display, automatic gain control	Temporal processing Laboratory: Background modelling and change detection	Blob processing Laboratory: Connected components analysis, and object tracking
Simulation and debugging Laboratory: Simulation in ModelSim and debugging with Signal-tap	Filters: Convolution and morphology Laboratory: Implementing Sobel filter, and CORDIC arithmetic	Fast Fourier transform Laboratory: Implementing the FFT

Further information

For further information, contact D.G.Bailey@massey.ac.nz
and to register for the workshop, visit http://sprg.massey.ac.nz/course_FPGA.asp