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SOME RECENT DEVELOPMENTS IN THE DESIGN OF BIOPOTENTIAL AMPLIFIERS FOR ENG RECORDING SYSTEMS

John Taylor, Delia Masanotti, Vipin Seetohul and Shiyong Hao

*Department of Electronic and Electrical Engineering
University of Bath, UK*



ACKNOWLEDGEMENTS

Professor N Donaldson, *Department of Medical Physics & Bioengineering
University College, London, UK*

Dr P Langlois, *Department of Electronic and Electrical Engineering,
University College, London, UK*

Dr J Robbins, *Department of Pharmacology, King' College,
London, UK*

Dr A Sapelkin, *Department of Physics, Queen Mary University,
London, UK*

Dr R Rieger, *Department of Electrical Engineering,
National Sun Yat-sen University, Taiwan*

Dr D Pal, *Department of Electronics &
Communication Engineering, B.I.T. Mesra, India*

Dr M Schuettler, *Department of Microsystems Engineering,
University of Freiburg, Germany*

Dr N Rijkoff *Centre for Sensory Motor Interaction (SMI), University of
Aalborg, Denmark*

Engineering and Physical Sciences Research Council (UK) (EPSRC)

SUMMARY

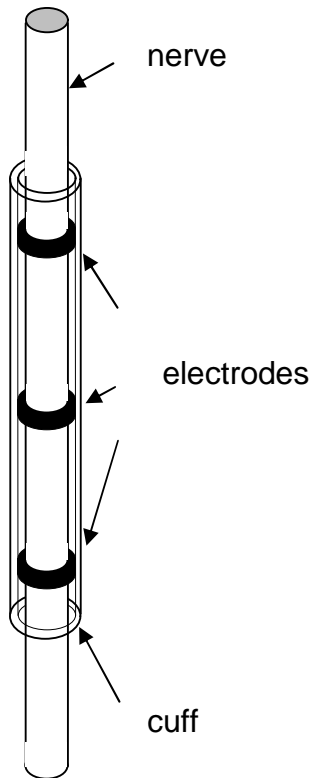
- The importance of real-time recording of *electroneurogram* (ENG) signals
- The difficulties of achieving a stable interface between tissue and electronic devices
- Illustrations of current problems being studied at Bath University
 - 1 *Velocity selective recording* (VSR) of ENG signals
 - 2 *In vitro* recording of ENG from cloned neurons
- Some possible future directions

THE IMPORTANCE OF ENG RECORDING

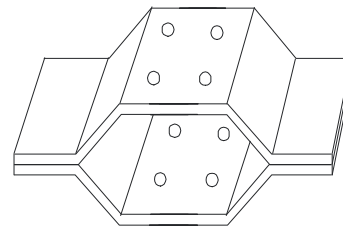
Although this area has been researched for some time, there is still much demand for improved systems for real-time ENG recording. Interest comes from eg:

- *Neuroscientists* requiring experimental data in fields such as neurophysiology and neuropharmacology
- *Engineers* requiring inputs for systems to control *Functional Electrical Stimulation* (FES) systems for a variety of rehabilitation applications such as neurogenic urinary incontinence by stimulation of the sacral roots
- There is a demand for recording methods with improved functionality, eg. Velocity/diameter selective recording (VSR)

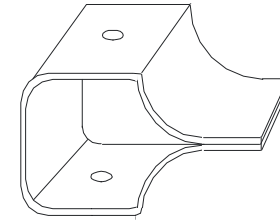
NERVE CUFFS FOR ENG RECORDING



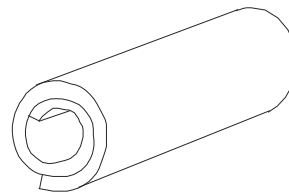
Nerve cuff with tripolar electrode assembly



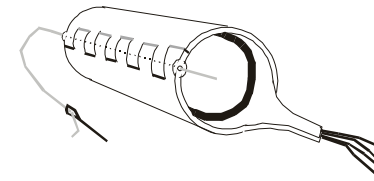
Avery and Wespic (1973)



Avery (1973)



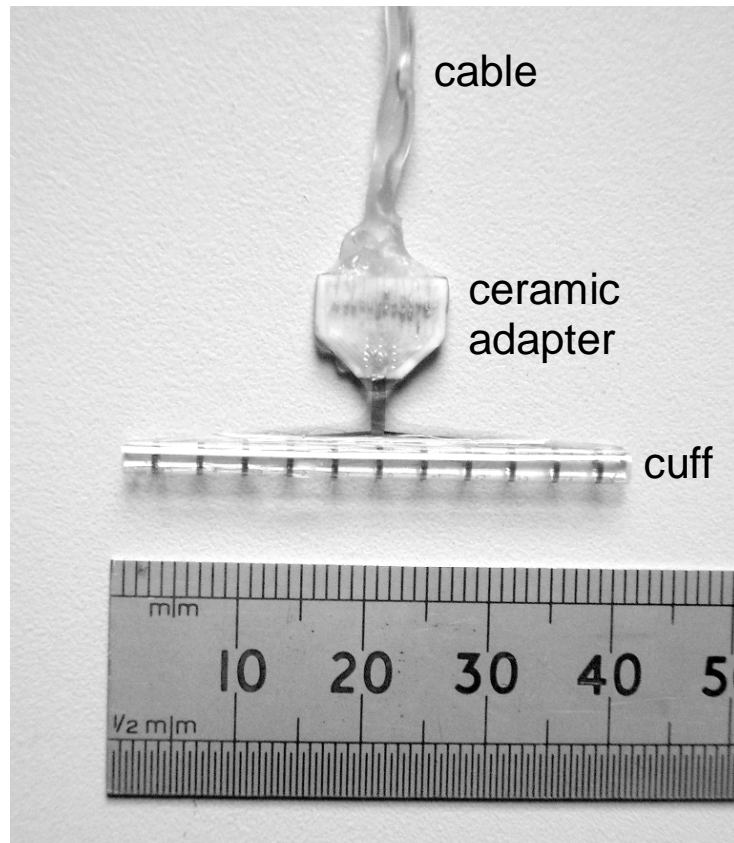
Naples et al (1988)



Kallesoe (1996)

Various types of cuff design

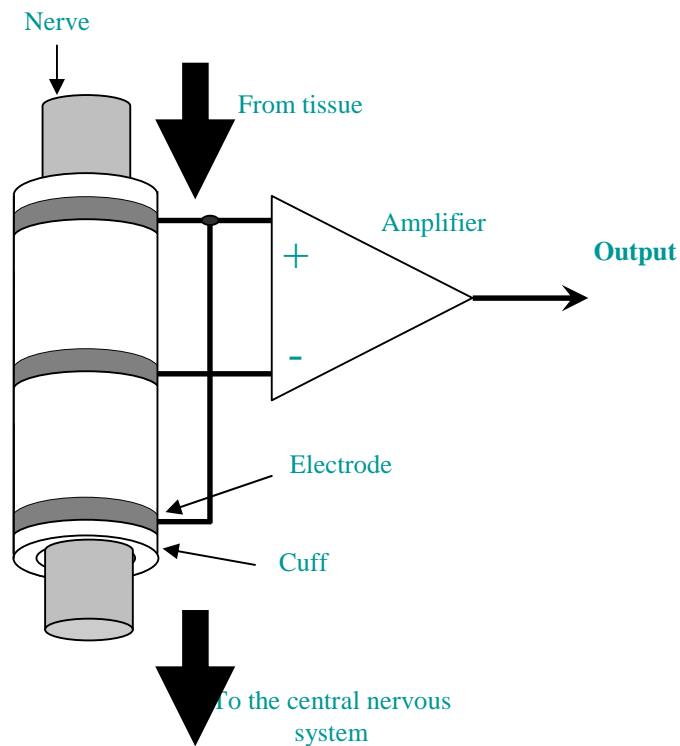
MULTIELECTRODE CUFF (MEC)



- Polyimide thin-film technology
- Sputtered platinum electrodes
- Etched using oxygen plasma.
- The final MEC was 1.5 mm in diameter, 40 mm long and carried eleven 0.5 mm wide, ring-shaped platinum electrodes

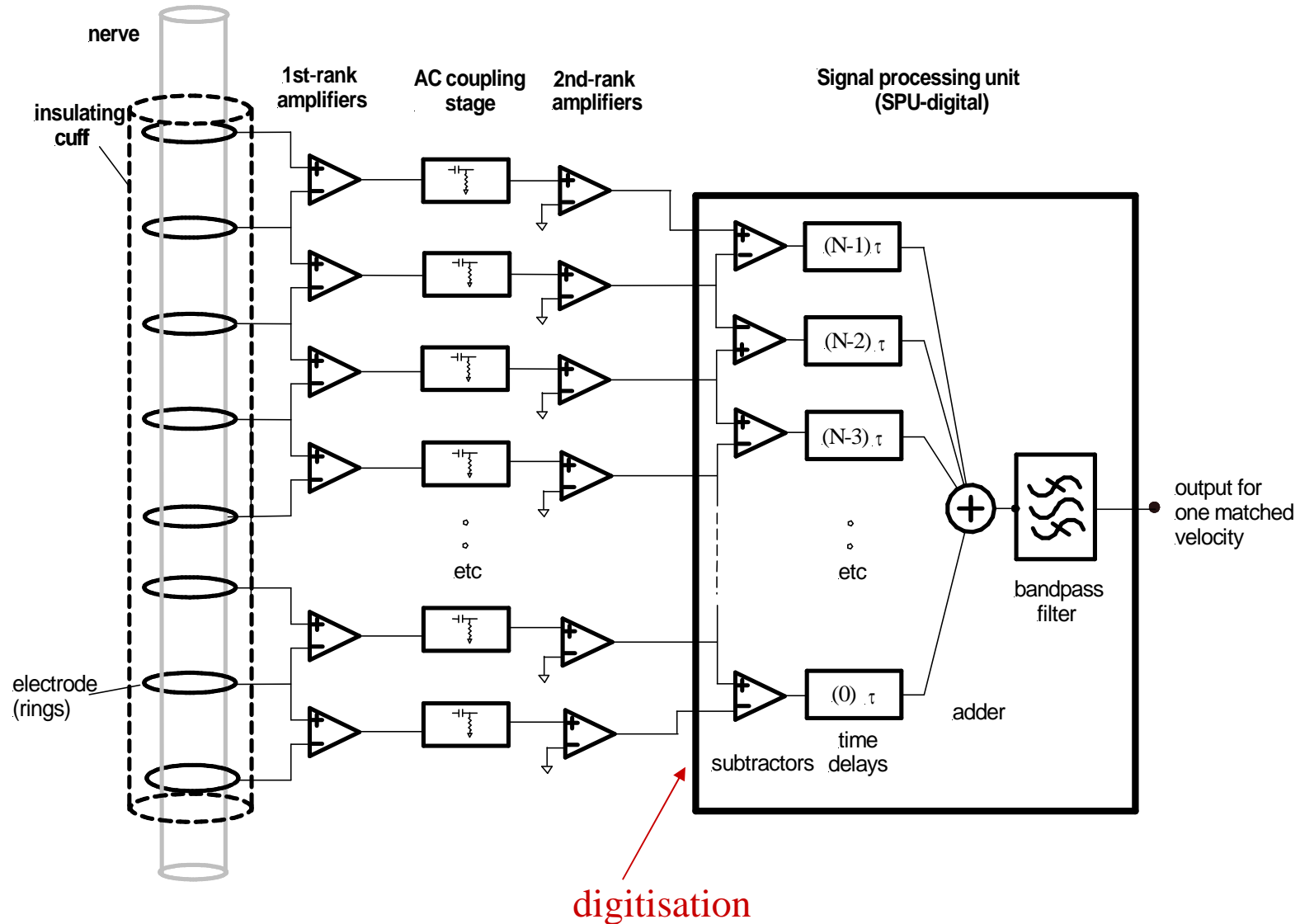
M Schuettler, 2006

RECORDING ENG USING NERVE CUFFS

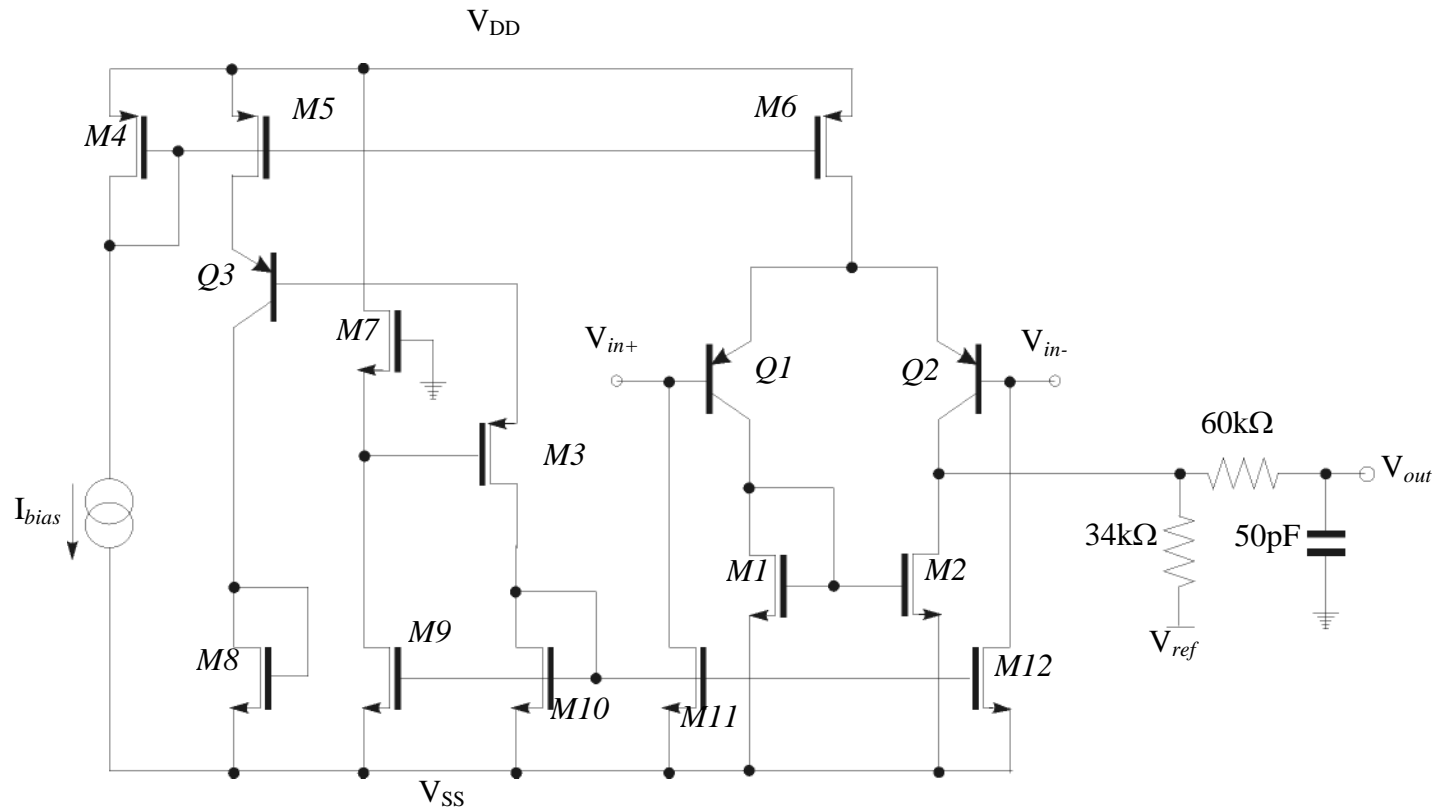


This type of cuff/amplifier connection is called a *Quasi Tripole* (QT). It provides good suppression of EMG and other artifacts. It only requires one amplifier and is relatively simple to implement. It has been much used in practical ENG recording systems.

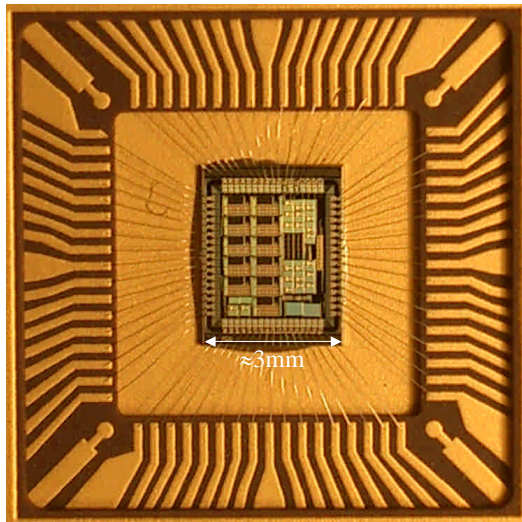
10 CHANNEL ENG RECORDING SYSTEM



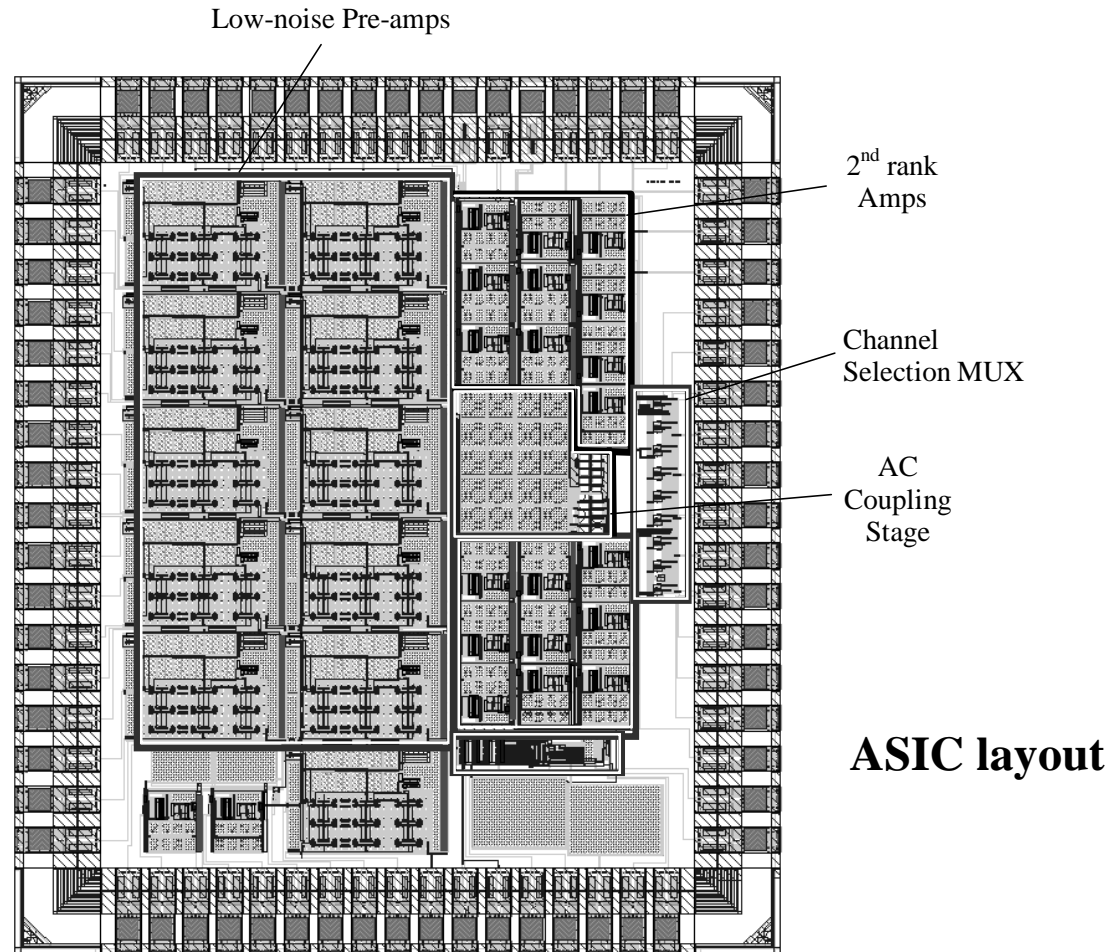
PREAMPLIFIER SCHEMATIC



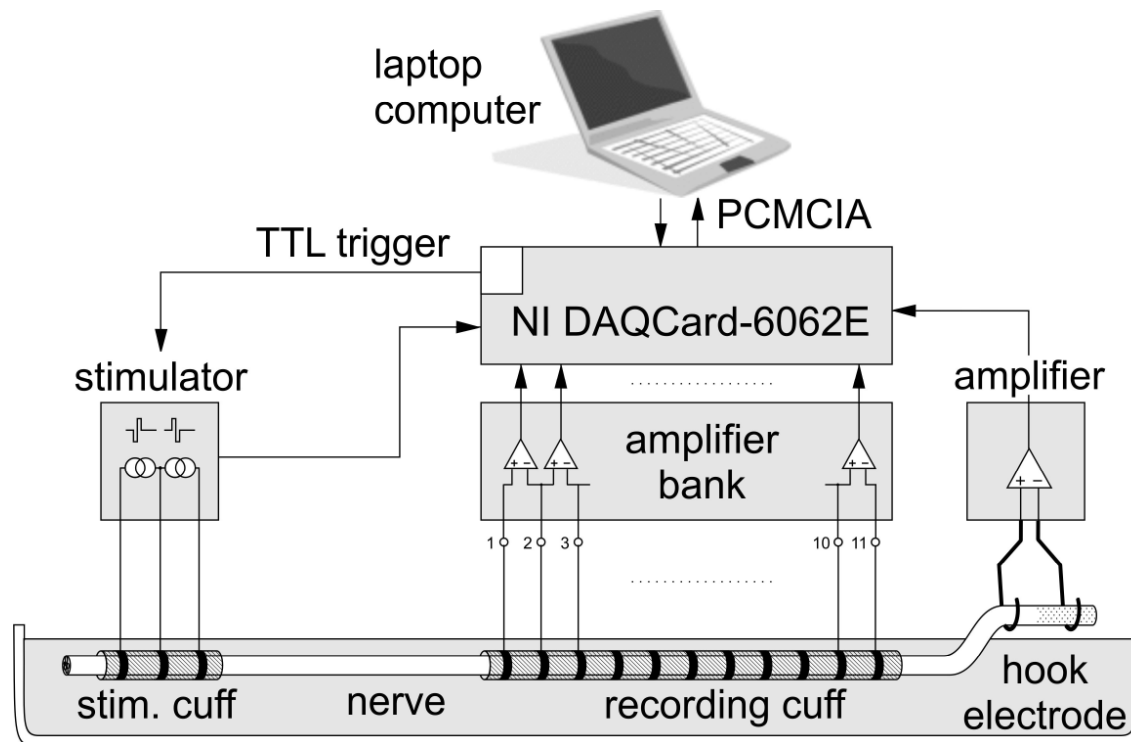
10 CHANNEL ENG RECORDING SYSTEM



Die mounted in PGA package



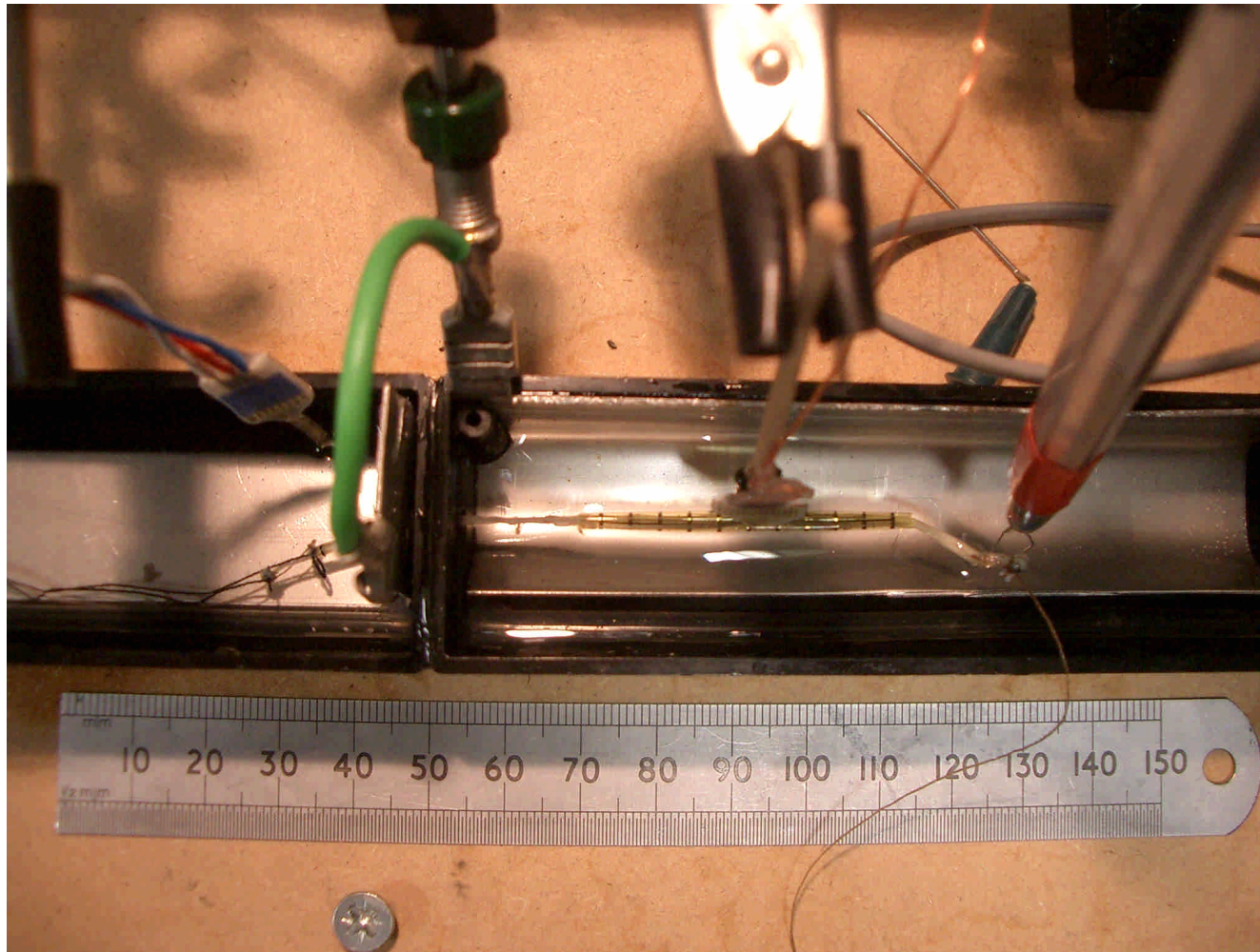
EXPERIMENTAL SETUP FOR MEC RECORDINGS



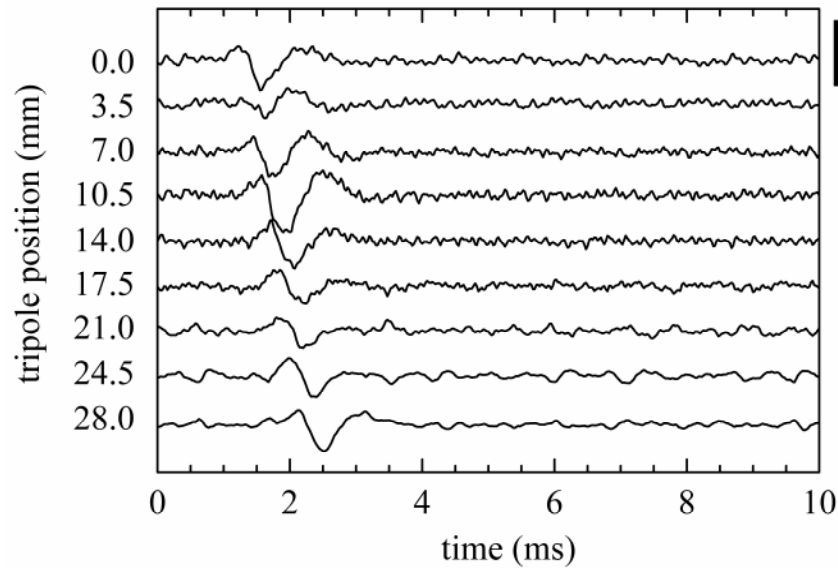
***XENOPUS* FROG PREPARED FOR REMOVAL OF *SCIATIC* NERVE**



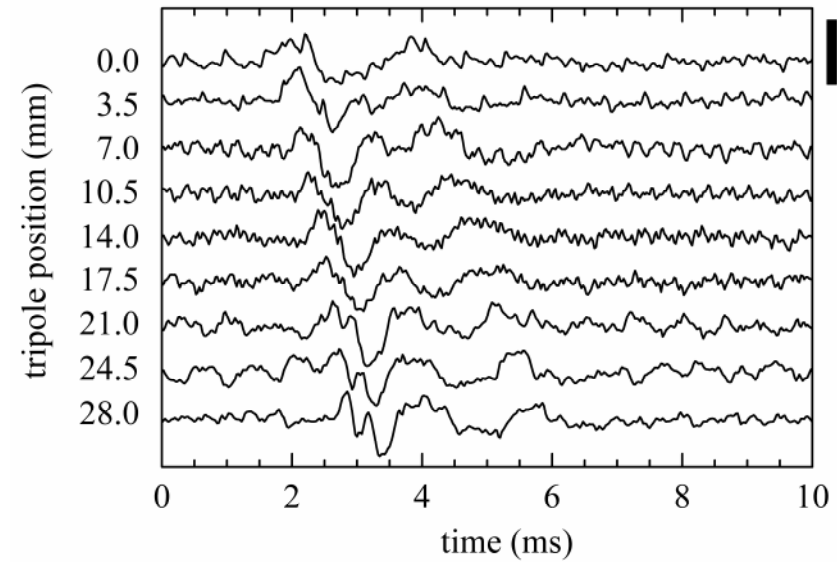
NERVE FITTED WITH MULTIELECTRODE CUFF *IN VITRO*



MEASURED RESULTS IN FROG

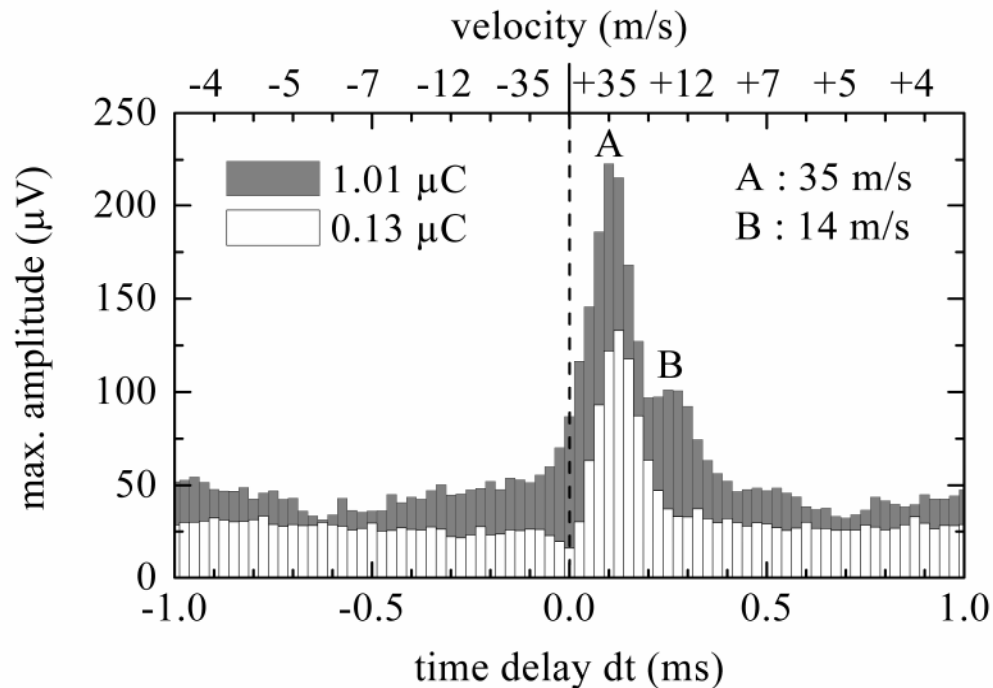


Stimulation intensity $0.13 \mu\text{C}$



Stimulation intensity $1.01 \mu\text{C}$

MEASURED VSR DATA IN FROG



Delay profiles corresponding to two different stimulation intensities:

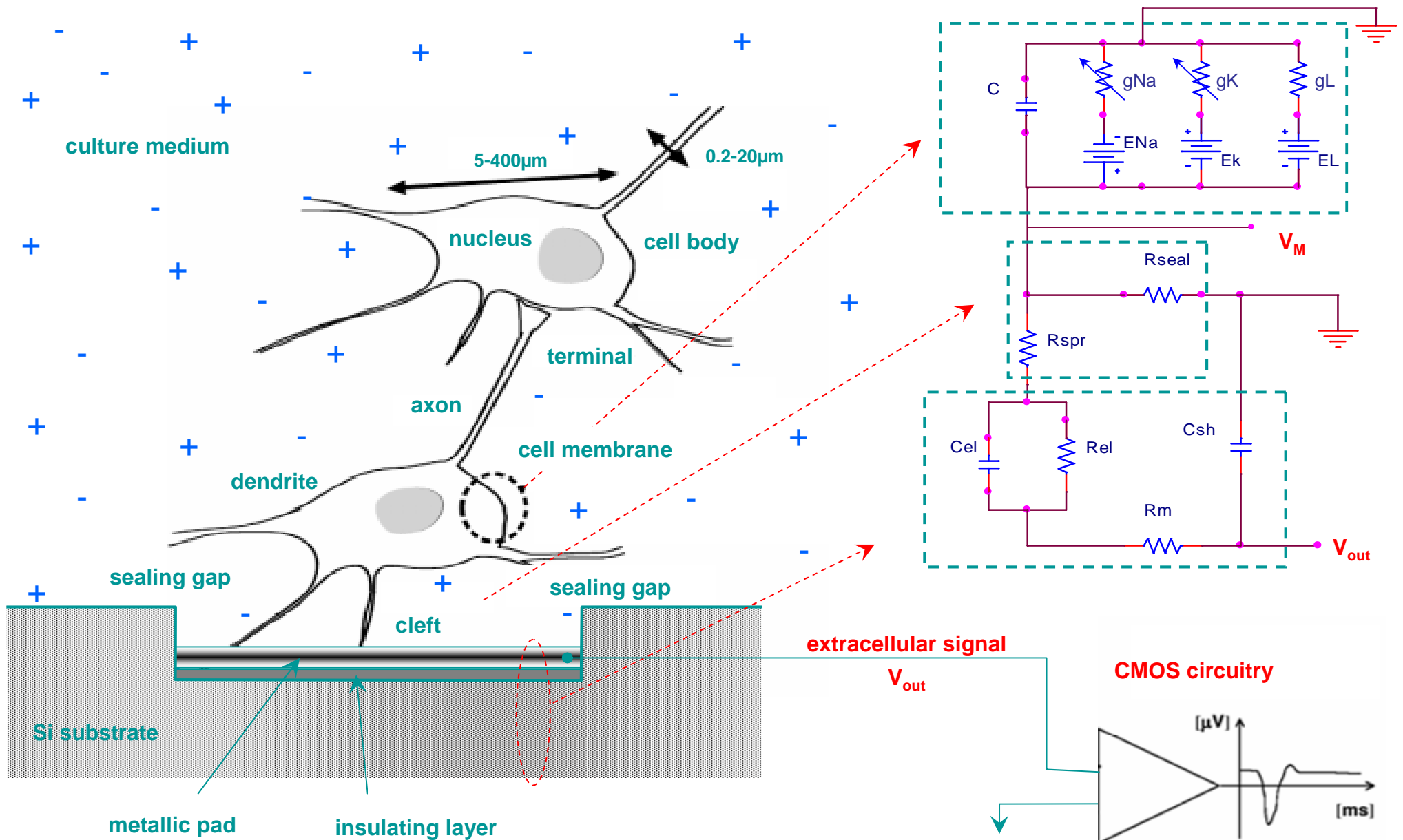
grey: 1.01 μC , *white*: 0.13 μC .

The bars have a width of 25 μs (reciprocal value of the sampling frequency)

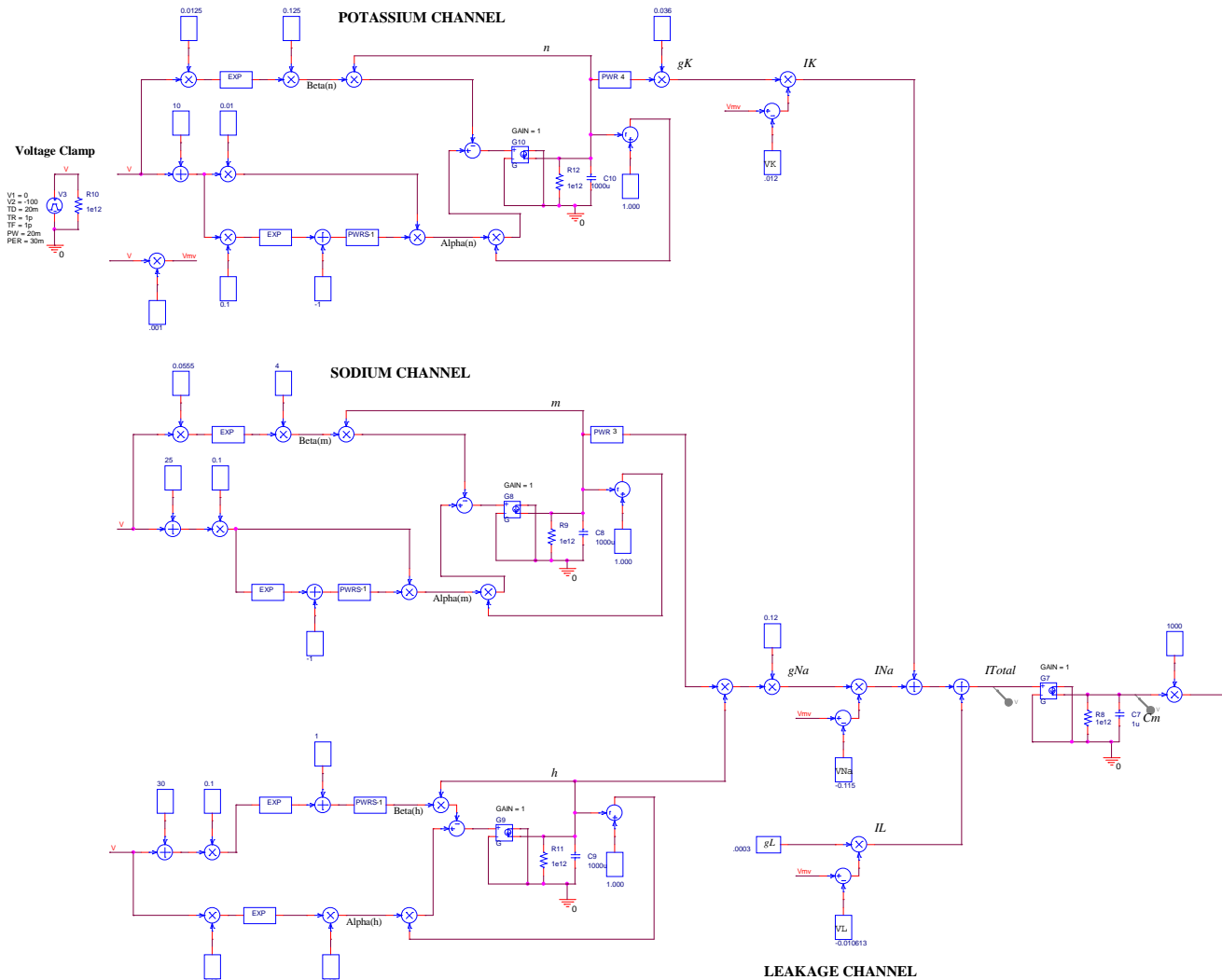
BI-DIRECTIONAL INTERFACING OF ELECTRONICS AND CULTURED NEURONS

- This is a collaborative programme involving E&EE at Bath, KCL/Guy's Hospital (London), Dept of EE at University College (London) and the Department of Physics at Queen Mary University (London)
- The overall aim is to enhance our understanding of how mammalian nerve cells can be connected optimally to integrated electronic circuitry for neurobiological research and medical applications
- We intend to find an alternative method to traditional *patch clamping* which is non-intrusive, less labour intensive in use and is based on a simple, cheap, reproducible CMOS integrated circuit without any need for elaborate post-processing

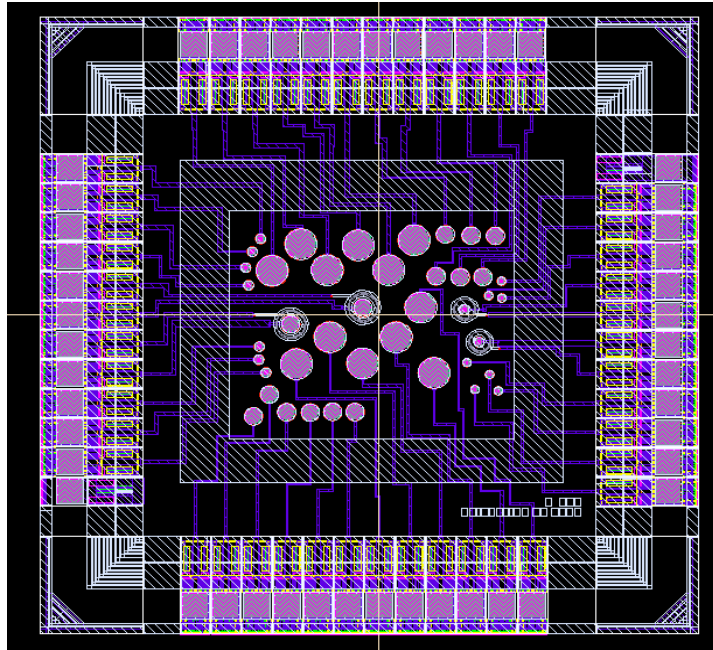
NEURON-ELECTRODE INTERFACE: EQUIVALENT CIRCUIT



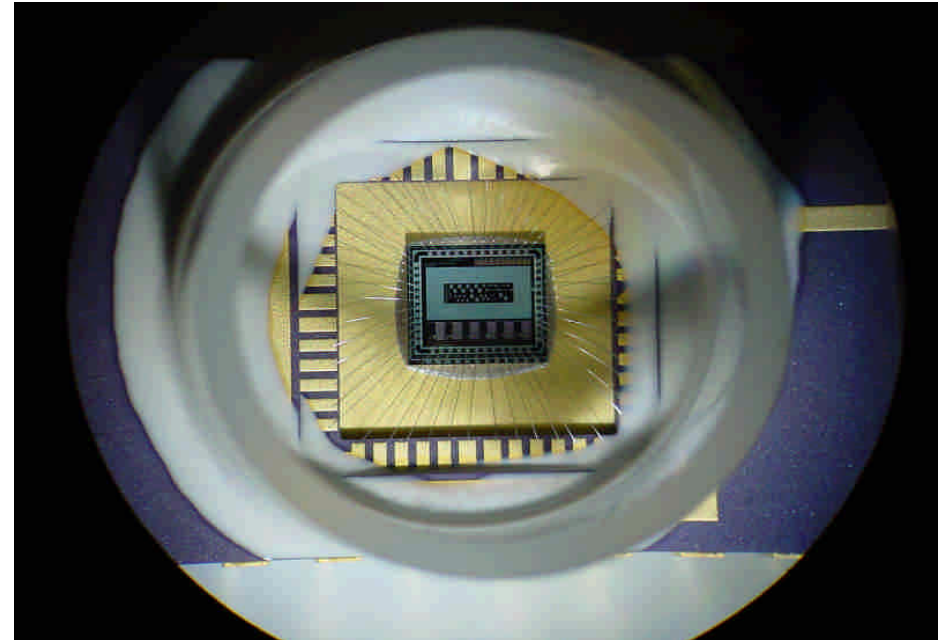
PSPICE REALISATION OF THE HODGKIN-HUXLEY MODEL OF A NEURON (1952)



PAD-ONLY CHIP LAYOUT

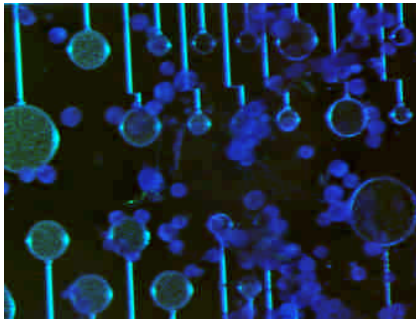


Chip layout



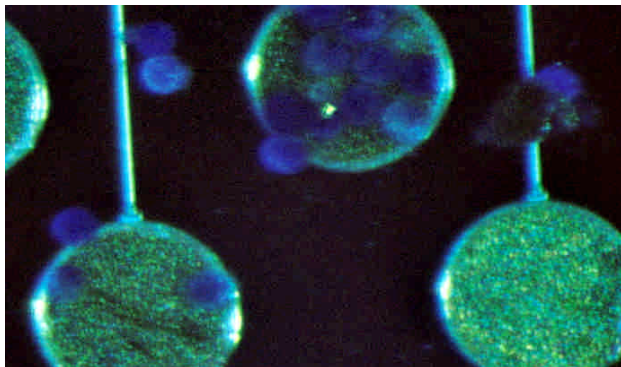
Packaged Die

GROWING NEURONAL CELLS ON CMOS



NG108-15 (neuroblastoma x glioma hybrid) cells, stained with methyl blue

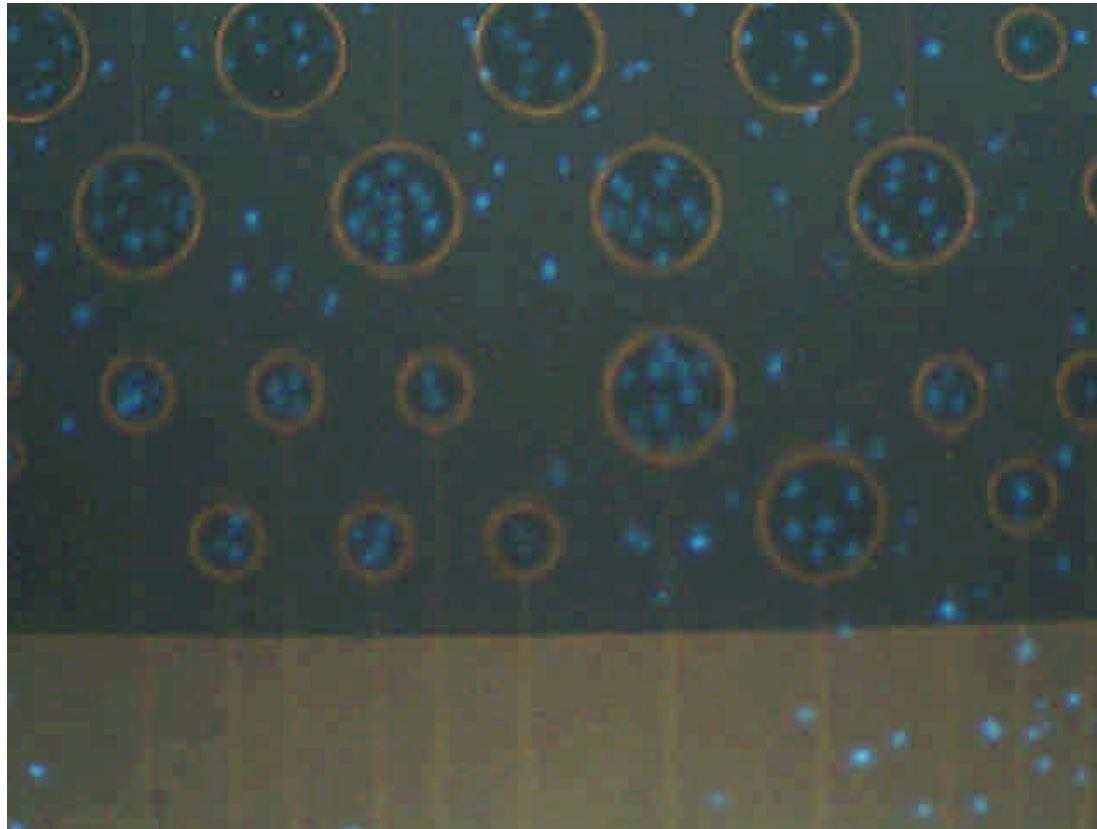
Grown on CMOS microchips pre-coated with a cationic polymer, (PE1), for 5 days



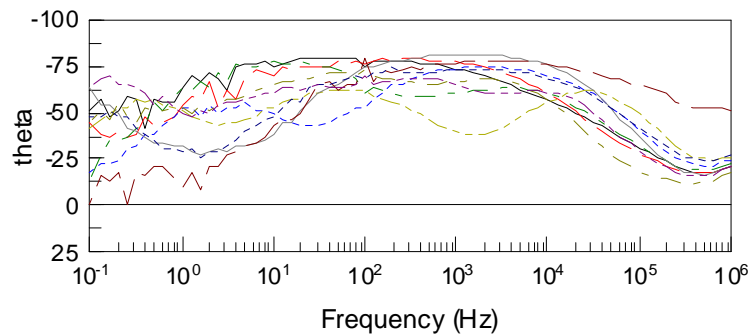
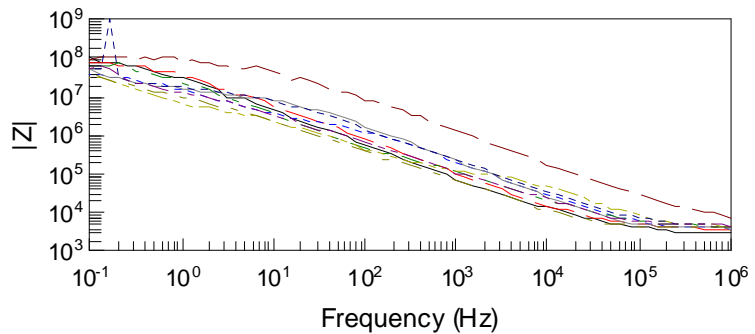
100µm

NEURONAL GROWTH ON POROUS SILICON

Etched from polysilicon on a CMOS chip

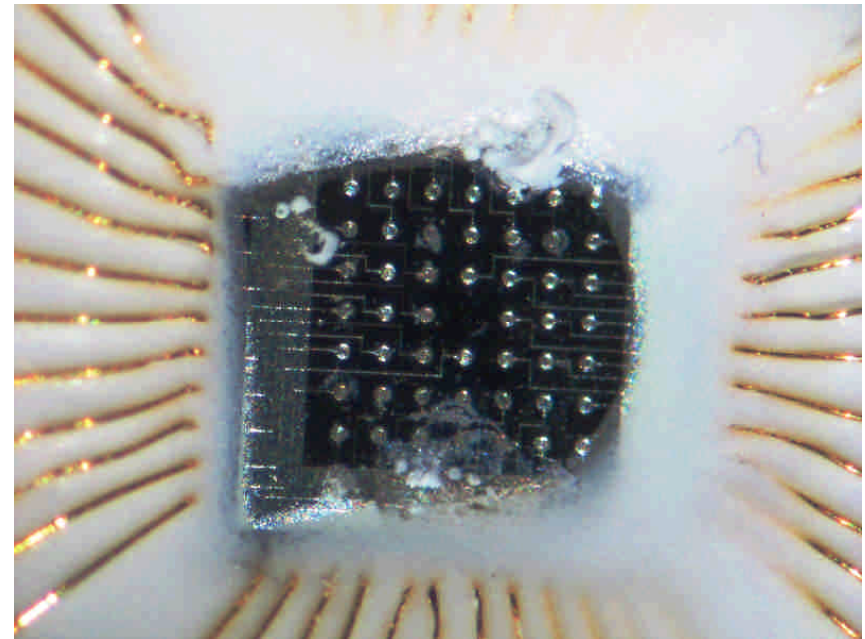


ELECTRICAL IMPEDANCE SPECTROSCOPY (EIS) MEASUREMENTS ON PACKAGED CMOS CHIPS



Averaged EIS
measurements

— pin1_chip1_31may06.z
— pin2_chip1_31may06.z
- - - pin3_chip1_31may06.z
- - - pin4_chip1_31may06.z



Packaged die with insulated bond wires

FUTURE WORK

- *Neural Prostheses*: (i) complete the demonstration of velocity selectivity (start January 2007) (ii) consider new methods of neural recording, e.g. using optoelectronics
- *Electro-neural Interfacing*: (i) Demonstrate capture of ENG from single excited neurons; design on-chip signal processing for optimum SNR. (ii) Complete modelling work
- *SMART Orthopaedic Sensors*: (i) Develop an optimal implanted sensor for hip micromotion detection and verify with *in-vitro* experiments. (ii) Develop other possible applications for the use of SMART sensors and actuators in modern orthopaedic applications

SYSTEM SPECIFICATION

Parameter	Specification	Measured
Number of channels	10	
Power supply	± 2.5 V	± 2.5 V
Power consumption	< 50 mW	24 mW
Circuit area		12 mm ²
Midband gain	10,000	10,100
Bandwidth	300 Hz, 3.5 kHz	310 Hz, 3.3 kHz
CMRR @ 1kHz	100 dB	82 dB
Input-referred voltage noise density 1 Hz, 1 kHz	20 nV/ $\sqrt{\text{Hz}}$, 4 nV/ $\sqrt{\text{Hz}}$	11.5 nV/ $\sqrt{\text{Hz}}$, 3.8 nV/ $\sqrt{\text{Hz}}$
Input-referred current noise density 1 Hz, 1 kHz	20 pA/ $\sqrt{\text{Hz}}$, 2 pA/ $\sqrt{\text{Hz}}$	17 nV/ $\sqrt{\text{Hz}}$, 1.5 nV/ $\sqrt{\text{Hz}}$
Input-referred rms voltage noise 1 Hz -5 kHz	< 300 nV	291 nV
Residual DC input current	< 100 nA	15 nA, 20 nA, +, - inputs