



**ED/CPMT Chapters of IEEE Orlando Section
AVS and IEEE Student Chapters of UCF**
Present guest lecture by

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ENG-III - 101

Germanium Transistors for the 22 nm Technology Node and Beyond

Abstract: As transistor scaling continues there is a need to boost the mobility of carriers far beyond the Si universal curves, so that drive current targets can be met whilst maintaining acceptable off-state leakage currents. A promising candidate to fulfill these requirements is Ge, which has bulk hole and electron mobilities approximately four and 2.5 times higher than Si respectively. The inclusion of strain allows mobility to be increased still further, and buried channel strained Ge pMOSFETs with hole mobility nine times higher than Si have been reported. In addition, it has already been demonstrated that Ge is compatible with a Si-like process flow.

In this presentation, the motivation for Ge transistors will be introduced, together with a brief overview of the current state of development of these devices. The electrical characteristics of deep submicron Ge pMOSFETs fabricated on Si wafers in a 200 mm pilot line will then be presented. These devices have a high-k/metal gate stack with peak hole mobilities in excess of $300 \text{ cm}^2/\text{Vs}$ and $I_{\text{ON}}/I_{\text{OFF}}$ ratios in excess of 10^4 , comparable to the best results reported in the literature. The hole mobility enhancement of more than twice the universal curve is maintained at vertical effective fields exceeding 1 MV/cm , which is the region of interest for heavily scaled transistors. Finally, the vision of IMEC's Ge III-V program for sub 45 nm device technology will be outlined. This proposal calls for Ge pMOS and III-V nMOS to be fabricated alongside one another on Si wafers. Ultra thin body Ge on insulator is foreseen to serve as the channel material for pMOSFETs, whilst also providing a platform for epitaxial growth of thin III-V layers for the nMOSFETs.

Bio: Gareth Nicholas was born in Bristol, U.K. in 1980. He received the B.Sc. and Ph.D. degrees in Physics from the University of Warwick, U.K., in 2001 and 2005 respectively. His research at Warwick focused on the use of biaxial strained Si and SiGe in the channel region of deep submicron MOSFETs, including investigations of carrier injection velocity and self-heating. In 2006 he joined IMEC, Belgium, where he is working on short channel Ge pMOSFETs and techniques for increasing carrier mobilities in Ge. He has authored or co-authored 15 papers and presentations.

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