Heterogeneous Processors: The Cell Broadband Engine (plus processor history & outlook)

IEEE SSC/CAS Joint Chapter, Jan. 18, 2011

H. Peter Hofstee

IBM Austin Research Laboratory
CMOS Microprocessor Trends, The First ~25 Years (Good old days)

- Single Thread
  - More active transistors, higher frequency
  - 2005
SPECINT


**VAX**: 25%/year 1978 to 1986

**RISC + x86**: 52%/year 1986 to 2002

25%/year

52%/year

??%/year

3X
1971 – 2000, A Comparison

<table>
<thead>
<tr>
<th>Feature</th>
<th>1971 (Intel 4004)</th>
<th>2000 (Intel Pentium III Xeon)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>10 micron (PMOS)</td>
<td>180 nm (CMOS)</td>
</tr>
<tr>
<td>Voltage</td>
<td>15V</td>
<td>1.7V (0.27V)</td>
</tr>
<tr>
<td>#Transistors</td>
<td>2,312</td>
<td>28M (69M)</td>
</tr>
<tr>
<td>Frequency</td>
<td>740KHz</td>
<td>600MHz – 1GHz (41MHz)</td>
</tr>
<tr>
<td>Cycles per Inst.</td>
<td>8</td>
<td>~1</td>
</tr>
<tr>
<td>Chip size</td>
<td>11mm2</td>
<td>106mm2</td>
</tr>
<tr>
<td>Power</td>
<td>0.45W</td>
<td>20.4 W (<a href="mailto:0.6GHz@1.7V">0.6GHz@1.7V</a>)</td>
</tr>
<tr>
<td>Power density</td>
<td>0.04W/mm2</td>
<td>0.18W/mm</td>
</tr>
<tr>
<td>Inst/(Hz * #tr)</td>
<td>5.4 E-5</td>
<td>3.6 E-8</td>
</tr>
</tbody>
</table>
~2004: CMOS Devices hit a scaling wall

Isaac e.a.  IBM
Microprocessor Trends

More active transistors, higher frequency

Single Thread

More active transistors, higher frequency

2005

Log(Performance)
Microprocessor Trends

Log(Performance)

Multi-Core
More active transistors, higher frequency

Single Thread
More active transistors, higher frequency

2005  2015(?)
Multicore Power Server Processors

Power 4  
2001  
Introduces Dual core

Power 5  
2004  
Dual Core – 4 threads

Power 7  
2009  
8 cores – 32 threads
POWER7 Processor Chip: Threads & SIMD

- **Physical Design:**
  - 567mm² Technology: 45nm lithography, Cu, SOI, eDRAM
  - 1.2B transistors
    - Equivalent function of 2.7B
eDRAM efficiency

- **Features:**
  - Eight processor cores
    - 12 execution units per core
    - 4 Way SMT per core
    - 32 Threads per chip
    - 256KB L2 per core
  - 32MB on chip eDRAM shared L3
  - Dual DDR3 Memory Controllers
    - 100GB/s Memory bandwidth per chip sustained
  - Scalability up to 32 Sockets
    - 360GB/s SMP bandwidth/chip
    - 20,000 coherent operations in flight

- Two I/O Mezzanine (GX++) System Buses
- Binary Compatibility with POWER6

- VSX Floating-Point / Media Units
POWER7 IH Memory DIMM

- Up to 128 DIMMs per Node
- 8 GB and 16 GB DIMMs
- Dual Super Novas per DIMM
- Water Cooled
Why are (shared memory) CMPs dominant?

- A new system delivers nearly twice the throughput performance of the previous one without application-level changes.

- Applications do not degrade in performance when ported (to a next-generation processor).
  - This is an important factor in markets where it is not possible to rewrite all applications for a new system, a common case.

- Applications benefit from more memory capacity and more memory bandwidth when ported.
  - .. even if they do not (optimally) use all the available cores.

- Even when a single application must be accelerated, large portions of code can be reused.

- Design cost is reduced, at least relative to the scenario where all available transistors are used to build a single processor.
PDSOI optimization results

Optimizing for maximum performance for each core

Constant power density 25 W/cm²

Constant performance improvement, 20% per gen.

D. Frank, C. Tyberg
Microprocessor Trends

Log(Performance)

More active transistors, higher frequency
Multi-Core

More active transistors, higher frequency
Single Thread

More active transistors, higher frequency
2005 2015(?)
What are the options? What are we doing about it?

- Just live with it: accept slowdown
  - Use added transistors for bigger caches

- Lighter weight threads only
  - More parallel = more efficient

- Mix strong and light-weight cores
  - More parallel = more efficient

- Add accelerators
  - More specialized = more efficient
Microprocessor Trends

- Hybrid/Heterogeneous
  - More active transistors, higher frequency

- Multi-Core
  - More active transistors, higher frequency

- Single Thread
  - More active transistors, higher frequency
  - 2005  2015(?)  2025(??)
Heterogeneous Power Architecture Processors

- Xilinx Virtex II-Pro 2002
  1-2 Power Cores
  + FPGA

- Cell Broadband Engine 2005
  1 Power Core
  + 8 accelerator cores

- Rapport Kilocore 2006
  1 Power Core
  + 256 accelerator cores
What Options do we Have? --LEVERAGING LOCALITY

- Ignoring locality is unbelievably wasteful
  - E.g. cache generally follows Pollack’s rule sqrt(x) return on x investment

- Ample proof that enhancing locality can improve both efficiency and performance (dramatically)
  - PGAS / thread local vs global (Increasingly serious alternative to MPI)
  - Vector/GPU (HPC, TPC-H ..)
  - Cell local store / tasks (sorting, searching, mapreduce …)
  - Function placement (Haifa TCP-IP stack example)

- Where we have failed thus far:
  - Non-standard languages – rewrite required
  - Non-incremental changes to HW – big benefit but limited reach
Cell Broadband Engine

- **Heterogeneous Multiprocessor**
  - Power processor
  - Synergistic Processing Elements

- **Power Processor Element (PPE)**
  - general purpose
  - running full-fledged OSs
  - 2 levels of globally coherent cache

- **Synergistic Proc. Element (SPE)**
  - SPU optimized for computation density
  - 128 bit wide SIMD
  - Fast local memory
  - Globally coherent DMA
Memory Managing Processor vs. Traditional General Purpose Processor

Cell
BE

IBM

AMD

Intel
Three Generations of Cell/B.E.

<table>
<thead>
<tr>
<th>Generation</th>
<th>W (mm)</th>
<th>H (mm)</th>
<th>Area (mm²)</th>
<th>Scaling from 90nm</th>
<th>Scaling from 65nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>90nm</td>
<td>19.17</td>
<td>12.29</td>
<td>235.48</td>
<td>100.0%</td>
<td></td>
</tr>
<tr>
<td>65nm</td>
<td>15.59</td>
<td>11.20</td>
<td>174.61</td>
<td>74.2%</td>
<td>100.0%</td>
</tr>
<tr>
<td>45nm</td>
<td>12.75</td>
<td>9.06</td>
<td>115.46</td>
<td>49.0%</td>
<td>66.1%</td>
</tr>
</tbody>
</table>

Synergistic Processor Element (SPE)

<table>
<thead>
<tr>
<th>Generation</th>
<th>W (mm)</th>
<th>H (mm)</th>
<th>Area (mm²)</th>
<th>Scaling from 90nm</th>
<th>Scaling from 65nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>90nm</td>
<td>2.54</td>
<td>5.81</td>
<td>14.76</td>
<td>100.0%</td>
<td></td>
</tr>
<tr>
<td>65nm</td>
<td>2.09</td>
<td>5.30</td>
<td>11.08</td>
<td>75.0%</td>
<td>100.0%</td>
</tr>
<tr>
<td>45nm</td>
<td>1.59</td>
<td>4.09</td>
<td>6.47</td>
<td>43.9%</td>
<td>58.5%</td>
</tr>
</tbody>
</table>

Power Processor Element (PPE)

<table>
<thead>
<tr>
<th>Generation</th>
<th>W (mm)</th>
<th>H (mm)</th>
<th>Area (mm²)</th>
<th>Scaling from 90nm</th>
<th>Scaling from 65nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>90nm</td>
<td>4.44</td>
<td>6.05</td>
<td>26.86</td>
<td>100.0%</td>
<td></td>
</tr>
<tr>
<td>65nm</td>
<td>3.50</td>
<td>5.60</td>
<td>19.60</td>
<td>73.0%</td>
<td>100.0%</td>
</tr>
<tr>
<td>45nm</td>
<td>2.66</td>
<td>4.26</td>
<td>11.32</td>
<td>42.1%</td>
<td>57.7%</td>
</tr>
</tbody>
</table>

Takahashi e.a.
Cell Broadband Engine-based CE Products

Sony Playstation 3 and PS3

Toshiba Regza Cell
Image Processing on the Cell Broadband Engine

Toshiba Magic Mirror

Sony PlayStation®Move

Mayo Clinic/IBM

Mercury Computer

Hitachi Medical

Axion Racing
Uses of Cell Technology beyond Consumer Electronics

- Three Generations of Server Blades Accompanied By 3 SDK Releases
  - IBM QS20
  - IBM QS21
  - IBM QS22

- Two Generations of PCIe Cell Accelerator Boards
  - CAB (Mercury)
  - PX-CAB (Mercury/Fixstars/Matrix Vision)

- 1U Formfactor
  - Mercury Computer
  - TPlatforms

- Custom Boards
  - Hitachi Medical (Ultrasound)
  - Other Medical and Defense

- World’s First 1 PFlop Computer
  - LANL Roadrunner

- Top 7 Green Systems
  - Green 500 list
Optimization of Sparse Matrix-Vector Multiplication on Emerging Multicore Platforms

Samuel Williams, Leonid Oliker, Richard Vuduc, John Shalf, Katherine Yelick, James Demmel

*CRD/NERSC, Lawrence Berkeley National Laboratory, Berkeley, CA 94720, USA
†Computer Science Division, University of California at Berkeley, Berkeley, CA 94720, USA
‡CASC, Lawrence Livermore National Laboratory, Livermore, CA 94551, USA

Figure 5: Architectural comparison of the median matrix performance showing (a) GFlop/s rates of OSKI and optimized SpMV on single-core, full socket, and full system and (b) relative power efficiency computed as total full system Mflop/s divided by sustained full system Watts (see Table 1).
Current Cell: Integer Workloads

Breadth-First Search
Villa, Scarpazza, Petrini, Peinador
IPDPS 2007

Mapreduce
Sangkaralingam, De Kruijf, Oct. 2007

<table>
<thead>
<tr>
<th>Application Name</th>
<th>Application Type</th>
<th>Lines of Code</th>
<th>Speedup vs. Core2</th>
<th>BIPS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>histogram</td>
<td>partition-dominated</td>
<td>345</td>
<td>216</td>
<td>1.06</td>
</tr>
<tr>
<td>kmeans</td>
<td>partition-dominated</td>
<td>324</td>
<td>318</td>
<td>0.91</td>
</tr>
<tr>
<td>linearRegression</td>
<td>map-dominated</td>
<td>279</td>
<td>114</td>
<td>0.34</td>
</tr>
<tr>
<td>wordCount</td>
<td>partition-dominated</td>
<td>226</td>
<td>324</td>
<td>0.87</td>
</tr>
<tr>
<td>NAS_EP</td>
<td>map-dominated</td>
<td>264</td>
<td>112</td>
<td>1.08</td>
</tr>
<tr>
<td>distributedSort</td>
<td>sort-dominated</td>
<td>171</td>
<td>93</td>
<td>0.41</td>
</tr>
</tbody>
</table>

D.A. Bader et al. / Parallel Computing 33 (2007) 720–740

a Comparison of List ranking on Cell with other Single Processors
for list of size 8 million nodes

Sort: Gedik, Bordawekar, Yu (IBM)
Table 3: Out-of-core sort performance (in secs)

<table>
<thead>
<tr>
<th># items</th>
<th>16 SPEs</th>
<th>3.2GHz Xeon quick</th>
<th>3.2GHz Xeon 2-core quick</th>
<th>PPE quick</th>
</tr>
</thead>
<tbody>
<tr>
<td>1M</td>
<td>0.0098</td>
<td>0.1813</td>
<td>0.098589</td>
<td>0.4333</td>
</tr>
<tr>
<td>2M</td>
<td>0.0234</td>
<td>0.3794</td>
<td>0.205728</td>
<td>0.9072</td>
</tr>
<tr>
<td>4M</td>
<td>0.0569</td>
<td>0.7941</td>
<td>0.429499</td>
<td>1.9574</td>
</tr>
<tr>
<td>8M</td>
<td>0.1372</td>
<td>1.6704</td>
<td>0.895188</td>
<td>4.0746</td>
</tr>
<tr>
<td>16M</td>
<td>0.3172</td>
<td>3.4673</td>
<td>1.863354</td>
<td>8.4577</td>
</tr>
<tr>
<td>32M</td>
<td>0.7461</td>
<td>7.1751</td>
<td>3.863495</td>
<td>18.3882</td>
</tr>
<tr>
<td>64M</td>
<td>1.7703</td>
<td>14.8731</td>
<td>7.946356</td>
<td>38.7473</td>
</tr>
<tr>
<td>128M</td>
<td>4.0991</td>
<td>30.0481</td>
<td>16.165378</td>
<td>79.9971</td>
</tr>
</tbody>
</table>
Playstation 3 high-level organization and PS3 cluster.
Roadrunner accelerated node and system.

Roadrunner Accelerated Node
QPACE PowerXCell8i node card and system.

QPACE node card.
### June 2010 Green500

<table>
<thead>
<tr>
<th>Green500 Rank</th>
<th>MFLOPS/W</th>
<th>Site*</th>
<th>Computer*</th>
<th>Total Power (kW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>773.38</td>
<td>Forschungszentrum Juelich (FZJ)</td>
<td>QPACE SFB TR Cluster, PowerXCell 8i, 3.2 GHz, 3D-Torus</td>
<td>57.54</td>
</tr>
<tr>
<td>1</td>
<td>773.38</td>
<td>Universitaet Regensburg</td>
<td>QPACE SFB TR Cluster, PowerXCell 8i, 3.2 GHz, 3D-Torus</td>
<td>57.54</td>
</tr>
<tr>
<td>1</td>
<td>773.38</td>
<td>Universitaet Wuppertal</td>
<td>QPACE SFB TR Cluster, PowerXCell 8i, 3.2 GHz, 3D-Torus</td>
<td>57.54</td>
</tr>
<tr>
<td>4</td>
<td>492.64</td>
<td>National Supercomputing Centre in Shenzhen (NSCS)</td>
<td>Dawning Nebulae, TC3600 blade CB60-G2 cluster, Intel Xeon 5550/ nvidia C2050, Infiniband</td>
<td>2580</td>
</tr>
<tr>
<td>5</td>
<td>458.33</td>
<td>DOE/NNSA/LANL</td>
<td>BladeCenter QS22/LS21 Cluster, PowerXCell 8i 3.2 GHz / Opteron DC 1.8 GHz, Infiniband</td>
<td>276</td>
</tr>
<tr>
<td>5</td>
<td>458.33</td>
<td>IBM Poughkeepsie Benchmarking Center</td>
<td>BladeCenter QS22/LS21 Cluster, PowerXCell 8i 3.2 Ghz / Opteron DC 1.8 GHz, Infiniband</td>
<td>138</td>
</tr>
<tr>
<td>7</td>
<td>444.25</td>
<td>DOE/NNSA/LANL</td>
<td>BladeCenter QS22/LS21 Cluster, PowerXCell 8i 3.2 Ghz / Opteron DC 1.8 GHz, Voltaire infiniband</td>
<td>2345.5</td>
</tr>
<tr>
<td>8</td>
<td>431.88</td>
<td>Institute of Process Engineering, Chinese Academy of Sciences</td>
<td>Mole-8.5 Cluster Xeon L5520 2.26 Ghz, nVidia Tesla, Infiniband</td>
<td>480</td>
</tr>
<tr>
<td>9</td>
<td>418.47</td>
<td>Mississippi State University</td>
<td>iDataPlex, Xeon X56xx 6C 2.8 GHz, Infiniband</td>
<td>72</td>
</tr>
<tr>
<td>10</td>
<td>397.56</td>
<td>Banking (M)</td>
<td>iDataPlex, Xeon X56xx 6C 2.66 GHz, Infiniband</td>
<td>72</td>
</tr>
</tbody>
</table>

* Performance data obtained from publicly available sources including [TOP500](http://www.top500.org/).
<table>
<thead>
<tr>
<th>Green500 Rank</th>
<th>MFLOPS/W</th>
<th>Site*</th>
<th>Computer*</th>
<th>Total Power (kW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1684.20</td>
<td>IBM Thomas J. Watson Research Center</td>
<td>NNSA/SC Blue Gene/Q, Prototype</td>
<td>38.80</td>
</tr>
<tr>
<td>2</td>
<td>958.35</td>
<td>GSIC Center, Tokyo Institute of Technology</td>
<td>HP ProLiant SL390s G7 Xeon 6C X5670, Nvidia GPU, Linux/Windows</td>
<td>1243.80</td>
</tr>
<tr>
<td>3</td>
<td>933.06</td>
<td>NCSA</td>
<td>Hybrid Cluster Core i3 2.93Ghz Dual Core, NVIDIA C2050, Infiniband</td>
<td>36.00</td>
</tr>
<tr>
<td>4</td>
<td>828.67</td>
<td>RIKEN Advanced Institute for Computational Science</td>
<td>K computer, SPARC64 VIIIfx 2.0GHz, Tofu interconnect</td>
<td>57.96</td>
</tr>
<tr>
<td>5</td>
<td>773.38</td>
<td>Forschungszentrum Juelich (FZJ)</td>
<td>QPACE SFB TR Cluster, PowerXCell 8i, 3.2 GHz, 3D-Torus</td>
<td>57.54</td>
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<td>773.38</td>
<td>Universitaet Wuppertal</td>
<td>QPACE SFB TR Cluster, PowerXCell 8i, 3.2 GHz, 3D-Torus</td>
<td>57.54</td>
</tr>
<tr>
<td>8</td>
<td>740.78</td>
<td>Universitaet Frankfurt</td>
<td>Supermicro Cluster, QC Opteron 2.1 GHz, ATI Radeon GPU, Infiniband</td>
<td>385.00</td>
</tr>
<tr>
<td>9</td>
<td>677.12</td>
<td>Georgia Institute of Technology</td>
<td>HP ProLiant SL390s G7 Xeon 6C X5660 2.8Ghz, nVidia Fermi, Infiniband QDR</td>
<td>94.40</td>
</tr>
<tr>
<td>10</td>
<td>636.36</td>
<td>National Institute for Environmental Studies</td>
<td>GOSAT Research Computation Facility, nvidia</td>
<td>117.15</td>
</tr>
</tbody>
</table>

* Performance data obtained from publicly available sources including TOP500
Blue Gene/Q

1. Chip:
   16 μP cores

2. Single Chip Module

3. Compute card:
   One chip module,
   16 GB DDR3 Memory,

4. Node Card:
   32 Compute Cards,
   Optical Modules, Link Chips, Torus

5a. Midplane:
   16 Node Cards

5b. IO drawer:
   8 IO cards w/16 GB
   8 PCIe Gen2 x8 slots

6. Rack: 2 Midplanes

7. System:
   20PF/s

• Sustained single node perf: 10x P, 20x L
• MF/Watt: (6x) P, (10x) L (~2GF/W target)
Performance and Productivity Challenges require a Multi-Dimensional Approach

Highly Productive Systems

Highly Scalable Multi-core Systems

Hybrid Systems

Comprehensive (Holistic) System Innovation & Optimization
HPC Cluster Directions

ExaF

Performance

Targeted Configurability

Roadrunner

BG/P

BG/Q

PERCS Systems

ExaScale

Accelerators

Accelerators

Extended Configurability

Accelerators

2007

2008

2009/2010

2011

2012

2013

2018-19

Linux Clusters  Power, x86-64, Less Demanding Communication

Power, AIX/ Linux

Capacity Clusters

Capability Machines
## Top 500, Nov 2010

<table>
<thead>
<tr>
<th>Site</th>
<th>Computer</th>
</tr>
</thead>
<tbody>
<tr>
<td>National Supercomputing Center in Tianjin</td>
<td>Tianhe-1A - NUDT TH MPP, X5670 2.93Ghz 6C, NVIDIA GPU, FT-1000 8C</td>
</tr>
<tr>
<td>China</td>
<td>NUDT</td>
</tr>
<tr>
<td>DOE/SC/Oak Ridge National Laboratory</td>
<td>Jaguar - Cray XT5-HE Opteron 6-core 2.6 GHz</td>
</tr>
<tr>
<td>United States</td>
<td>Cray Inc.</td>
</tr>
<tr>
<td>National Supercomputing Centre in Shenzhen (NSCS)</td>
<td>Nebulae - Dawning TC3600 Blade, Intel X5650, NVidia Tesla C2050 GPU</td>
</tr>
<tr>
<td>China</td>
<td>Dawning</td>
</tr>
<tr>
<td>GSIC Center, Tokyo Institute of Technology</td>
<td>TSUBAME 2.0 - HP ProLiant SL390s G7 Xeon 6C X5670, Nvidia GPU, Linux/Windows</td>
</tr>
<tr>
<td>Japan</td>
<td>NEC/HP</td>
</tr>
<tr>
<td>DOE/SC/LBNL/NERSC</td>
<td>Hopper - Cray XE6 12-core 2.1 GHz</td>
</tr>
<tr>
<td>United States</td>
<td>Cray Inc.</td>
</tr>
<tr>
<td>Commissariat a l'Energie Atomique (CEA)</td>
<td>Tera-100 - Bull bullx super-node S6010/S6030</td>
</tr>
<tr>
<td>France</td>
<td>Bull SA</td>
</tr>
<tr>
<td>DOE/NNSA/LANL</td>
<td>Roadrunner - BladeCenter QS22/LS21 Cluster, PowerXCell 8i 3.2 Ghz</td>
</tr>
<tr>
<td>United States</td>
<td>/ Opteron DC 1.8 Ghz, Voltaire Infiniband</td>
</tr>
<tr>
<td>National Institute for Computational Sciences/University of Tennessee</td>
<td>Kraken XT5 - Cray XT5-HE Opteron 6-core 2.6 GHz</td>
</tr>
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<td>United States</td>
<td>Cray Inc.</td>
</tr>
<tr>
<td>Forschungszentrum Juelich (FZJ)</td>
<td>JUGENE - Blue Gene/P Solution</td>
</tr>
<tr>
<td>Germany</td>
<td>IBM</td>
</tr>
<tr>
<td>DOE/NNSA/LANL/SNL</td>
<td>Cielo - Cray XE6 8-core 2.4 GHz</td>
</tr>
<tr>
<td>United States</td>
<td>Cray Inc.</td>
</tr>
</tbody>
</table>
Next Era of Innovation – Hybrid Computing

Symmetric Multiprocessing Era

- p6
- Cell
- BlueGene

Driven by cores/threads

Technology Out

Hybrid Computing Era

- p7
- Throughput
- Computational

Driven by workload consolidation

Market In

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Converging Software ( Much Harder! )

- Software-Hardware Efficiency Driven by
  - Number of operations (we all learn this in school)
  - Degree of thread parallelism
  - Degree of data parallelism
  - Degree of locality (code and data, data more important)
  - Degree of predictability (code and data, data more important)

- Need a new Portable Framework
  - Allow portable format to retain enough information for run-time optimization.
  - Allow run-time optimization to heterogeneous hardware for each of the parameters above.
OpenCL vs CUDA ecosystem
Two Standards for Programming the Node

- Two standards evolving from different sides of the market

Concurrent and Locality
Hybrid Parallel Gas Dynamics in OpenCL

Los Alamos Booth (715) Configuration:
- IBM BladeCenter Q322 Blade (PowerXCell)
- IBM BladeCenter JS43 Blade (PowerXCell)
- IBM QS22 Blade (PowerXCell)
- IBM HS22 Blade (Xeon)
- IBM LS22 Blade (Opteron)
- NVIDIA GPU

IBM Booth (1335) Configuration:
- IBM System x3755
- NVIDIA GPU
- Lenovo ThinkStation D10

Hybrid Parallel Gas Dynamics Code:
- http://sourceforge.net/projects/hypgad/
- IBM’s OpenCL Development Kit for Linux on Power:
- ATI’s Stream Software Development Kit:
- NVIDIA’s OpenCL for NVIDIA’s CUDA Architecture GPUs:
- Kxanomos OpenCL:
- http://www.kxanomos.org/opencl/
Finite difference, linear, hyperbolic, inhomogeneous PDE
EMRI Teukolsky

Cell Broadband Engine

![Bar Chart]

- **Performance Factor**

- **X-axis Categories**:
  - PPE
  - OpenCL (Source)
  - OpenCL (Binary)
  - Cell SDK

The chart shows the performance factor for different platforms and libraries.
Figure 3. Overall performance of the EMRI Teukolsky Code accelerated by the Tesla CUDA GPU using OpenCL. The baseline here is the supporting system’s CPU — an AMD Phenom 2.5 GHz processor.
Figure 4. Relative performance of the OpenCL-based EMRI Teukolsky Code on all discussed architectures – CPU, CBE and GPU. The baseline here is the system CPU – an AMD Phenom 2.5 GHz processor.
Microprocessor Trends

- More active transistors, higher frequency
- Hybrid
- Multi-Core
- Single Thread

2005  2015(?)  2025(??)  2035(???)
Microprocessor Trends

- **Special Purpose (ASIC)**: More active transistors, higher frequency
- **Hybrid**: More active transistors, higher frequency
- **Multi-Core**: More active transistors, higher frequency
- **Single Thread**: More active transistors, higher frequency

Years:
- 2005
- 2015(?)
- 2025(??)
- 2035(???)
Microprocessor Trends

- **Single Thread**
  - More active transistors, higher frequency
  - 2005

- **Multi-Core**
  - More active transistors, higher frequency
  - 2015(?)

- **Hybrid**
  - More active transistors, higher frequency

- **Special Purpose (ASIC)**
  - More active transistors, higher frequency

- **Reconfigurable Hybrid / FPGAs?**

The trend lines project possible advancements in performance over time, with conjectures for years 2015, 2025, and 2035.
Five Decades of Innovations (Beyond Scaling)

1960s - 1970s
- S/360 Model 67: first virtualized machine
- Thermal convection cooling technology
- S/360 Model 67: first virtualized machine

1980s
- VM virtualization
- CMOS processors
- Modular refrigeration cooling technology
- High-k metal gates
- IBM Energy Efficiency Institute, Austin, TX

mid-1990s
- Airgap

late-1990s
- Cell BE processor
- Copper chip
- 3D chip stacking
- eDRAM

2000s
- Power6

Airgap

2000s
- Power6

Airgap
Summary

- **Technology limits drive fundamental change:**
  - First multi-core, then hybrid and eventually special-purpose again?
  - Cell an early example of hybrid

- **What is next:**
  - Continued Focus on Efficiency
    - Technology developments require it
  - Increasing Focus on Ease of Use
    - Focus on efficiency fundamentals in code
    - Make accelerators “invisible” for most customers
    - Commercial and CE applications, not just HPC
    - Not an easy thing to do
  - Increasing Focus on Standards-Based Programming
    - OpenMP & OpenCL
    - ...
  - Continue to Broaden Application Reach for Hybrid Systems
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