Bridging Design and Manufacture of Analog/Mixed-Signal (AMS) Circuits in Advanced CMOS

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Synopsys

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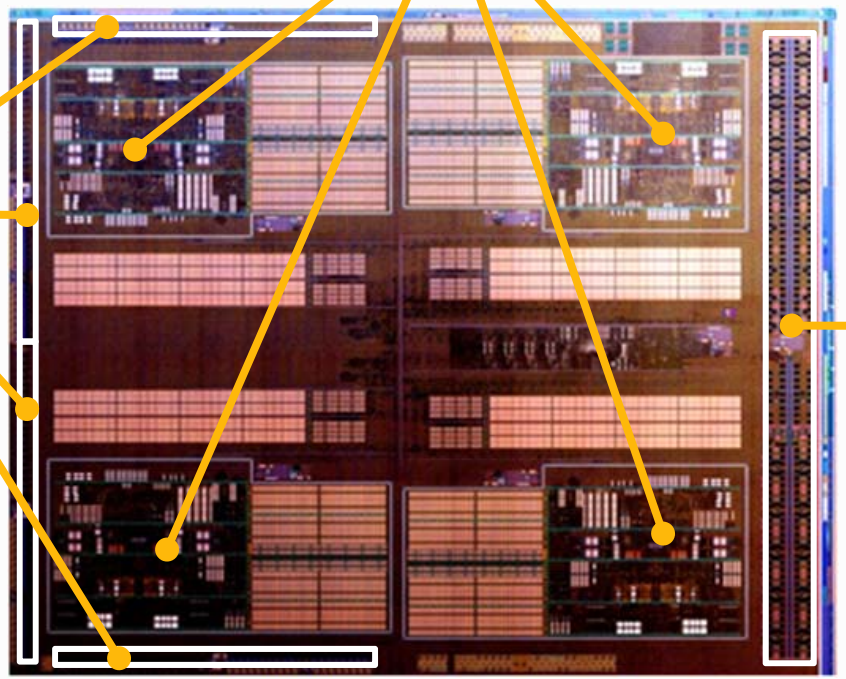
AMS is Essential in Processors

Core PLL Clocks (voltage/frequency islands)
Regulators & Thermal Sensors

HT3+ I/Os
PLL Clocks
Regulators



DDR3 I/O
PLL Clock

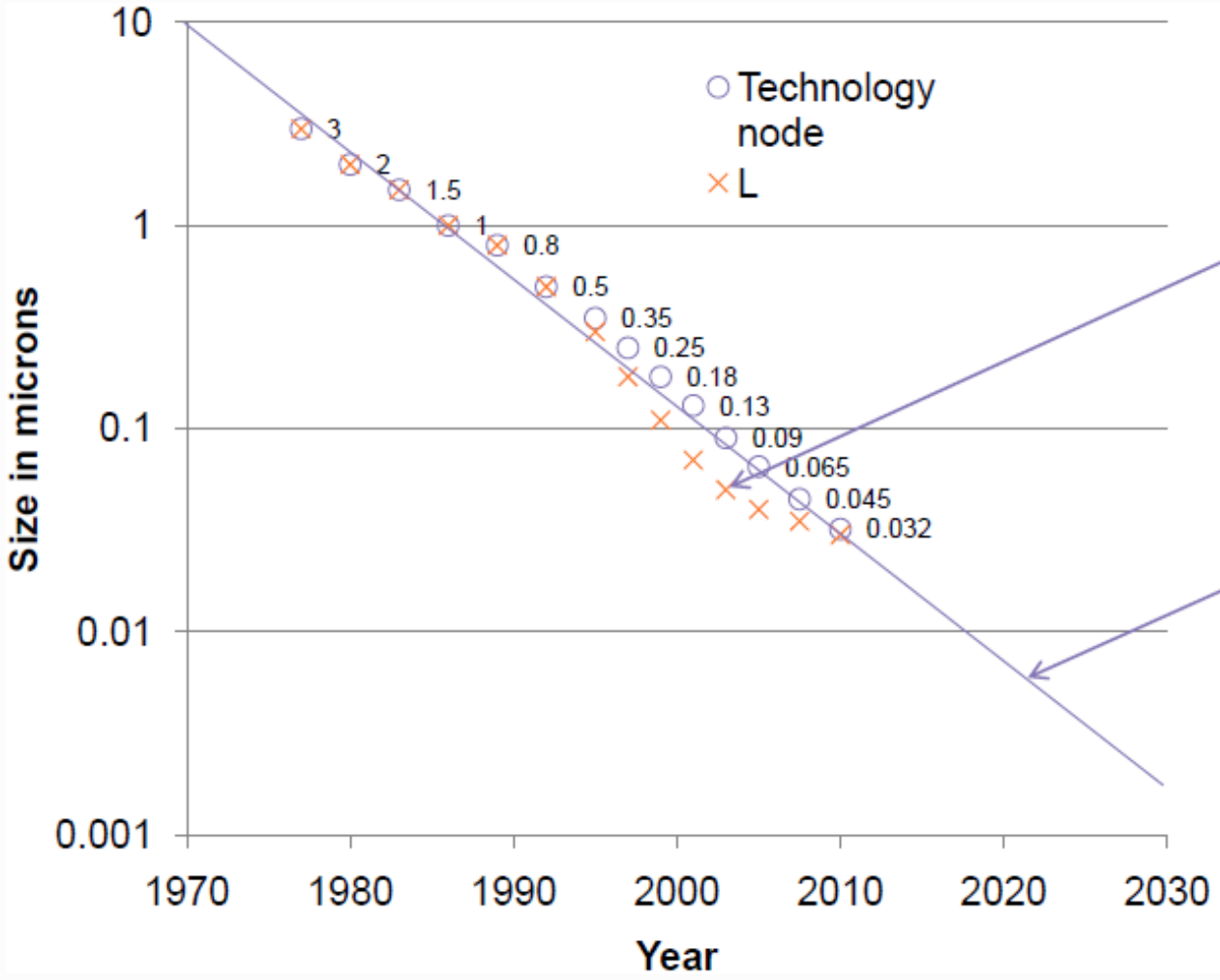
32nm SOI-CMOS “Orochi” server processor with Bulldozer cores

Fischer *et al.*, Ref. [1]

Outline

- Background & Motivation
- Device-Level Characterization
- Circuit-Level Characterization
- Circuit Simulator Developments
- Conclusions

CMOS Scaling Driven by Logic Needs

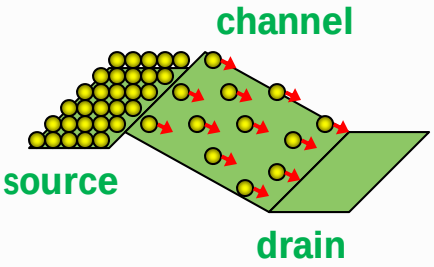


Channel length L had accelerated scaling for a while, but now is back in line with the node

Transistor density doubles every 2.5 years

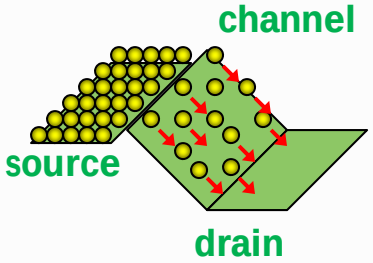
Keating, Ref. [2]

The Roads to Higher Performance



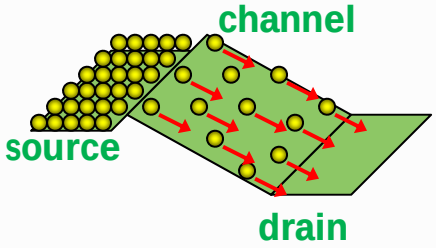
$$t_{delay} \approx \frac{C_{load}\,\Delta V}{I_{FET}}$$

Decrease L – steepen the hill



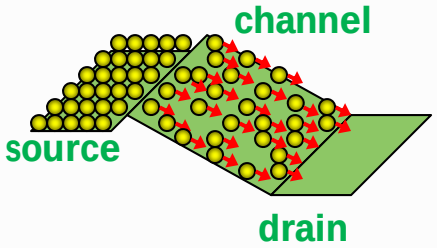
lithography
scaling

Increase μ – move carriers faster



strain engineering
faster materials

Increase C_{ox} – move more carriers



high-K dielectric
metal gate

- Doing it all without parasitic R & C undoing all the I_{FET} gains

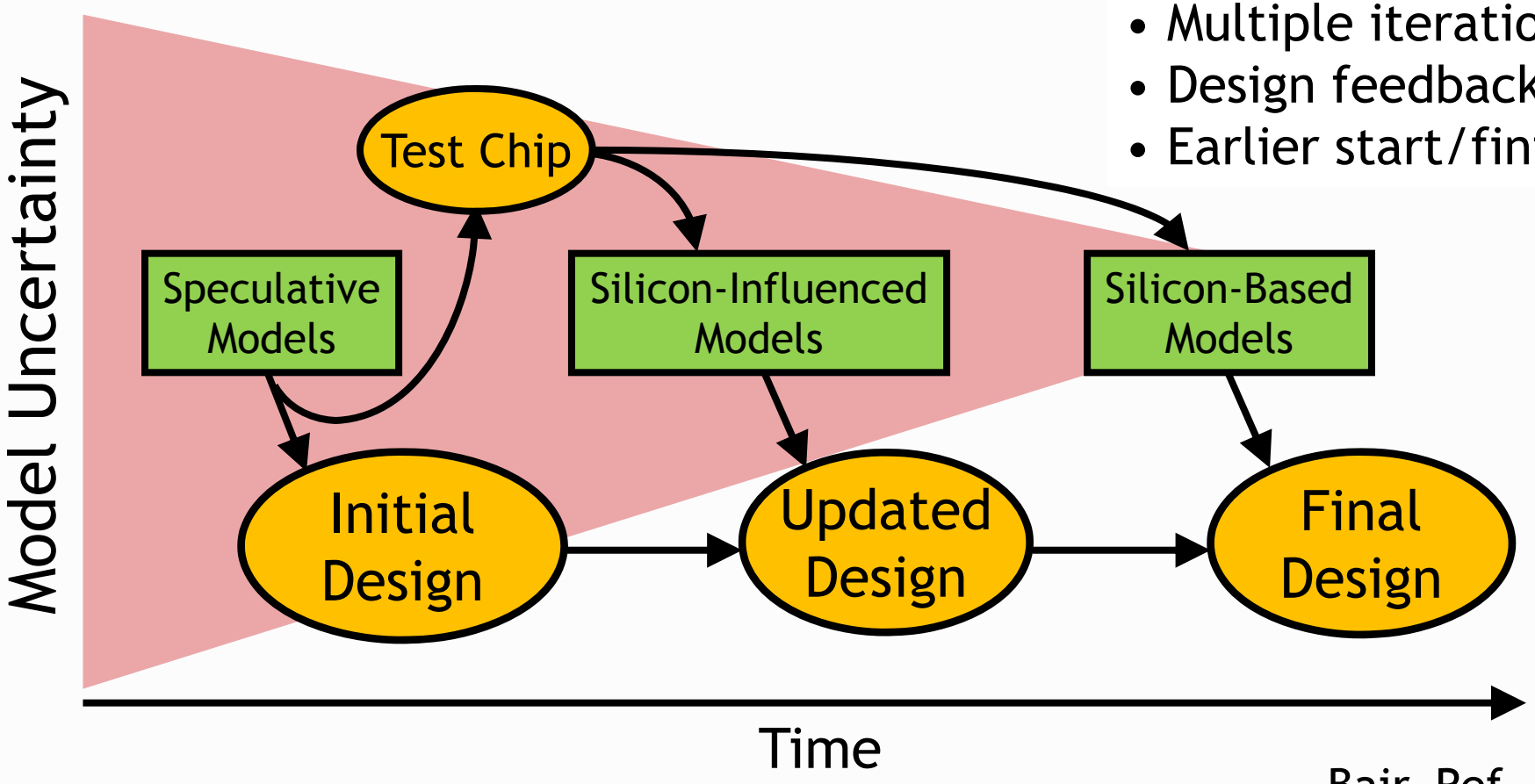
AMS Design Realities

- Difficult to co-optimize process for both AMS and logic and stay cost-effective
- So we generally have to live with what we get
  - Voltage headroom ↓
  - FETs: gain ↓, output resistance ↓, variation ↑, leakage ↑
  - Passives: as cheap as possible, choices ↓, less ideal
  - Layout proximity effects ↑
  - Circuit options ↓

Bleeding-Edge Processor Development

- Design concurrently developed with technology to shorten product time-to-market

- Multiple models
- Multiple iterations
- Design feedback
- Earlier start/finish

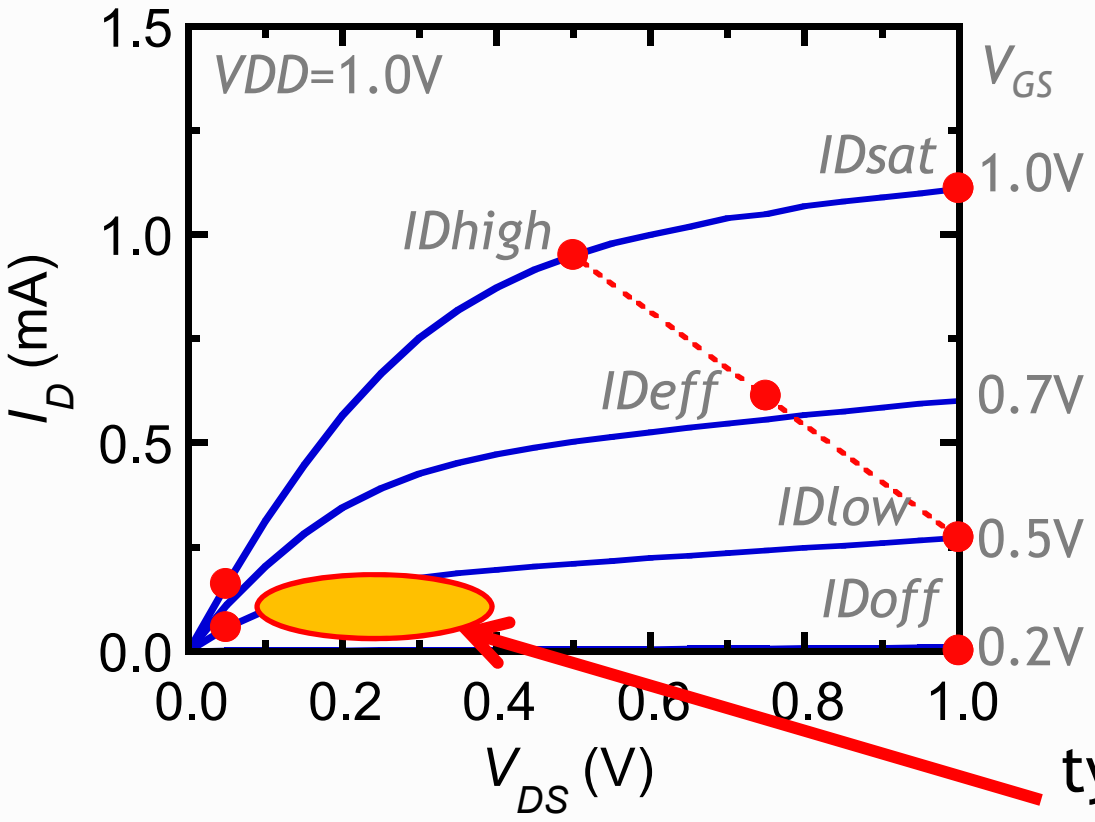


Bair, Ref. [3]

Let The Truth Be Told About Our Models

- Speculative and inherently uncertain
- Historically tailored to logic, not analog or passives
  - Go digital if it makes sense (complexity, power, area, etc.)… fab will take better care of you, easier to port to next node
- Limited to fab understanding of design usage
- Intrinsically late to capture new effects
  - e.g., STI stress, well implant proximity, stress proximities
- *Understand their limitations*

Analog vs. Digital Regions of Operation



IDeff is better metric than *Idsat* for effective inverter current in *CV/I*

Na *et al.*, Ref. [4]

typical analog biasing
$V_{GS}=V_T$ to V_T+0.2V

- Analog design needs accurate modeling of slopes (g_m, g_{ds}, etc.) as well as points (*IDsat*, *IDoff*, etc.)

Don’t Overlook the Circuit Simulator

- HSPICE calculates FET parameters (terminal currents & voltages, transconductances, capacitances, etc.) and reports them in output templates
- Parameters (as basic as V_T) may not be measured the same way on silicon
- We’ll cover examples of simulator limitations and co-development to overcome them

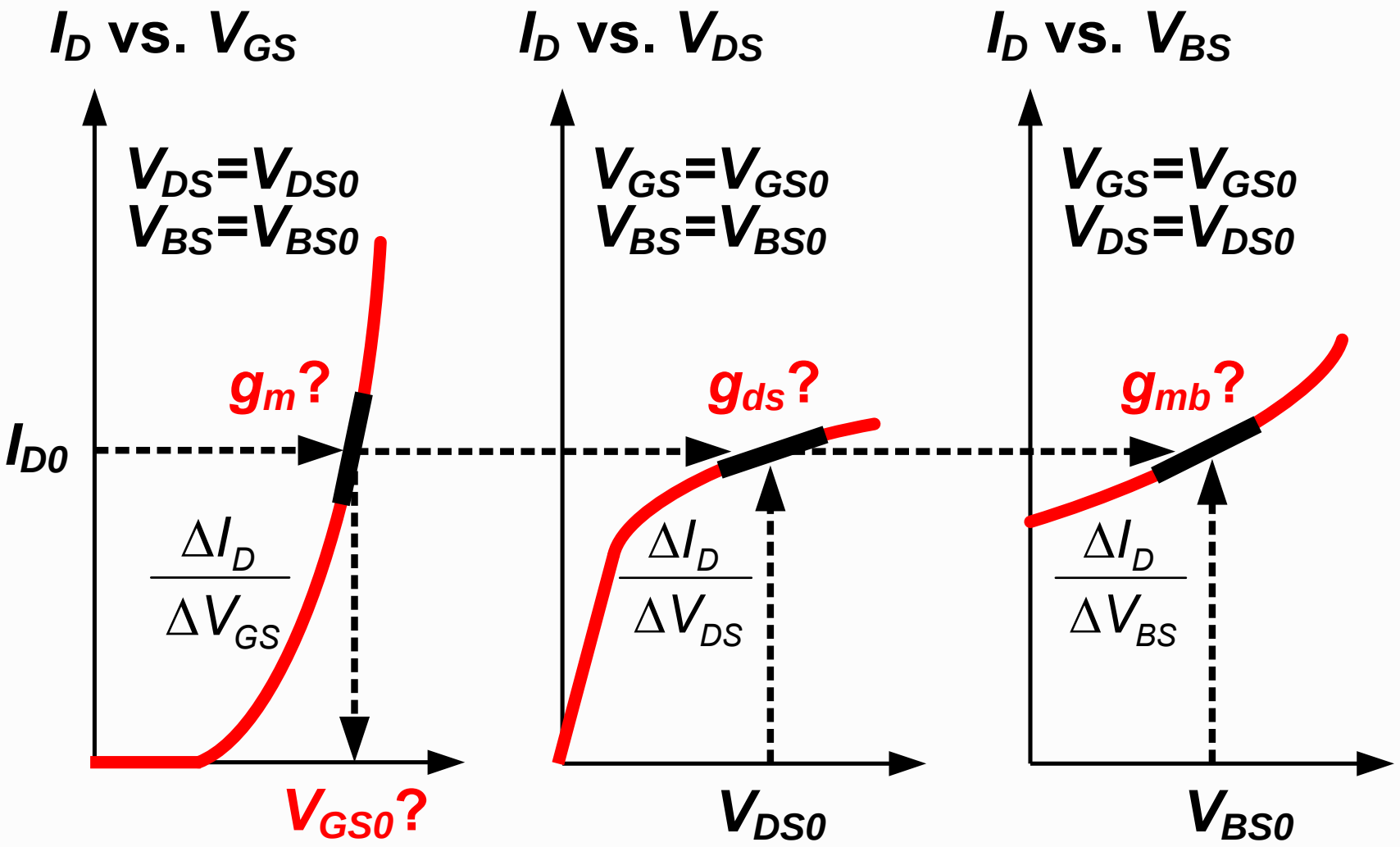
Outline

- Background & Motivation
- Device-Level Characterization
  - MOSFETs
    - Current-Based g_m, g_{ds} & g_{mb}
    - Drain saturation margin
  - Passives
- Circuit-Level Characterization
- Circuit Simulator Developments
- Conclusions

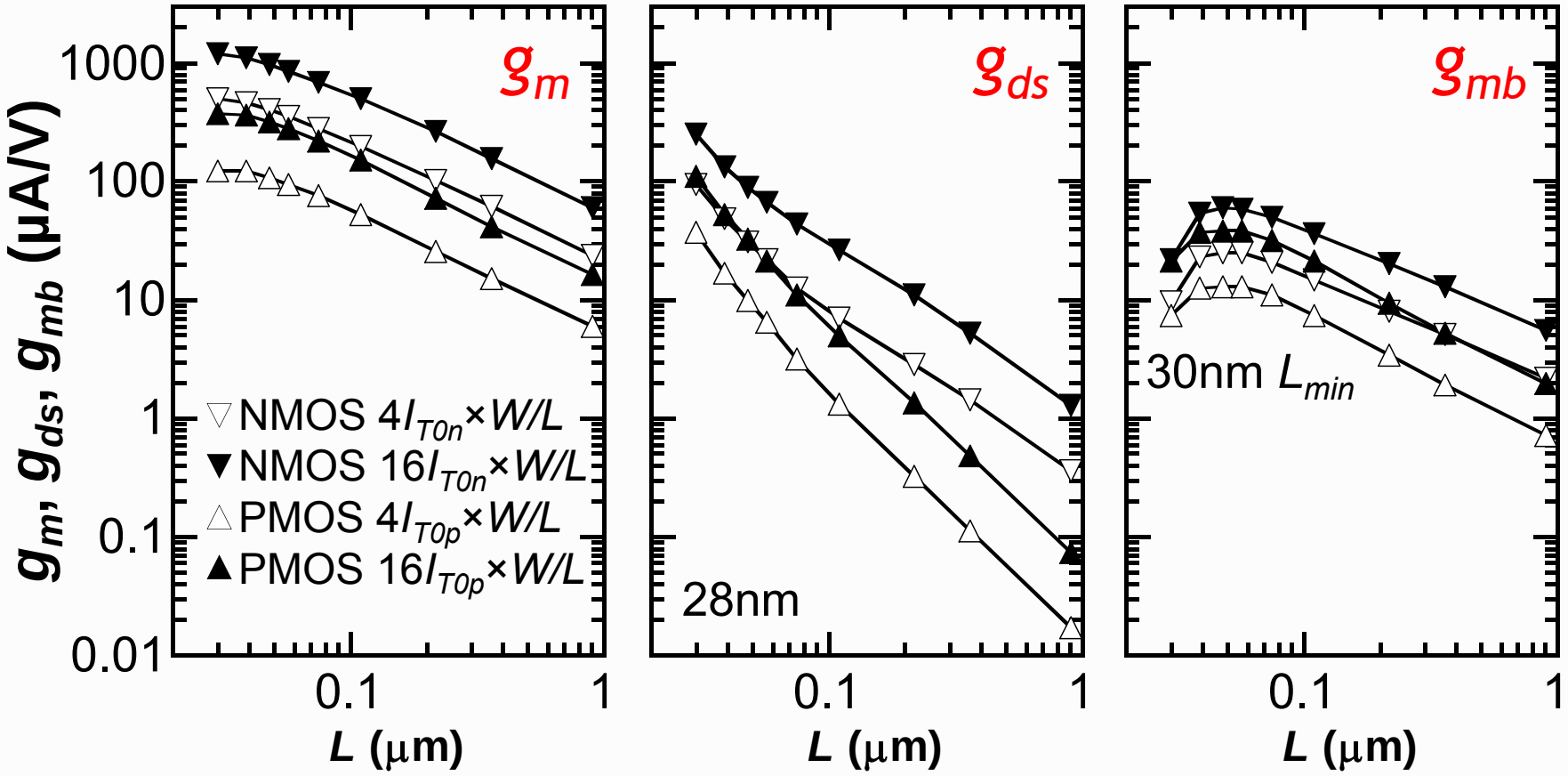
Analog Usage of MOSFETs

- Transconductor in saturation, want $I_{DS}=f$(only V_{GS})
- Fab measures g_m, g_{ds} & g_{mb} at $V_{GS} = V_T+V_{ON}$ or *VDD*
- Scaled supply → V_{ON} & $V_{DS}-V_{DSsat}$ as low as 50mV
- Constant-current V_T definition somewhat arbitrary
  - Simulated V_T criterion ≠ Fab V_T criterion
  - Cumbersome to correlate simulation to silicon
- Analog circuits typically biased by I_{REF}
- Examine g_m, g_{ds} & g_{mb} at realistic min/max I_{DS} usage

I_D-Based g_m, g_{ds} & g_{mb}



I_D-Based g_m, g_{ds} & g_{mb} Example

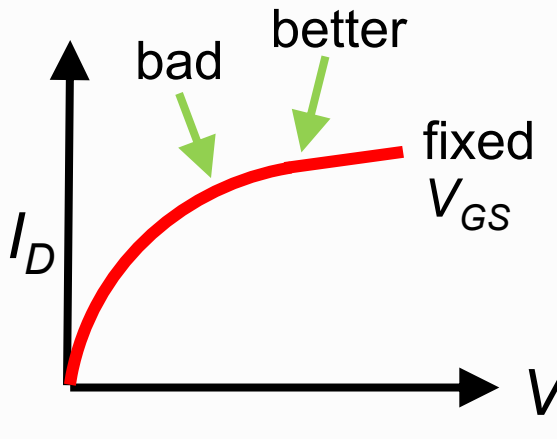


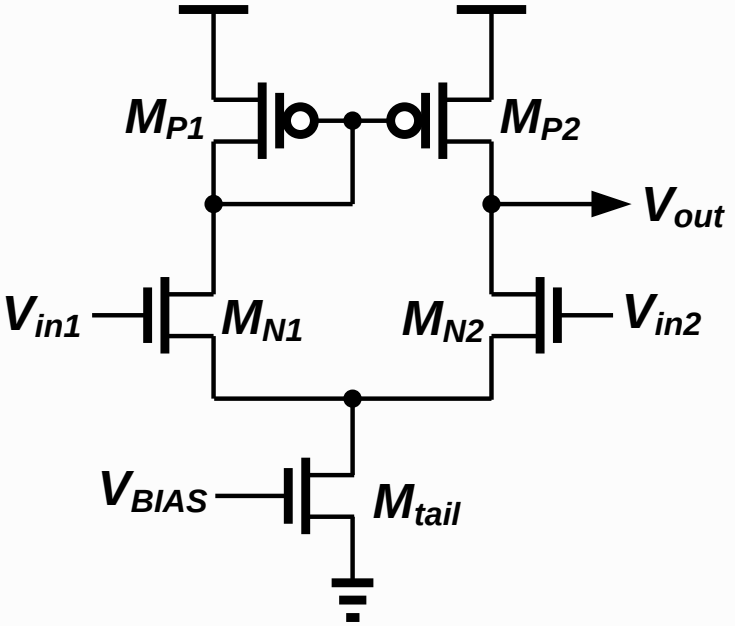
V_{DS0} = 0.4V I_{T0n} = 300nA (NMOS)

V_{BS0} = 0V I_{T0p} = 70nA (PMOS)

Saturation Margin

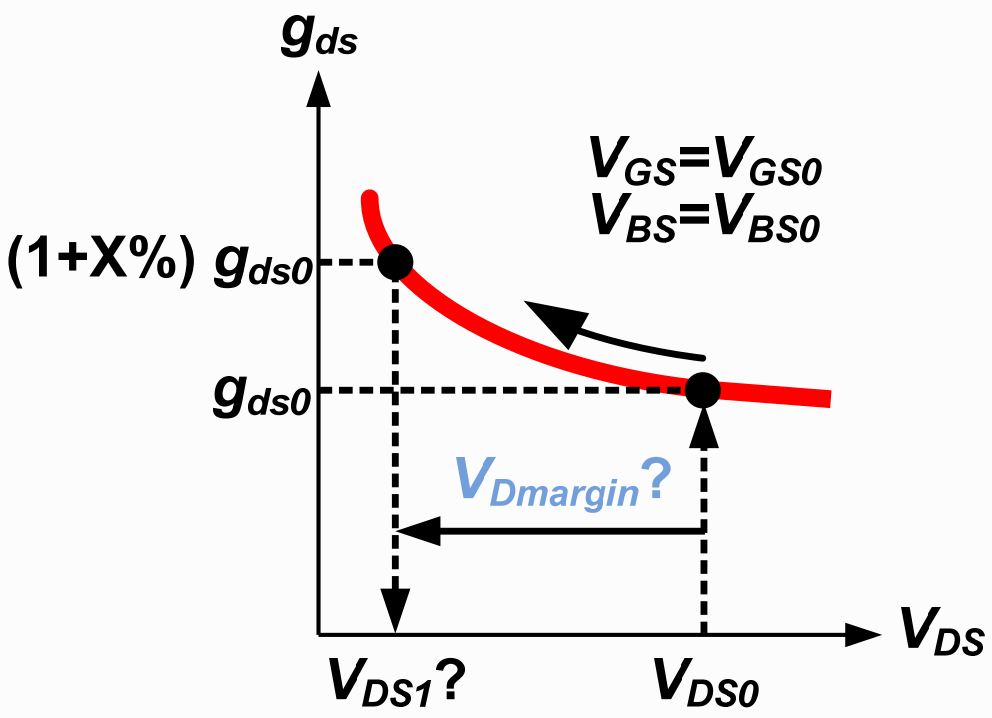
- Analog folks adamant about *biasing* FETs safely in saturation, i.e., device stays in "pinch-off"
- Need for saturation margin
  - Signal swing (sometimes with gain)
  - Modeling errors
  - Supply droop
- Saturation margin usually $V_{DS} - V_{DSsat}$
- V_{DSsat} depends on model & is difficult to measure
- Tough to have ample margin with decreasing *VDD*





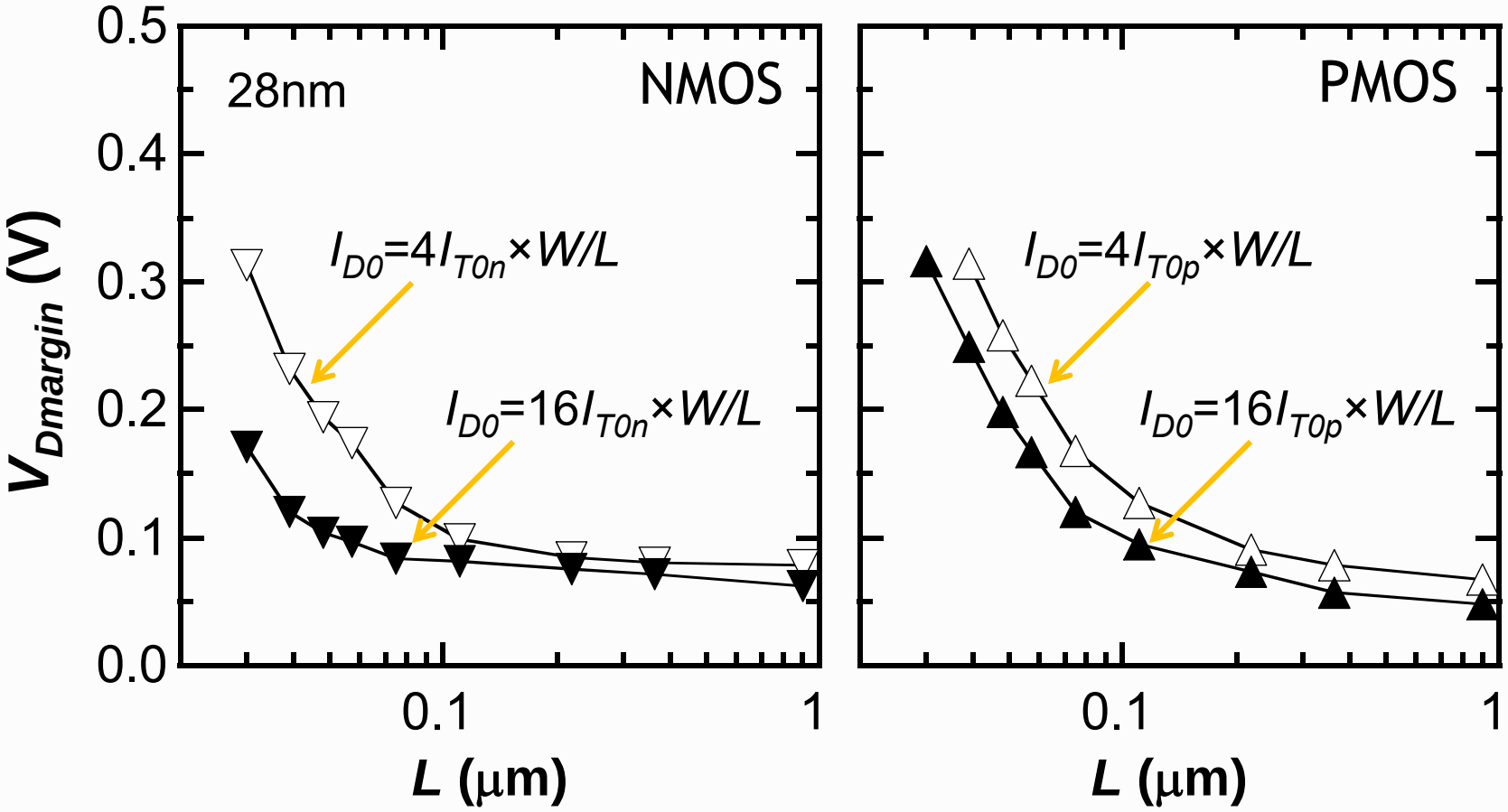
Introducing $V_{Dmargin}$

- Find V_{DS} margin available before $g_{ds}\uparrow$ by X%
- $V_{Dmargin}$ can be simulated & measured uniquely
- $V_{Dmargin}$ is much smaller in linear vs. saturation region



$$V_{Dmargin} = V_{DS0} - V_{DS1}$$

$V_{Dmargin}$ Example for Δg_{ds}=+20%

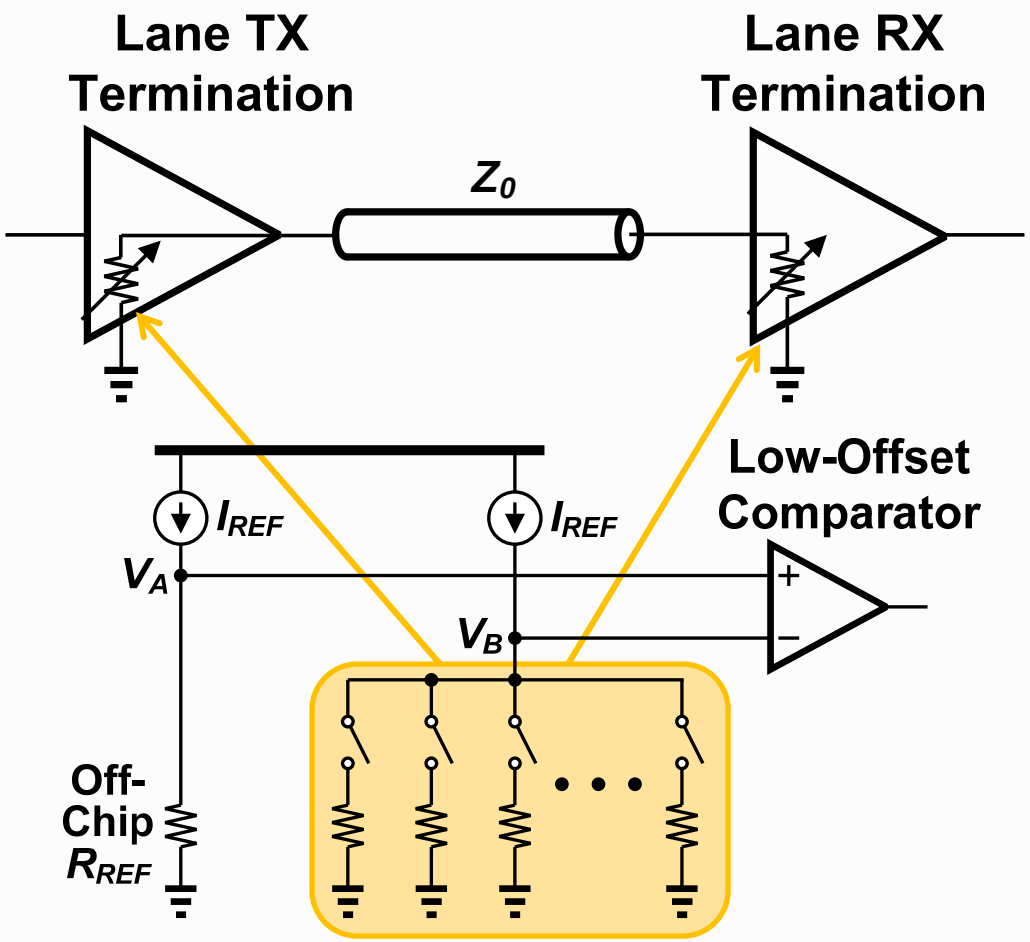


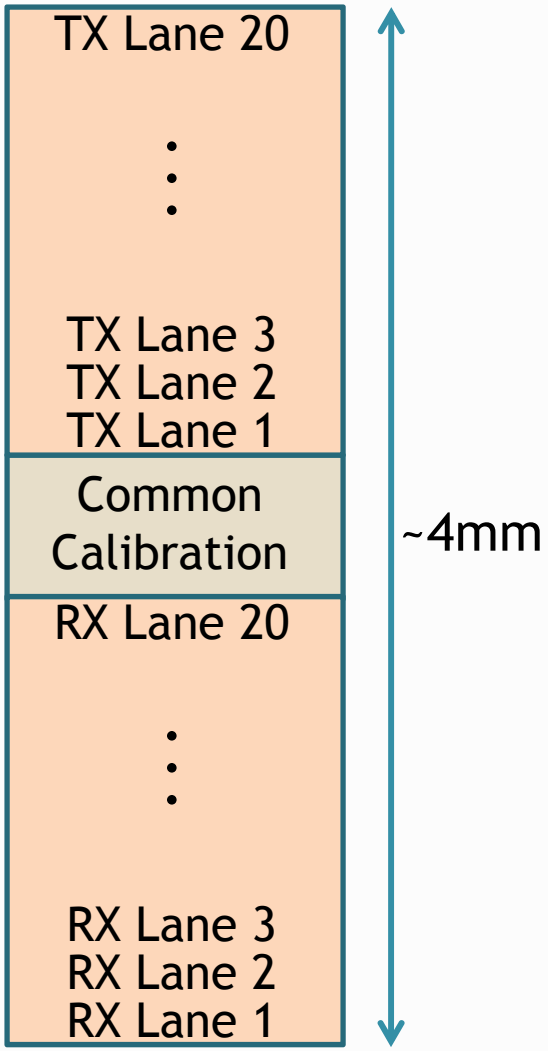
V_{DS0}=0.4V, V_{BS0}=0V

Outline

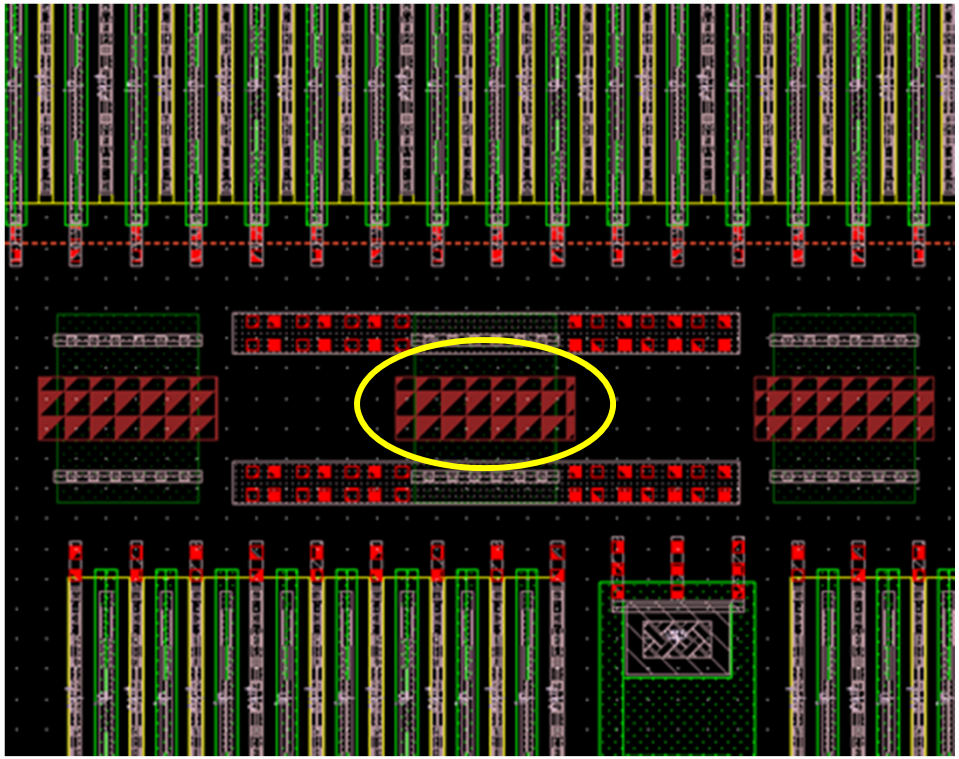
- Background & Motivation
- Device-Level Characterization
  - MOSFETs
  - Passives
    - Across-Chip Variation of Poly Resistor
    - Series Resistance of Accumulation-Mode Varactor
    - Diode Ideality
- Circuit-Level Characterization
- Circuit Simulator Developments
- Conclusions

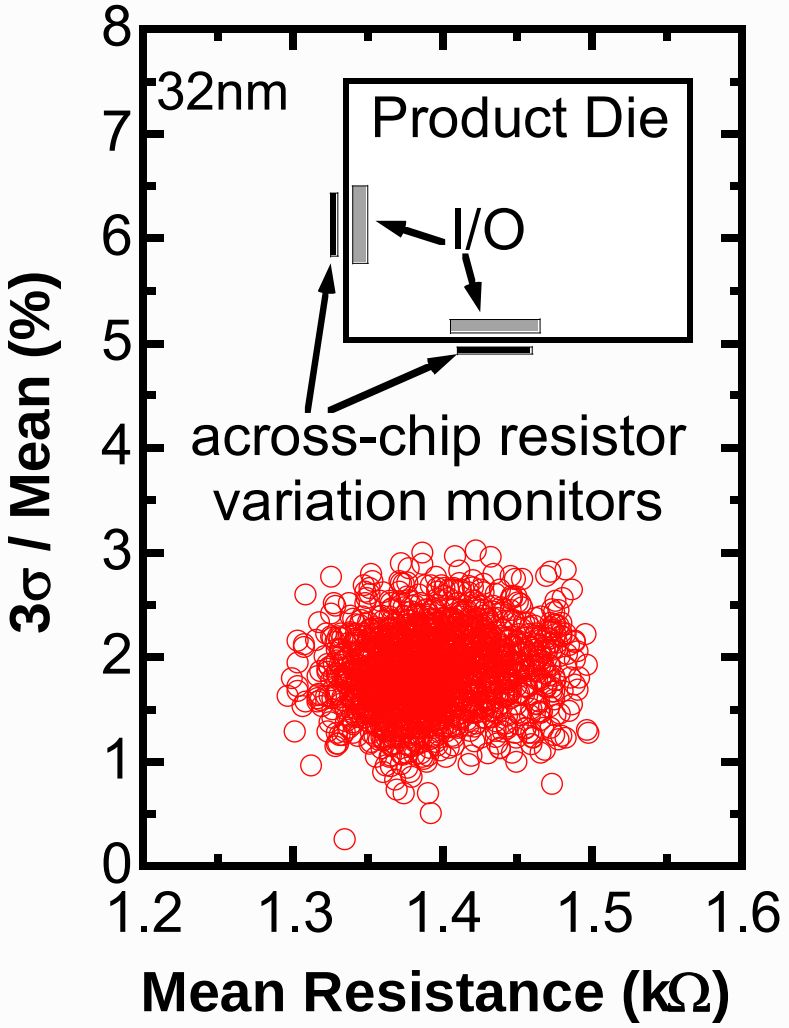
Calibration of Poly Resistance Variation





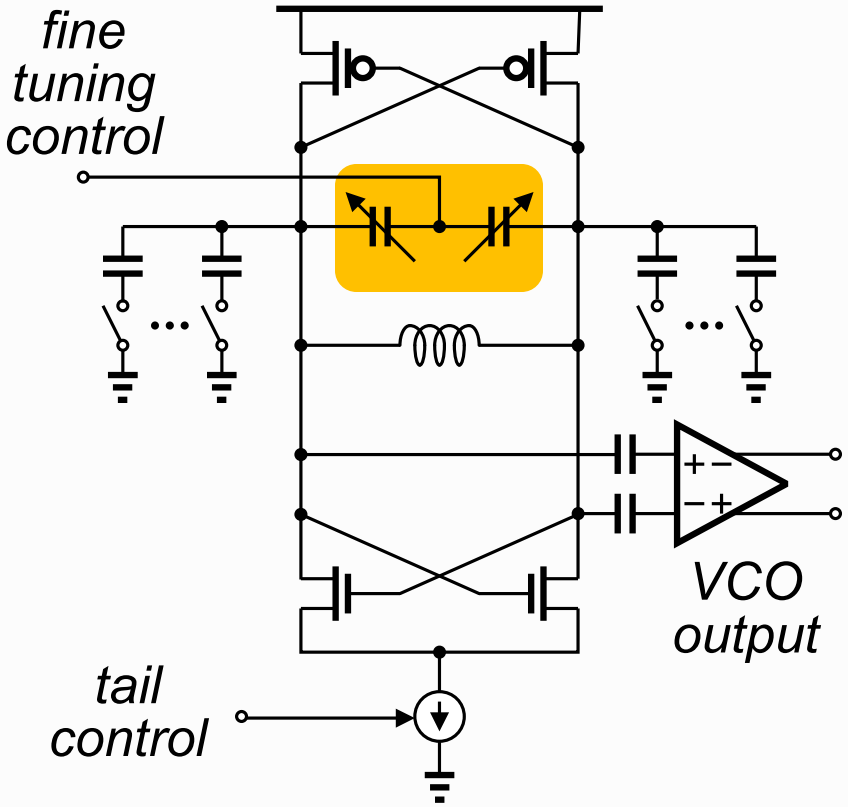
Across-Chip Variation of Poly Resistor

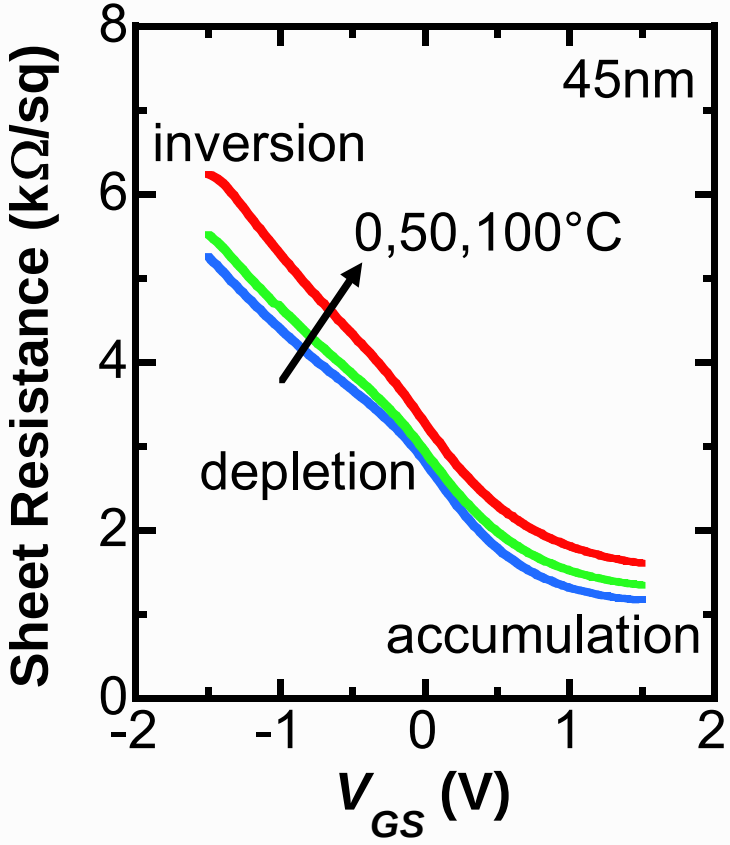




Scribe lane monitor has array of cropped I/O receiver layout to minimize scribe-to-die bias

Series Resistance of Varactor *n*-Well

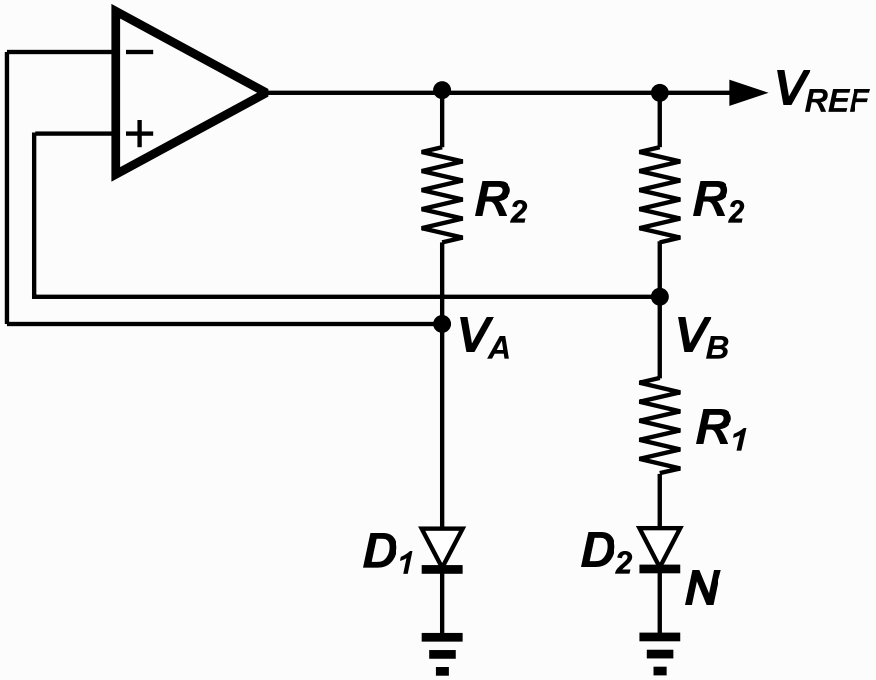




- *n*-type accumulation DECAP built for *VDD* noise reduction
- Need accurate *Q* modeling for *LC*-VCO application

Fischette *et al.*, Ref. [5]

Bandgap Voltage Reference



$$V_{REF} = V_{D_1} + I_{R_1} R_2 = V_{D_1} + \frac{\Delta V_D}{R_1} R_2$$

$$= V_{D_1} + \frac{\frac{\eta kT}{q} \ln\left(\frac{I_{R_2}}{I_S}\right) - \frac{\eta kT}{q} \ln\left(\frac{I_{R_2}}{N I_S}\right)}{R_1} R_2$$

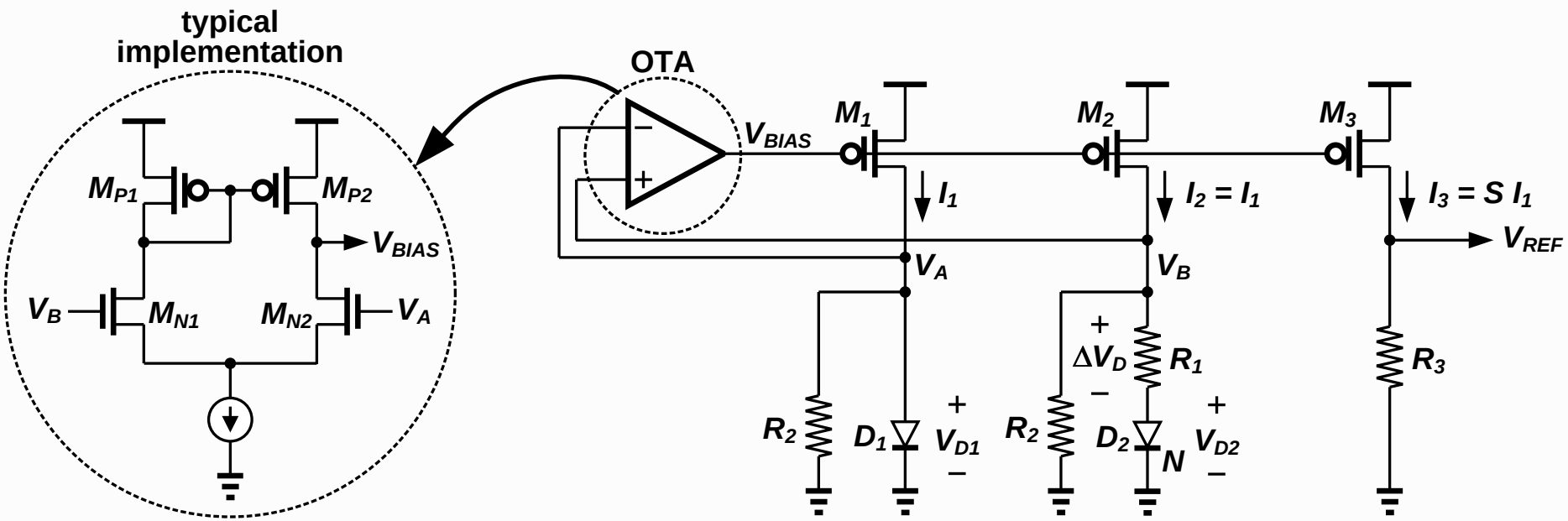
$$= V_{D_1} + \frac{R_2}{R_1} \frac{\eta kT}{q} \ln N \approx 1.2V$$

CTAT + PTAT → zero tempco

- PTAT+CTAT using voltage
- Resistors determine weighted voltage summing
- Applications: absolute voltage references, references for regulators delivering quieter power

Razavi, Ref. [6]

Low-Voltage Bandgap Reference

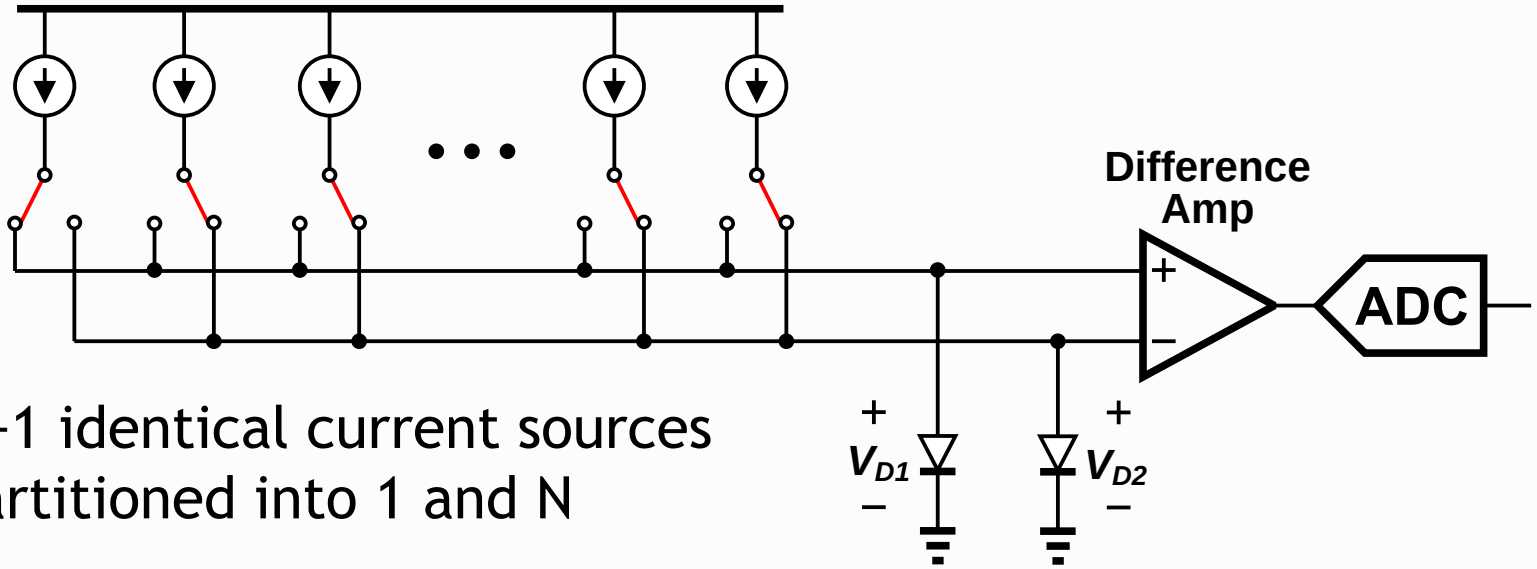


$$V_{REF} = SI_1R_3 = S\left(\frac{V_{D_1}}{R_2} + \frac{\Delta V_D}{R_1}\right)R_3 = S\left(\frac{V_{D_1}}{R_2} + \frac{\frac{\eta kT}{q}\ln N}{R_1}\right)R_3 = \underbrace{\frac{SR_3}{R_2}V_{D_1}}_{\text{CTAT}} + \underbrace{\frac{SR_3}{R_1}\frac{\eta kT}{q}\ln N}_{\text{PTAT}}$$

- PTAT+CTAT using *current*
- Resistors determine weighted summing

Banba *et al.*, Ref. [7]

Temperature Sensing

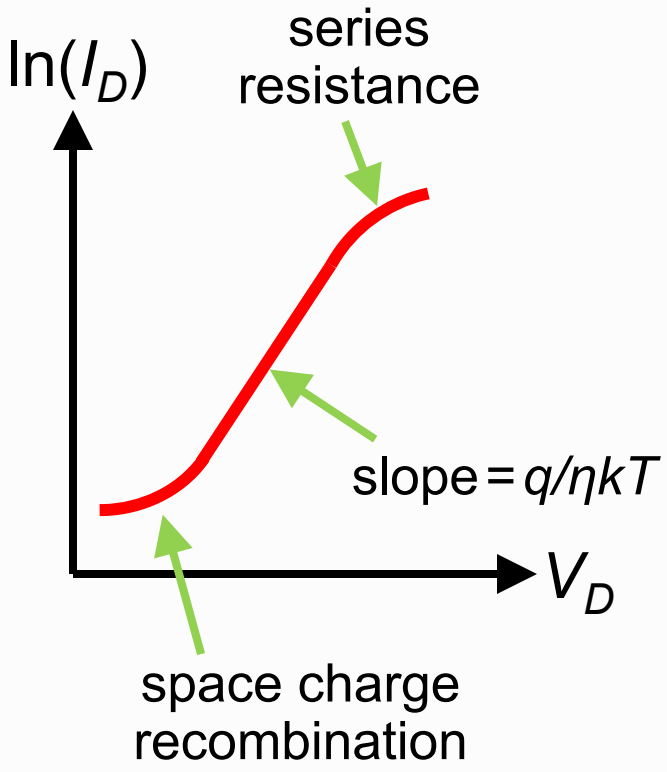


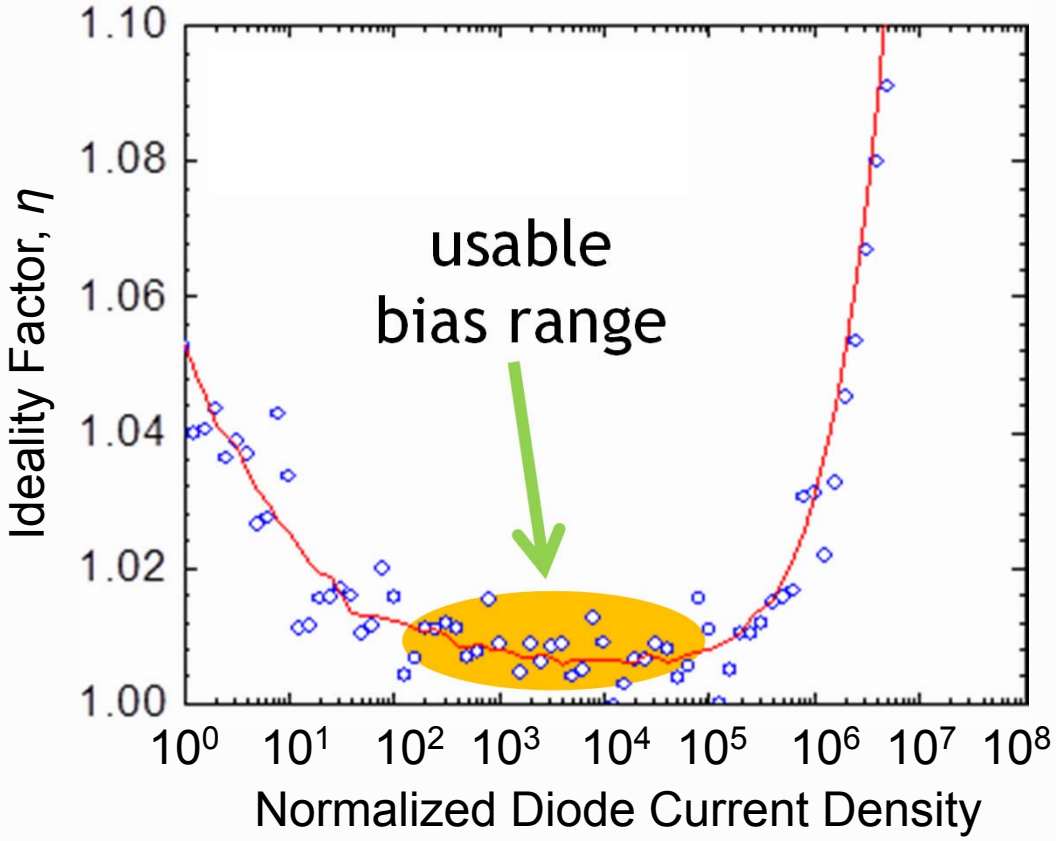
N+1 identical current sources partitioned into 1 and N

- Sense PTAT ΔV_D between identical diodes with ratio'ed currents
- Average/integrate with Dynamic Element Matching (DEM) to eliminate impact of current source mismatches
- Swap inputs to difference amp to average out offset

$$\Delta V_D = V_{D1} - V_{D2} = \frac{\eta kT}{q}\ln\left(\frac{NI_D}{I_S}\right) - \frac{\eta kT}{q}\ln\left(\frac{I_D}{I_S}\right) = \frac{\eta kT}{q}\ln N$$

Diode Ideality



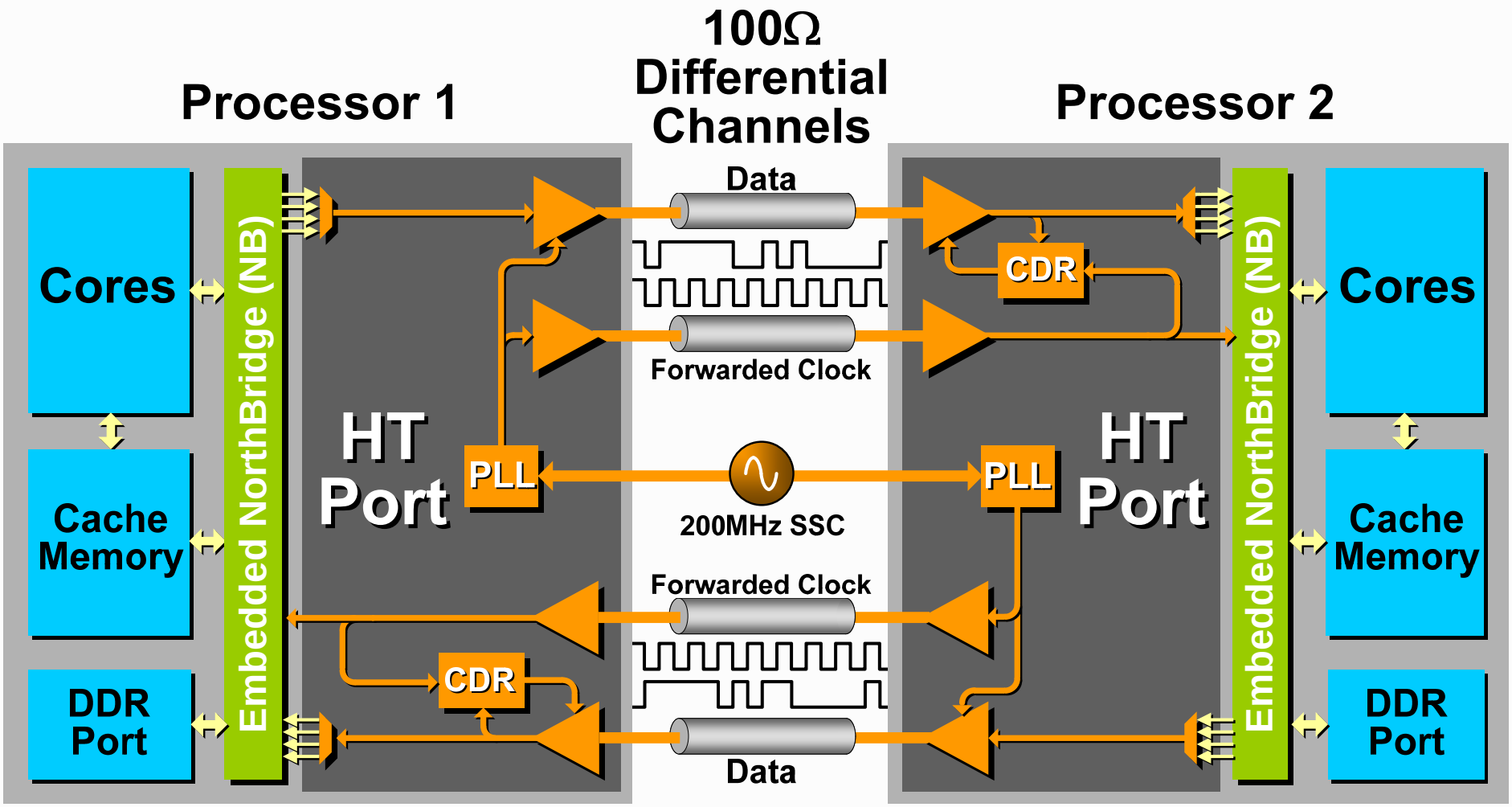


- Need to operate at constant η for accurate ΔV_D computation
- Factor some margin to cover PVT variation
- Monitor η at forward-bias current range of interest

Outline

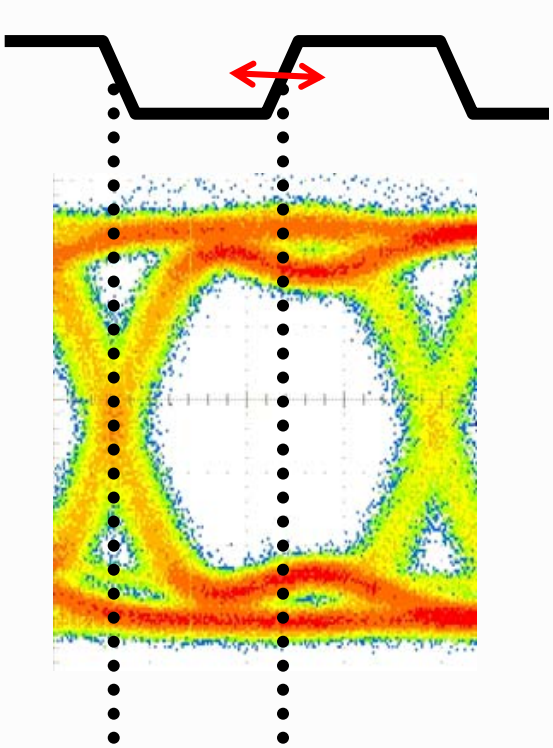
- Background & Motivation
- Device-Level Characterization
- Circuit-Level Characterization
  - Voltage-Starved Ring Oscillators
  - Transmitter Differential Output Driver
  - Pseudo-Bandgap Voltage Reference
- Circuit Simulator Developments
- Conclusions

HyperTransport™ Die-to-Die Link



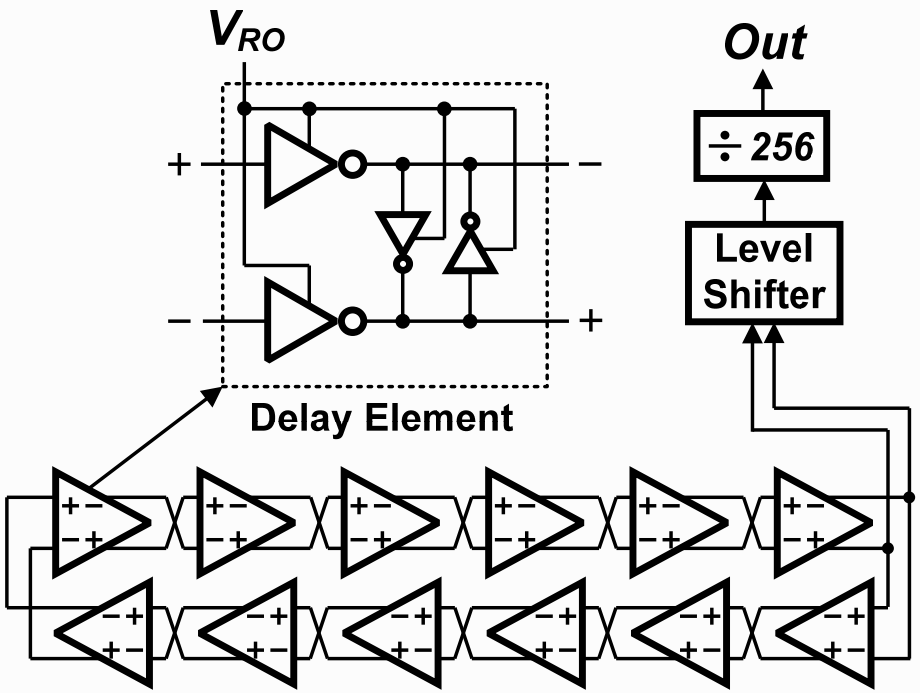
Loke *et al.*, Ref. [8]

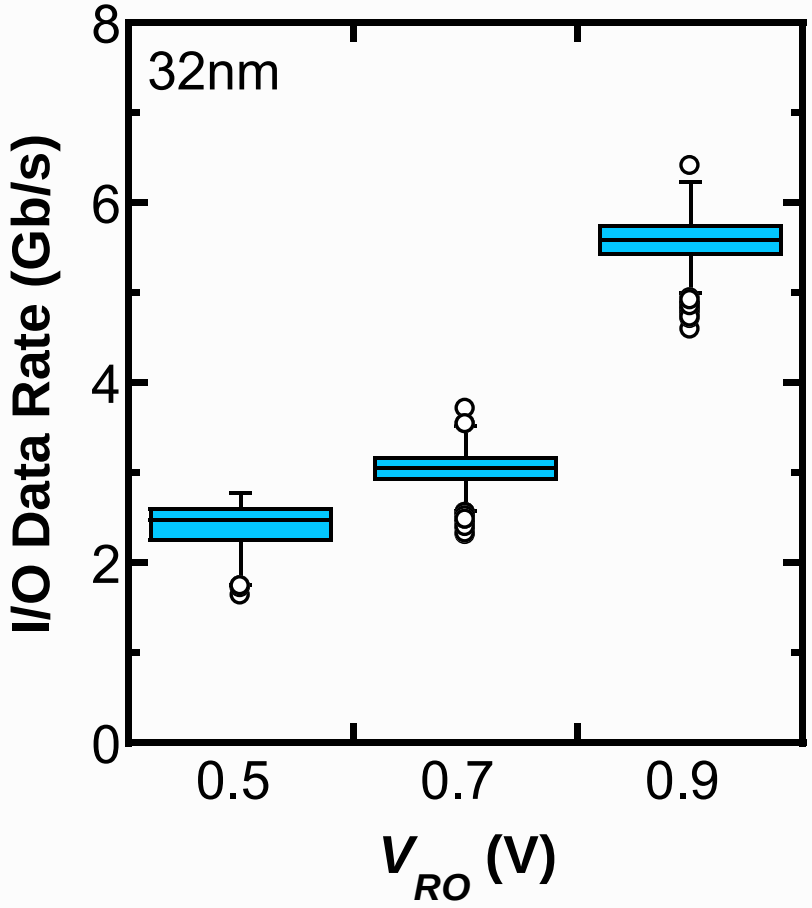
DLL for Data Recovery



- Need ability to adjust clock phase for optimum sampling of data
- Generate phases spaced by 30° for subsequent phase interpolation to achieve finer phase resolution
- Use cascade of variable delay stages to generate required phases

Voltage-Starved Ring Oscillator

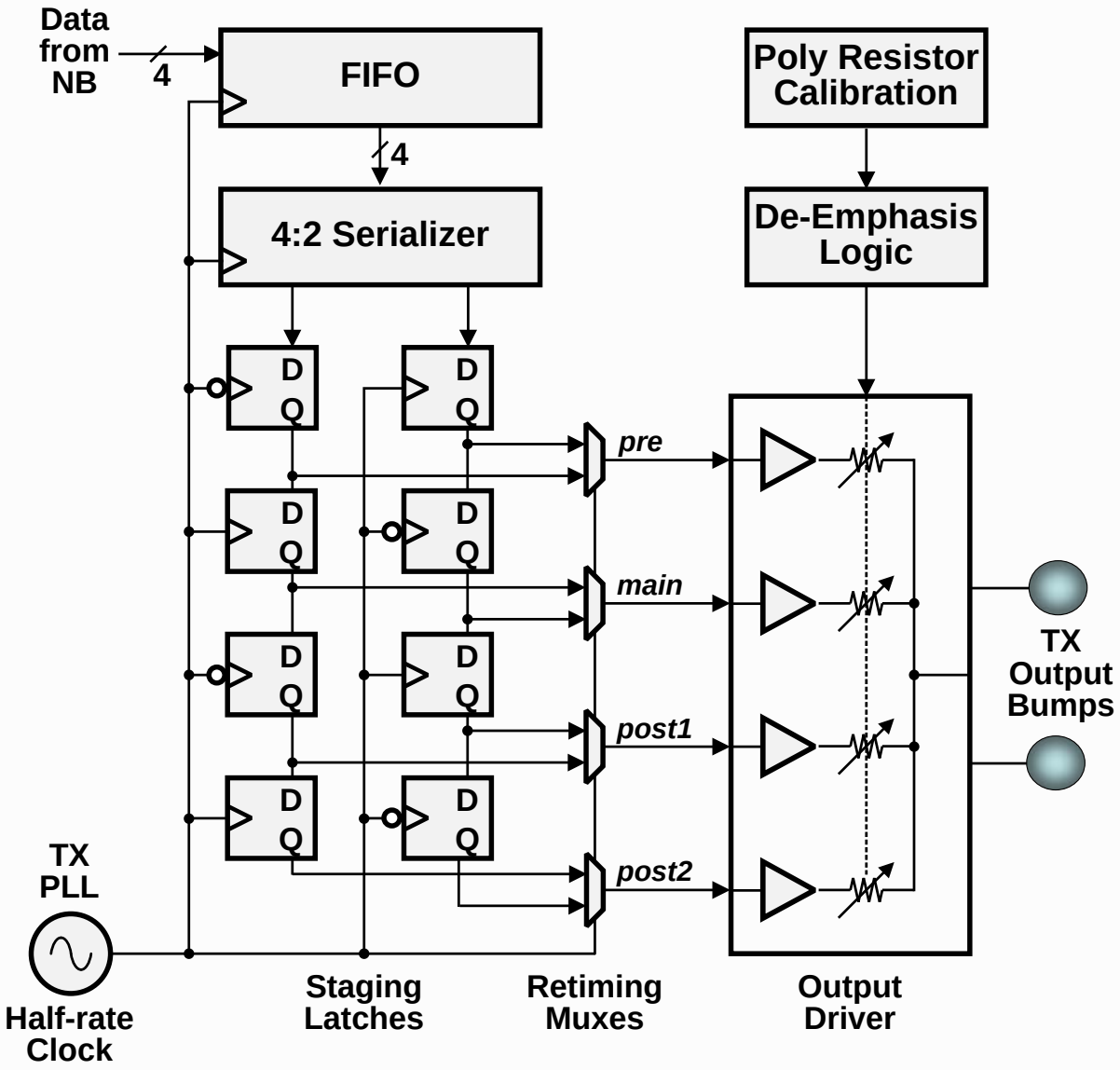




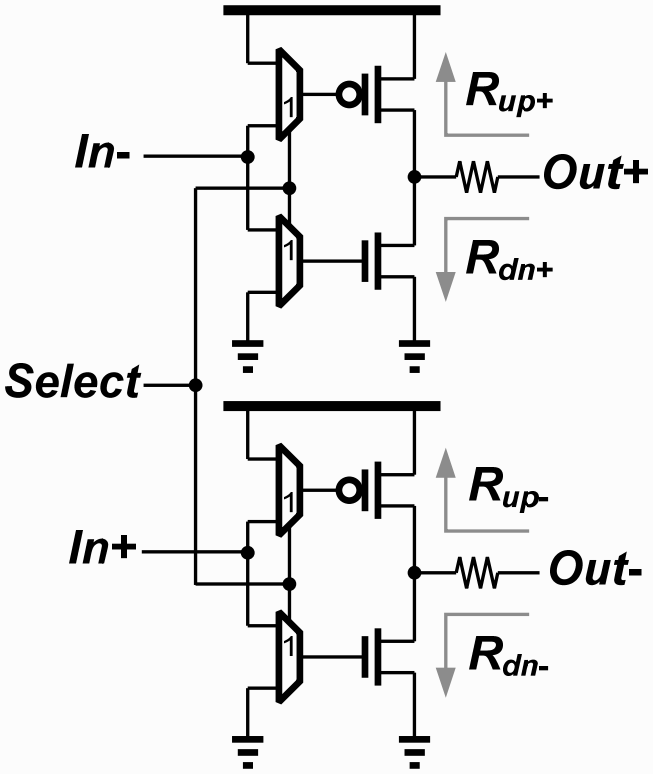
- Monitor FET digital behavior at low *VDD* (0.5-0.7V)

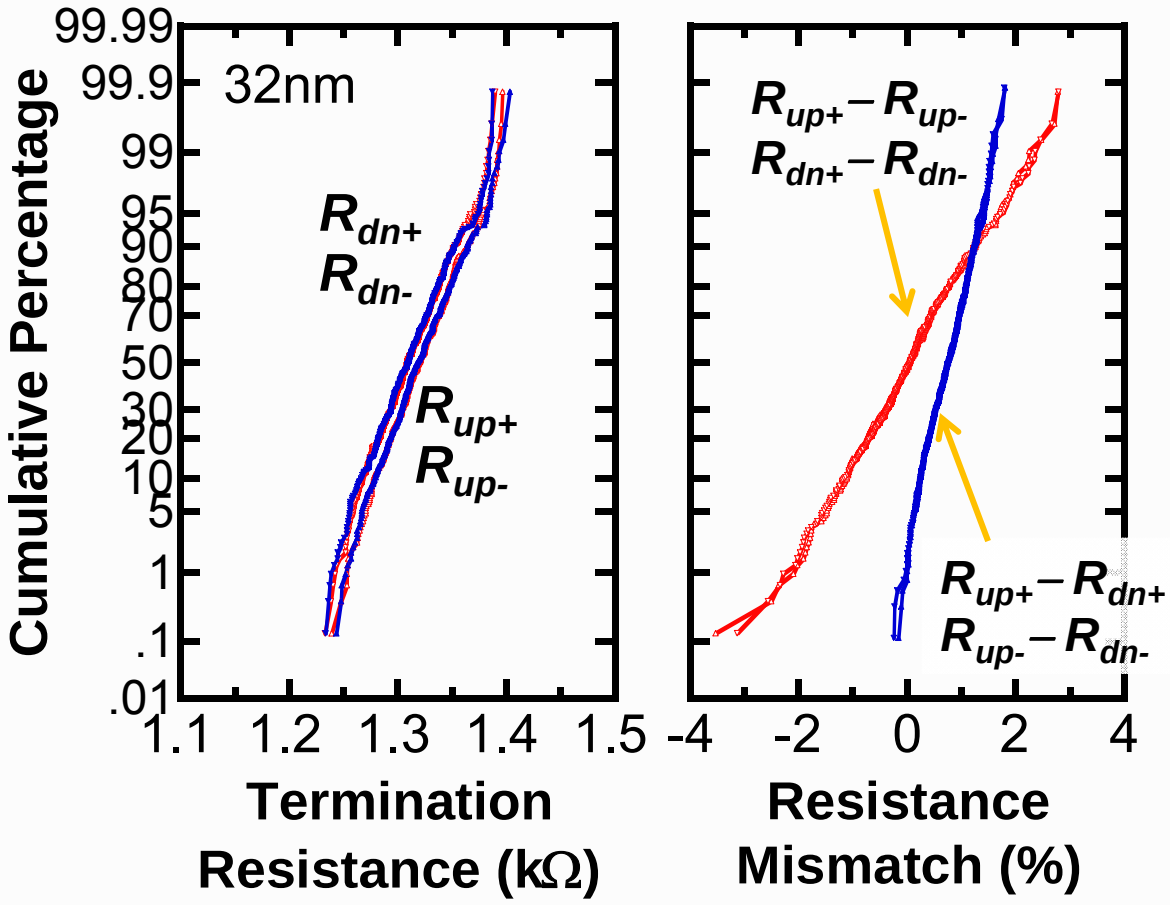
HT Transmitter Architecture

- 4-tap FIR filter to equalize channel losses
- Tunable driver output resistance to match channel Z_0 for minimal reflection



Transmitter Differential Output Driver

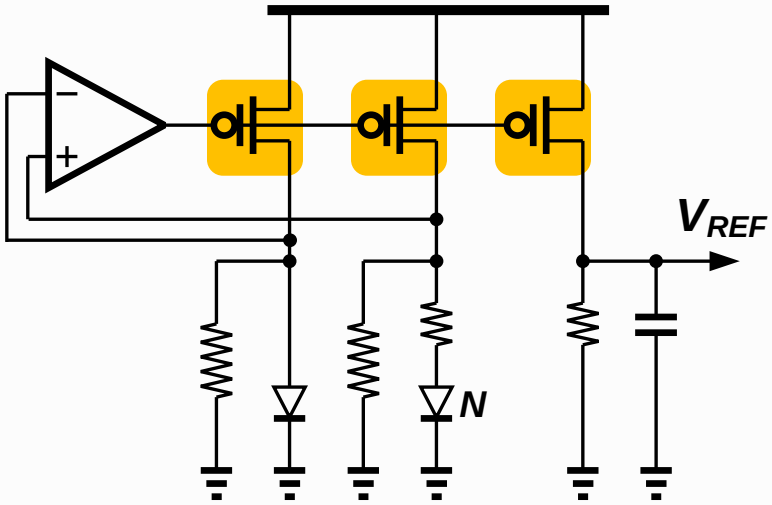




- Monitor FET R_{linear}, resistors, β ratio, mismatch

Pseudo-Bandgap Voltage Reference

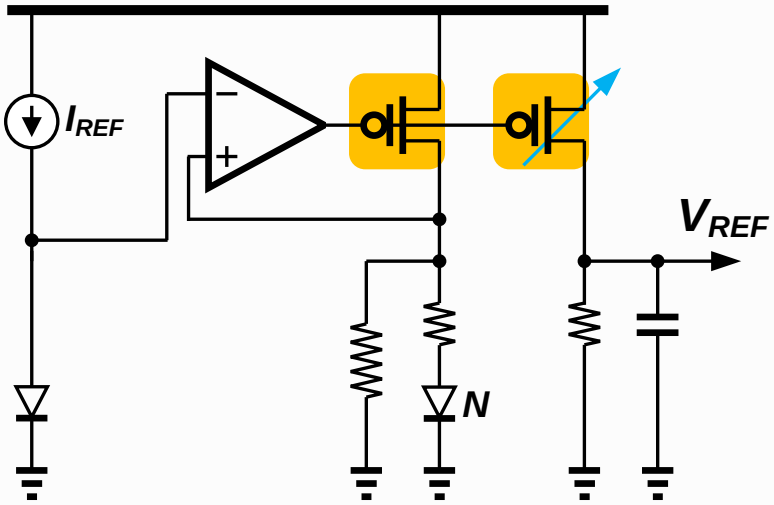
Classic Low-Supply Bandgap Reference



Banba *et al.*, Ref. [7]

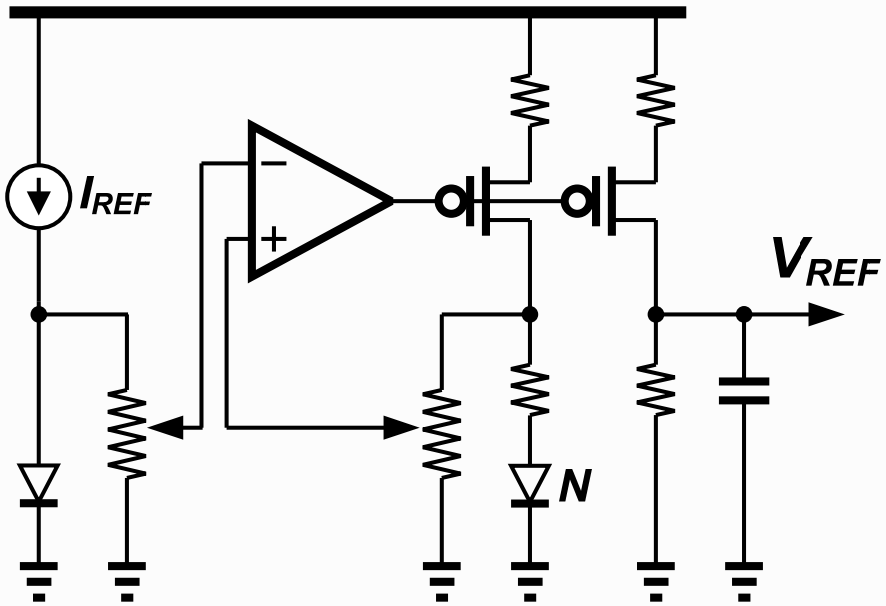
- PTAT+CTAT with current
- Prone to PMOS mismatch

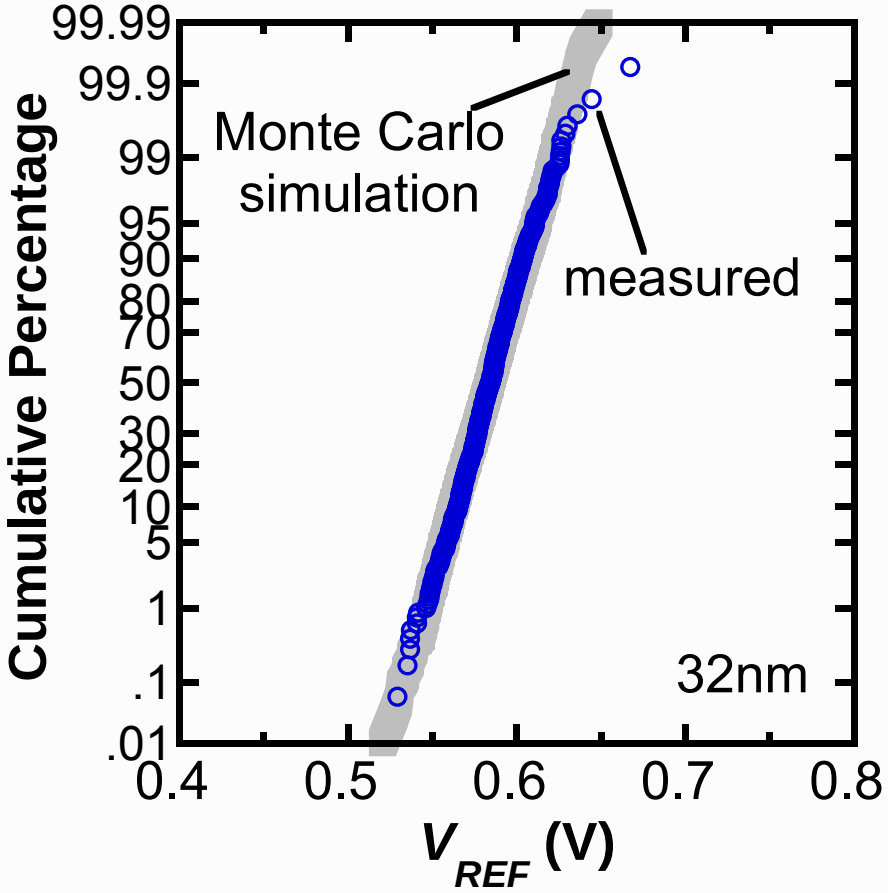
Low-Supply Pseudo-Bandgap Reference



- Less PMOS mismatch
- More systematic PVT variation which can be removed by calibration

Pseudo-Bandgap Measurements



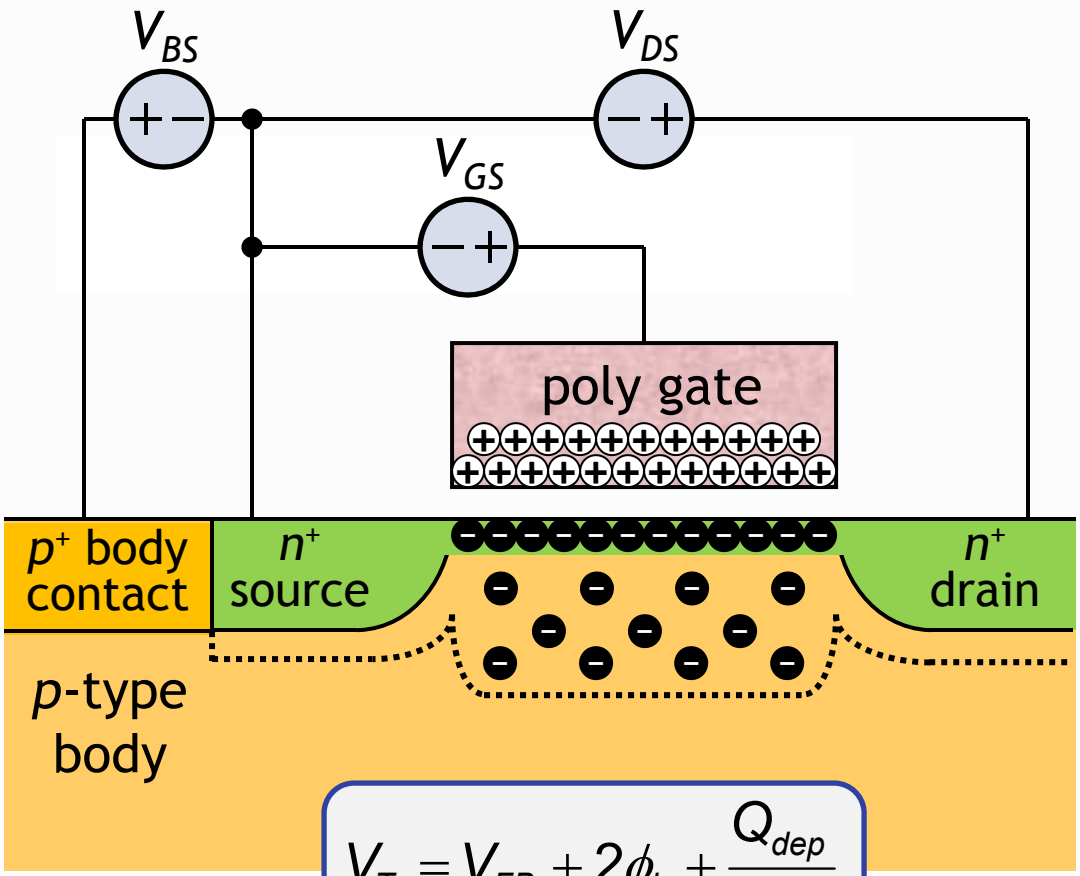


- Monitor long-*L* FETs, diodes, resistors, mismatch

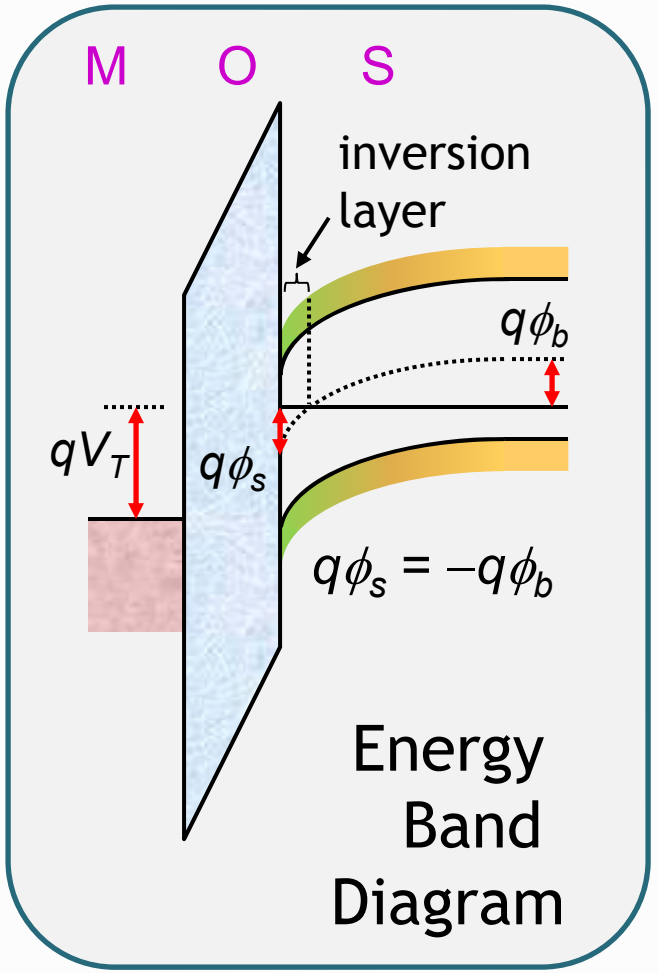
Outline

- Background & Motivation
- Device-Level Characterization
- Circuit-Level Characterization
- Circuit Simulator Developments
  - V_T Measurement
  - $V_{Dmargin}$ Measurement
  - Macromodel Output Templates
- Conclusions

Revisiting the Most Basic of Basics



$$V_T = V_{FB} + 2\phi_b + \frac{Q_{dep}}{C_{ox}}$$



BSIM4.6.2 V_T Equation – The Band-Aids

$$V_T = VTH0 + \left(K_{1ox}\cdot\sqrt{\Phi_s - V_{BSeff}} - K1\cdot\sqrt{\Phi_s}\right)\sqrt{1+\frac{LPEB}{L_{eff}}} - K_{2ox}V_{BSeff}$$

$$+ K_{1ox}\left(\sqrt{1+\frac{LPEB}{L_{eff}}} - 1\right)\sqrt{\Phi_s} + \left(K3 + K3B\cdot V_{BSeff}\right)\frac{TOXE}{W'_{eff} + W0}\Phi_s$$

$$- \left[\frac{DVT0W}{\cosh\left(DVT1W\,\frac{L_{eff}W'_{eff}}{l_{tw}}\right) - 1} + \frac{DVT0W}{\cosh\left(DVT1\,\frac{L_{eff}W'_{eff}}{l_t}\right) - 1}\right]\frac{V_{bi} - \Phi_s}{2}$$

$$- \frac{ETA0 + ETAB\cdot V_{BSeff}}{\cosh\left(DSUB\,\frac{L_{eff}}{l_{t0}}\right) - 1}\,\frac{V_{DS}}{2} - n\,\frac{k_B T}{q}\ln\left\{\frac{L_{eff}}{L_{eff} + DVTP0\left[1+\exp\left(-DVTP1\cdot V_{DS}\right)\right]}\right\}$$

- Reported in **LV9** output template

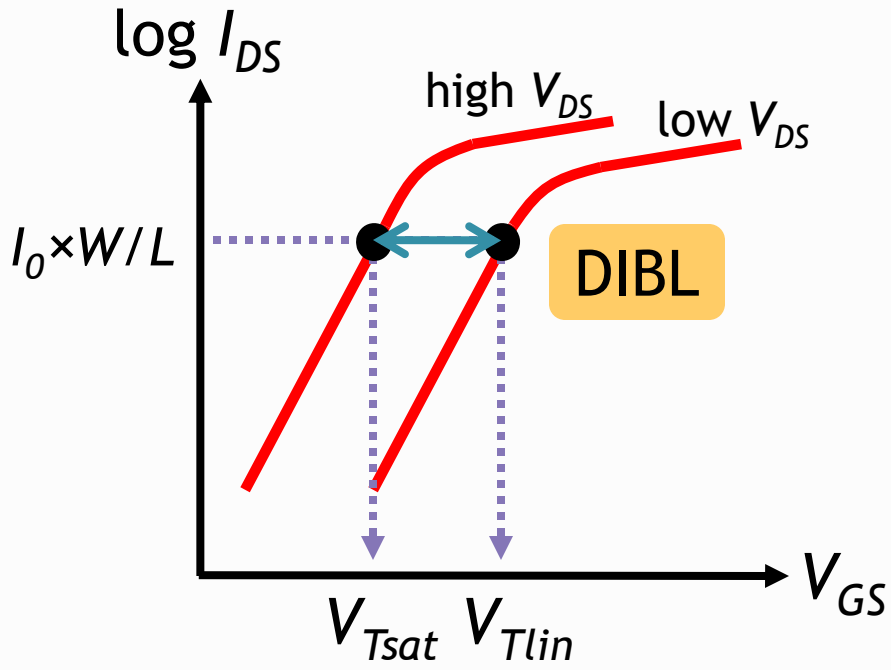
Yang *et al.*, Ref. [9]

Please… Physics *NOT* Math

- Based on “fundamental” strong inversion criterion
- Extended to *behaviorally* model
  - Body effect (V_{BS} < 0 in NMOS, V_{BS} > 0 in PMOS)
  - Short-channel effect including DIBL
  - Narrow-width effect
  - Non-uniform lateral doping – halo implants
  - Non-uniform vertical doping – retrograded well
  - LOD effect from STI compressive stress
  - Well proximity effect from implant mask scattering
- Model late to include new silicon V_T dependencies
- Impossible to measure in silicon

Fab Measurement – Constant-Current V_T

- Sweep log I_{DS} vs. V_{GS} at fixed V_{BS}
- Choose V_{DS} depending on region of operation
- Find V_{GS} when I_{DS} crosses user-specified threshold I_0 normalized to W/L
- Typical I_0 ~ 10 to 500 nA
- No physical connection to onset of strong inversion
- Be careful when you compare V_T across foundries → know their I_0

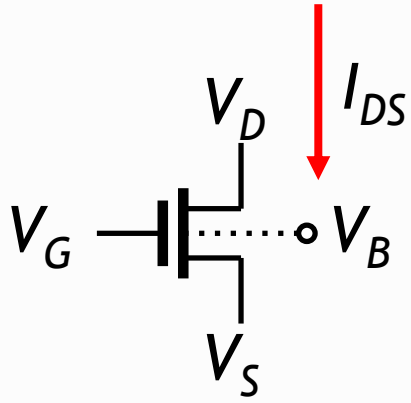


$$V_T = V_{GS}\Big|_{I_{DS}=I_0\times\frac{W_{drawn}}{L_{drawn}}}$$

Simulating What The Fab Measures

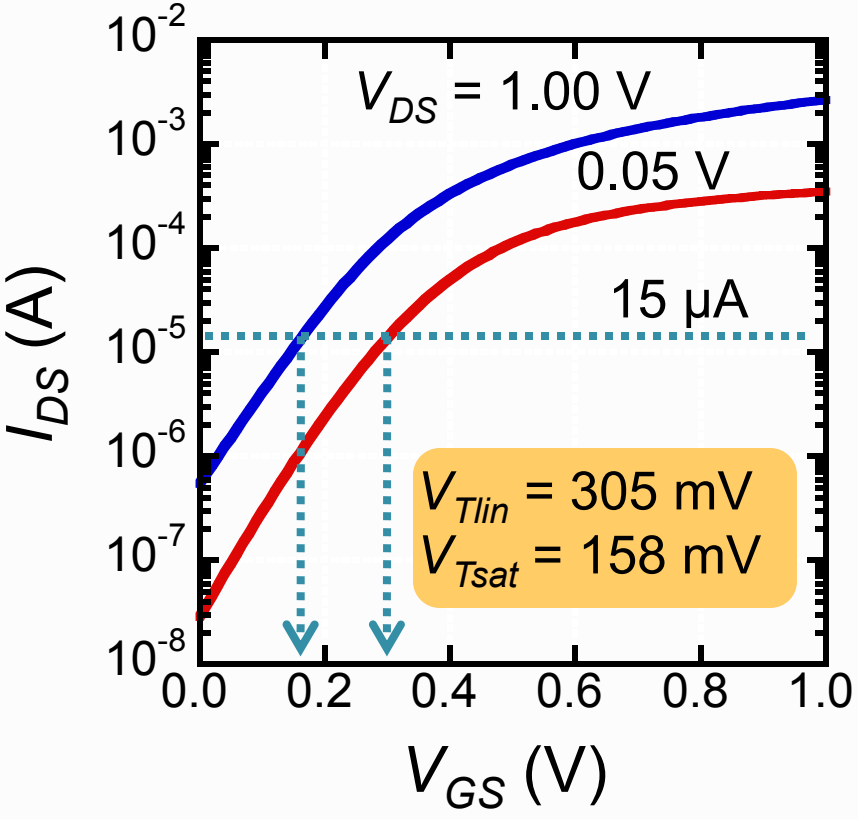
- **`.OPTION IVTH=`*`val`*` | IVTHN=`*`val1`*` | IVTHP=`*`val2`**
- Freeze FET node voltages at given instant
- Determine V_{GS} for $I_{DS} = I_0 \times W_{drawn} / L_{drawn}$
- Report extracted V_T in **LX142** output template
- V_{DS} limited to **VDSMIN** (50mV default)
- Feature available since HSPICE-2009.09

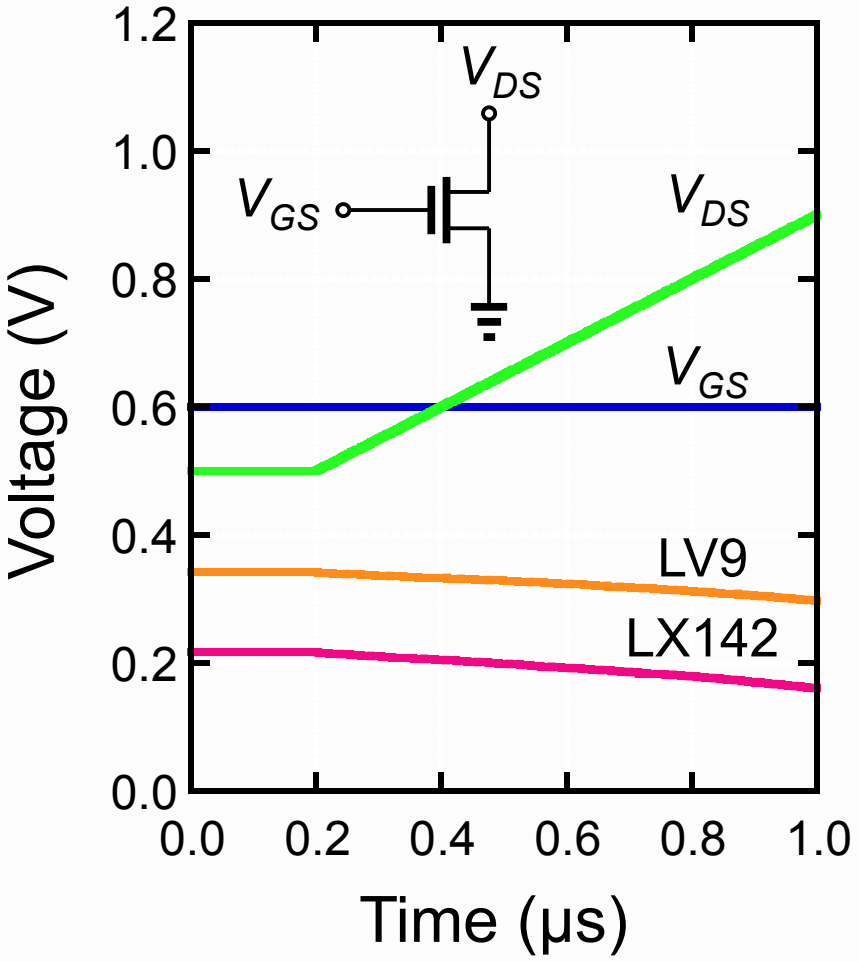
V_{GS} = ? for
I_{DS} = **IVTHN** × W/L



LX142 Example

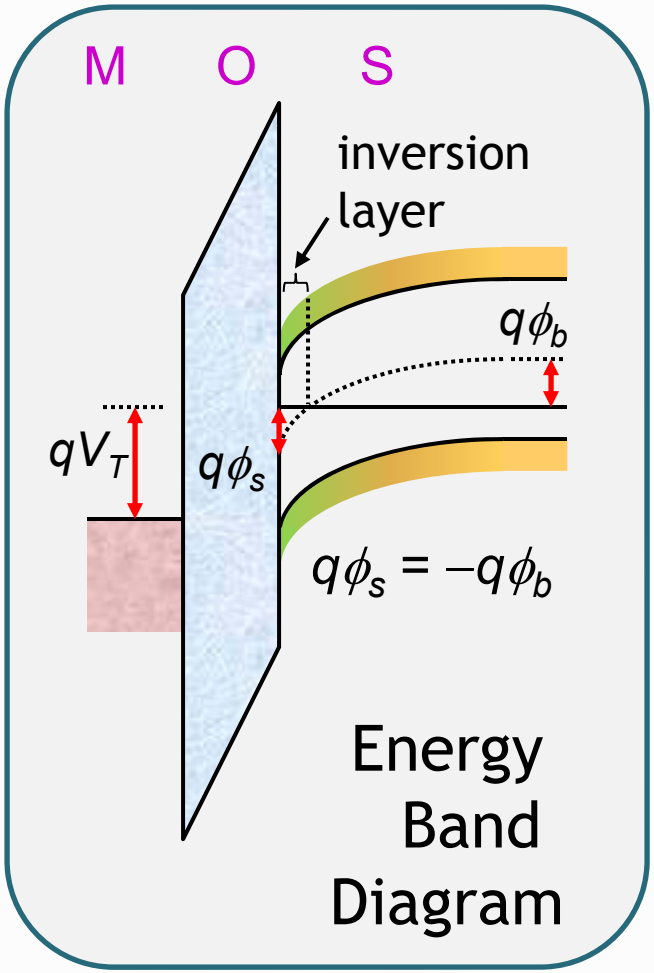
32nm SOI-CMOS, I_0 = 300nA





Loke *et al.*, Ref. [10]

Not So Fundamental After All



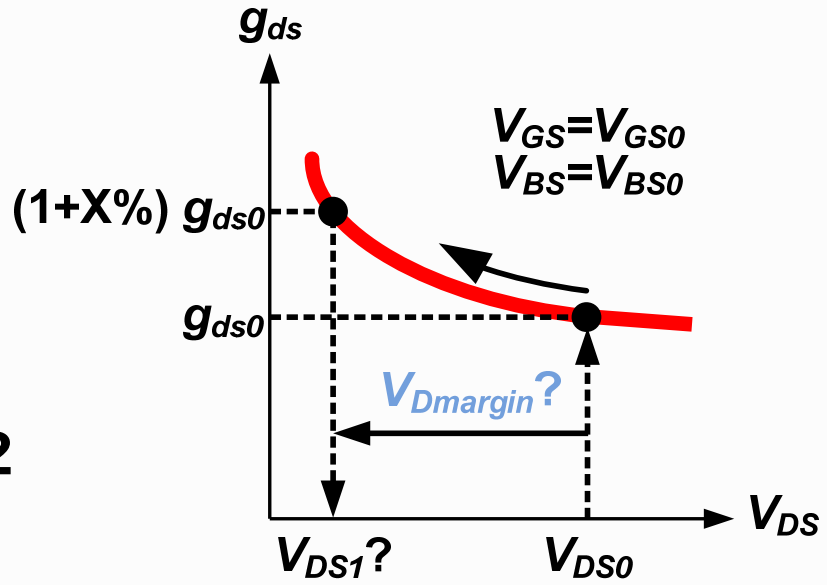
$$V_T = V_{FB} + 2\phi_b + \frac{Q_{dep}}{C_{ox}}$$

- Body doping levels have increased by 2-3 orders of magnitude over the decades
- Surface charge density way more conductive at strong inversion condition based on "fundamental" V_T definition
- Best to treat V_T as just a *reference point*
- I_{OFF} vs. I_{ON} plots have become universally more important for reporting device characteristics

$V_{Dmargin}$ in HSPICE

- Feature recently implemented in HSPICE-2012.06
- **LX286** output template
- Usage example

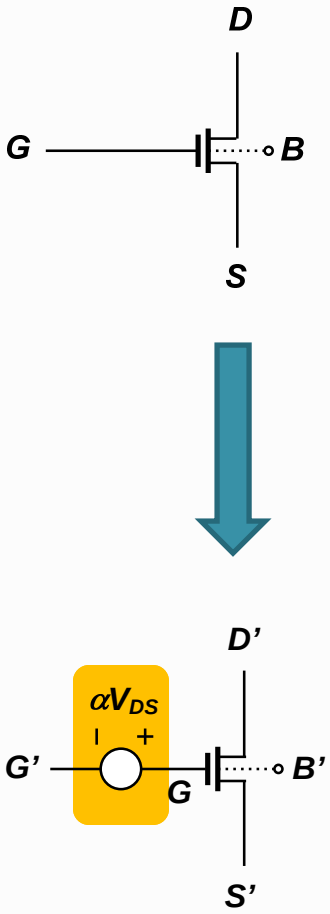
```
.IVDMARGIN M3 DELTAGDS=0.2
.PRINT DC VDMARGIN(M3)
```



$$V_{Dmargin} = V_{DS0} - V_{DS1}$$

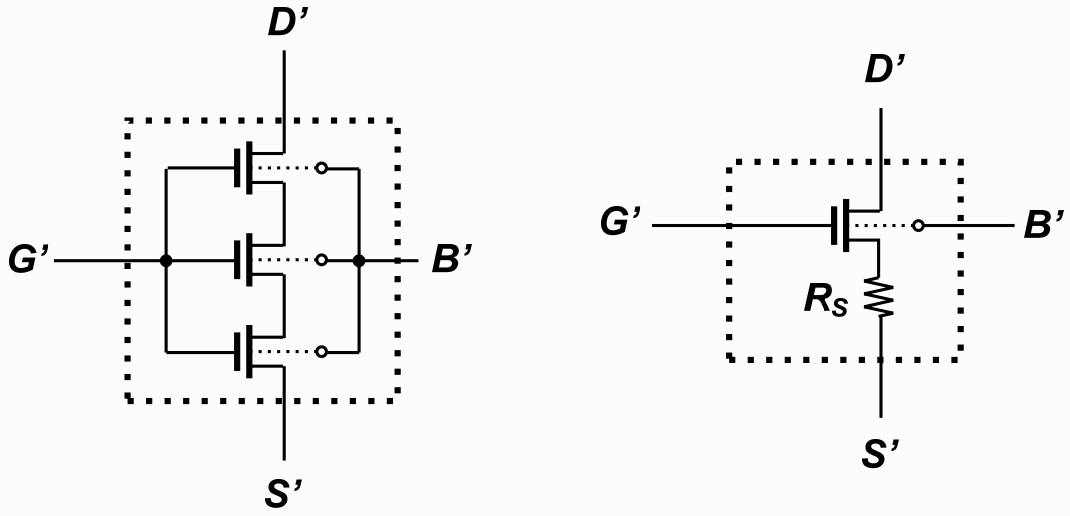
Macromodel Output Templates

- Models late to capture new silicon observation
- Meanwhile, foundries build subckt wrappers around intrinsic models
- Output templates report device characteristics of intrinsic model BUT what really matters are characteristics of the subckt
- Example
  - V_{DS}-controlled voltage source in series with gate to degrade V_T and g_{ds} for better correlation to observed silicon at process corners
  - "DIBL wrapper" took over a year to implement into BSIM4.7
- Co-development with Synopsys R&D in progress to provide subckt output templates



Extending Macromodel Concept

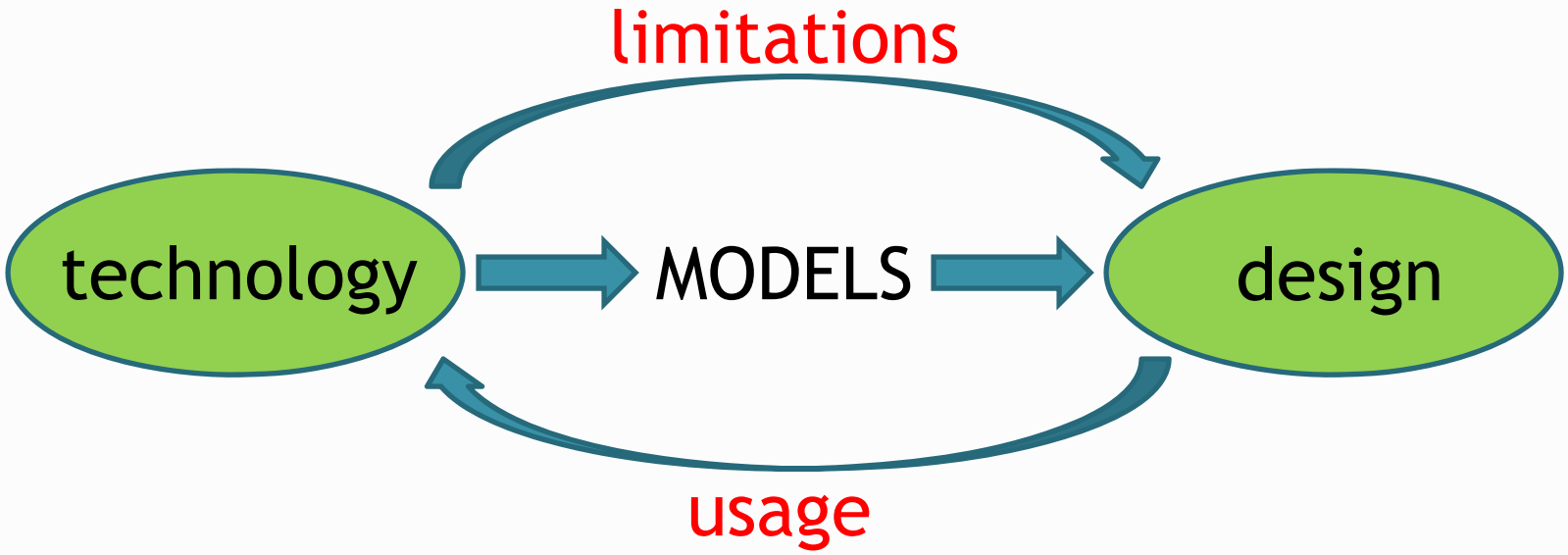
- Scaling of conventional planar devices continues to constrain analog design, e.g., poor g_{ds}
  - Stronger halo implants for short-channel control
  - Stricter L_{max} from replacement-gate HKMG integration
- More frequent usage of source degeneration to reduce g_{ds}



- Really interested in output template of composite device

Conclusion

- Scaling will continue to be more restrictive on AMS
- Co-development improves model quality and fab monitoring of device behavior for AMS designs
- Pay attention to details, don't overlook CAD



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