Signal Integrity 101

A brief overview of Signal Integrity and where it fits in the Digital Design Process.

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What is the Objective of Signal Integrity Analysis?

- Ensure the reliable operation of a digital design by predicting, measuring and modifying the behavior of electrical signals on interconnects between electronic components.
- In general the SI Engineer is not interested in (IC) core functions, except where these generate external timing constraints.

How do we achieve the goal?

1. Identify Signal Integrity Constraints
    - Driver to Load Delays
      (including effects of crosstalk and ring-back)
    - Overshoot Voltages
    - Other Signal Quality Measures
      (Eye opening …)
2. Measure or Simulate the Interconnect
3. Modify the behavior of the Interconnect to meet the constraints.
    - Terminate, modify trace routing, change components…

Challenges associated with Measurement.

- Bandwidths are continuously increasing
  - Now commonly seeing 3-4 Gbits/sec.
  - Measurement equipment vendors are investing considerable resources in keeping up
  - Equipment is expensive and may become quickly obsolete.
- Difficult to make measurements without modifying the signal you are trying to measure.
  - Excellent papers from equipment vendors and independent consultants.

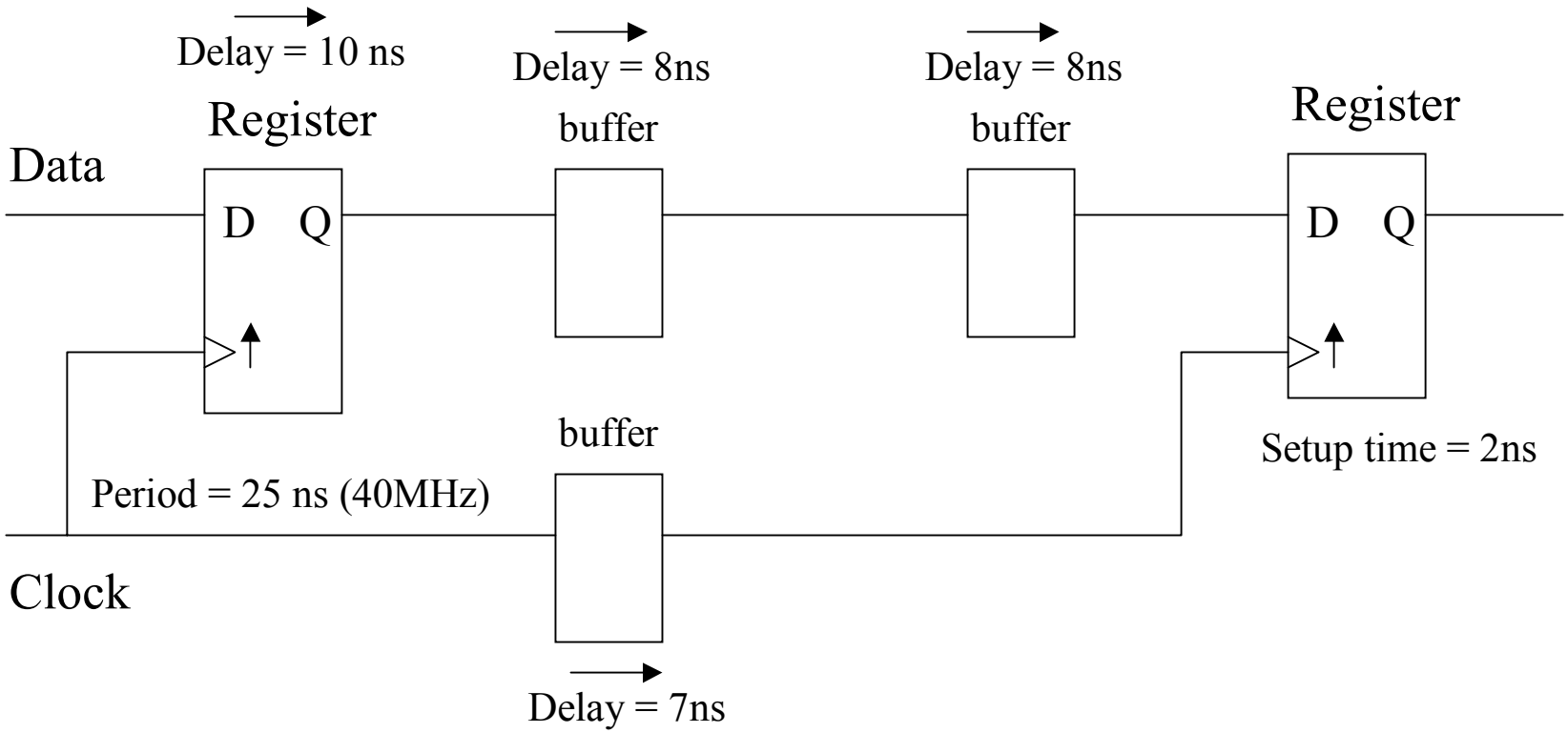
Challenges associated with Simulation

- Deciding which interconnect elements have a significant effect on your digital design.
- Obtaining appropriately accurate models for the significant elements.
- Choosing a cost effective simulation tool that meets your requirements
  - Flexibility
  - Accuracy
  - Integration and Ease of Use

Synchronous Digital Design

- Almost all IC designs internally use conventional synchronous operation.
- Up to the 1990's, most signaling between ICs was based on conventional synchronous operation
  - Directly
  - Indirectly using (read/write) strobes
- Modern designs still have many examples
  - Alternatives require very high transistor count and may have higher power dissipation

Example of Synchronous Design



Slack time = 25 – 10 – 8 – 8 – 2 + 7 = 4ns

Synchronous Delay Constraint

- In the example there is a timing slack of 4 ns.
- We obtained this by assuming the signal paths were ideal.
- When the design is laid out the ideal signals become PCB traces.
  - PCB traces have length
    - they must have delays
  - PCB traces distort the signal
    - delays may be longer than the simple flight time.
- Our circuit will only work if the combined signal delays are less than 4ns.

Primary Characteristics of Traces

- Below 50 MHz the important primary characteristics are:
  - Capacitance
  - Inductance
- Above 50 MHz also consider:
  - Resistive losses in the conductor
    - Roughly increases as the square of frequency
  - Dielectric loss in the PCB substrate
    - Roughly increases in proportion to frequency

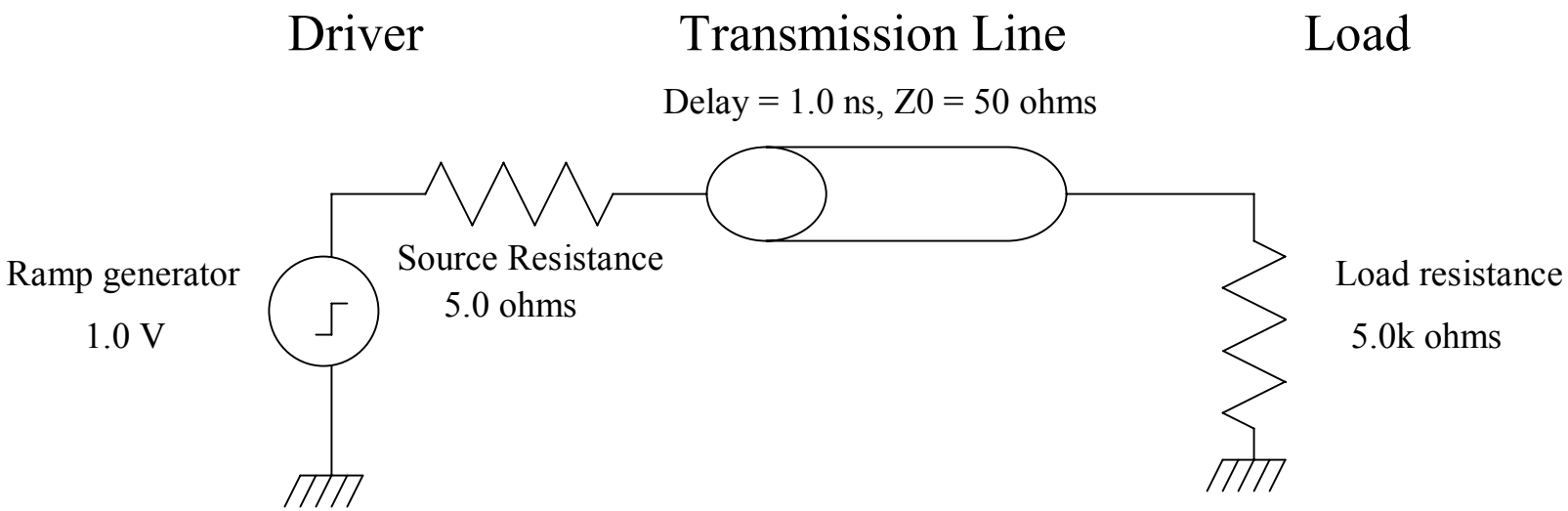
Secondary Characteristics of Traces

- If a trace has delay greater than 1/10th of the edge rate, you should model it as a transmission line.
  - Characteristic Impedance
    - $Z0 = \sqrt{(R + j\omega L) / (G + j\omega C)}$ ω = freq in radians/sec
      $= \sqrt{(L/C)}$ **(if lossless)** j = complex operator
  - Velocity of Propagation
    - $Vp = \sqrt{((R + j\omega L)(G + j\omega C))}$
      $= \sqrt{(LC)}$ **(if lossless)**
- We can calculate the flight time

  Flight time = trace length / velocity of propagation

Signal Reflections

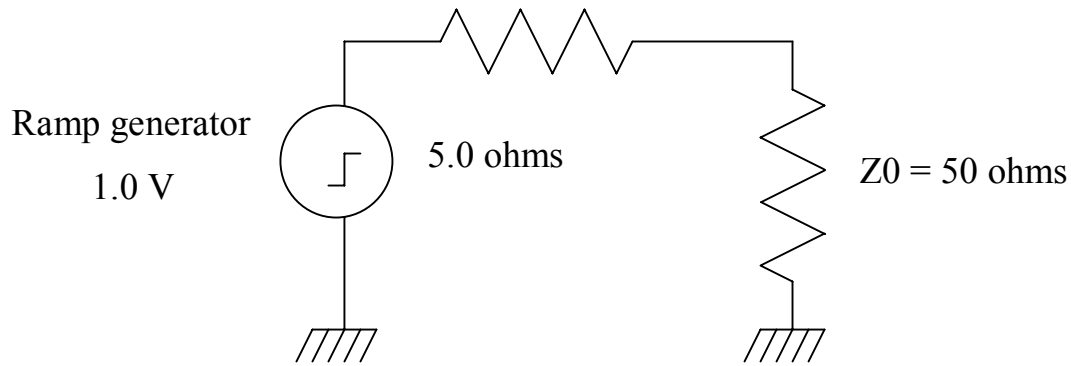
- A Lattice Diagram can be used to do simple analysis of a system with discontinuities.



Initial Signal into Transmission Line

Voltage Divider

$$V_{\text{into transmission line}} = 1.0V * (50 / 50 + 5) = 0.91V$$



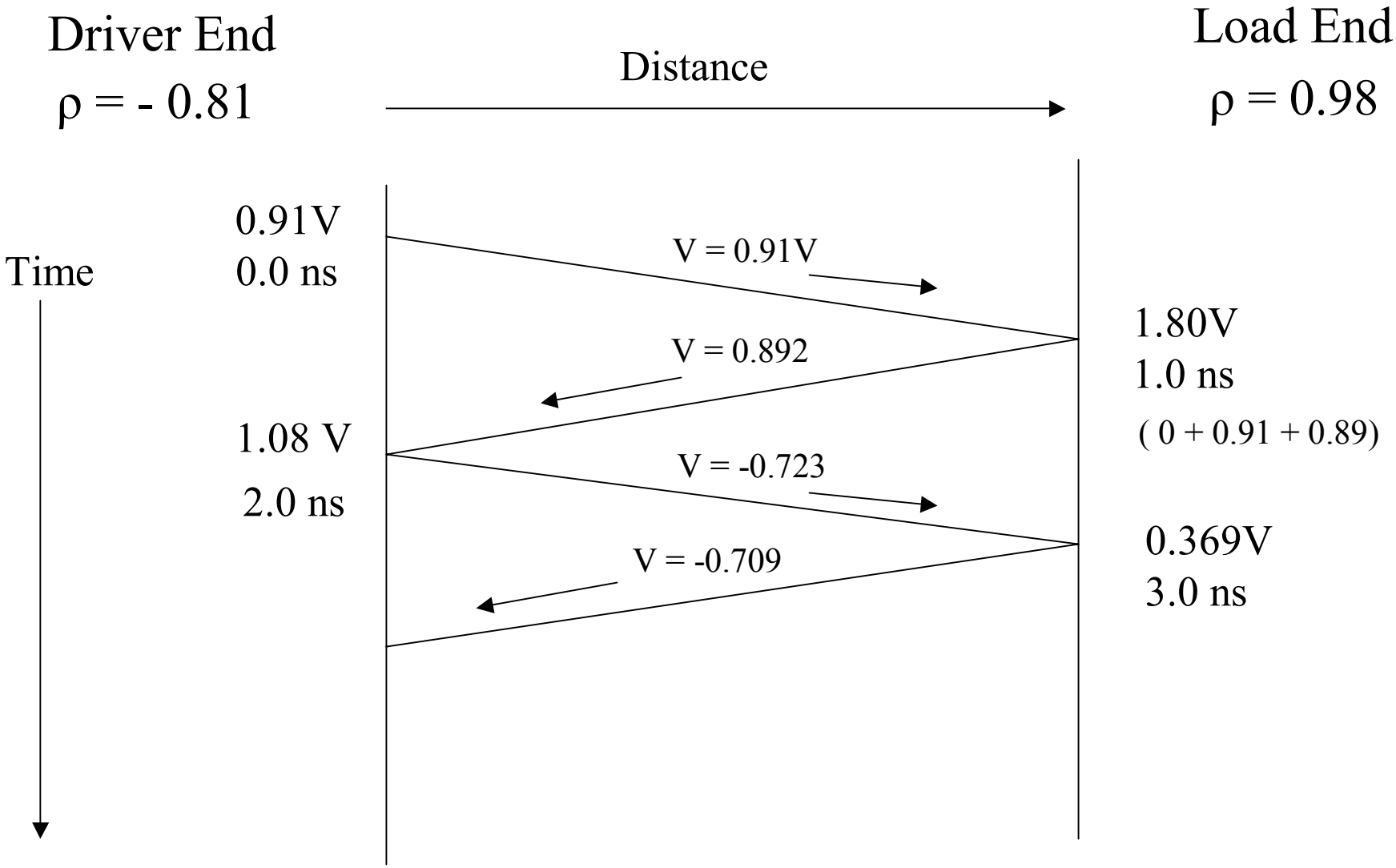
Reflection Coefficients

- Reflection Coefficient ρ (rho)

  $Z_{load} - Z0 \;/\; Z_{load} + Z0$

- Load End $\rho = 5000 - 50 \;/\; 5000 + 50$
  $= 0.98$
- Driver End $\rho = 5 - 50 \;/\; 5 + 50$
  $= -0.81$

Lattice Diagram



$V_{node} = V_{prev} + V_{in} + V_{out}$

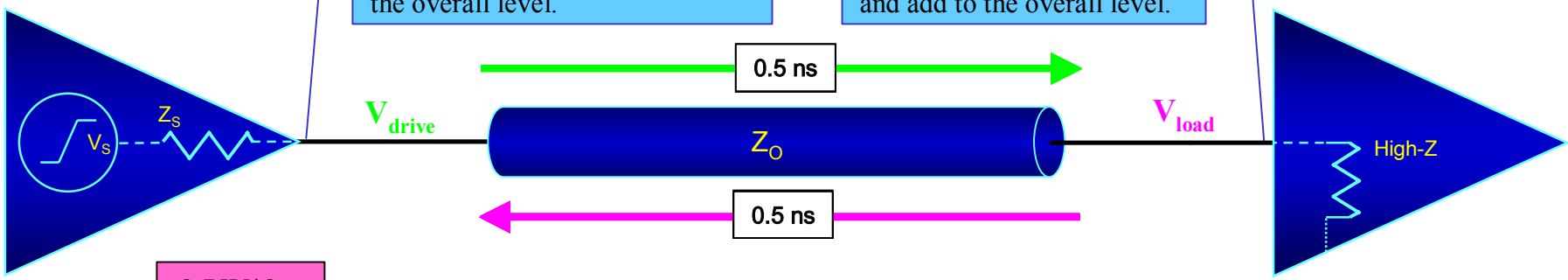
$V_{out} = V_{in} * \rho$

Unterminated Trace

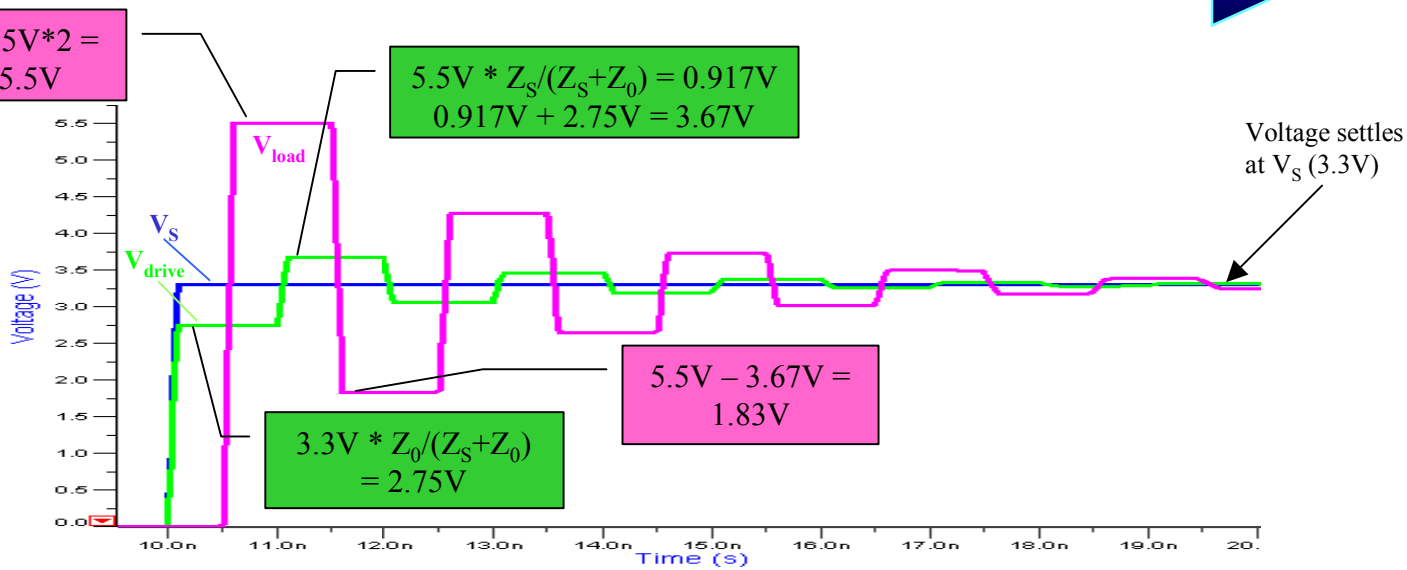
With ideal buffers, no pin parasitics

When a trace terminates into a lower impedance, the reflections have the opposite polarity as the driving signal, and subtract from the overall level.

When a trace terminates into a higher impedance, the reflections have the same polarity as the driving signal, and add to the overall level.



V_S = 3.3V
Z_S = 10 Ohms
Z_0 = 50 Ohms



Special Cases

- R_{load} equals Z0

  $\rho = 0$

  No reflection at load

- R_{source} equals Z0, R_{load} is high impedance

  Initial voltage = half driver swing

  Voltage at load = full driver swing

  No reflection when edge arrives back at driver.

Termination Strategies

- Simple pull up / down resistor or Thevenin network at last load on net
  - Effective resistance matched to Z0 of net
  - Good performance, high power consumption
- Series resistor at driver
  - Resistance equal to Z0 of net minus driver impedance
  - Reduces noise margins or doubles delay
- RC terminator at last load on net
  - Larger physical size, effectiveness is data pattern dependant.

Termination Strategies (2)

- Clamp Diodes
  - Built into many devices.
  - No power penalty
  - Provide termination only outside normal operational range of signal
  - Protect against device latch-up or other catastrophes

Simulation of Signal Reflections

- The analysis in the previous slide made unrealistic assumptions:
  - Single driver and load, one trace segment
    - Real layouts have complex trace topologies
  - Instantaneous voltage jump
    - Real driver have a controlled ramp time
  - Fixed impedance at driver and load
    - Real devices have non-linearity's (including clamp diodes)
- This is where manual analysis needs to give way to automated analysis tools!

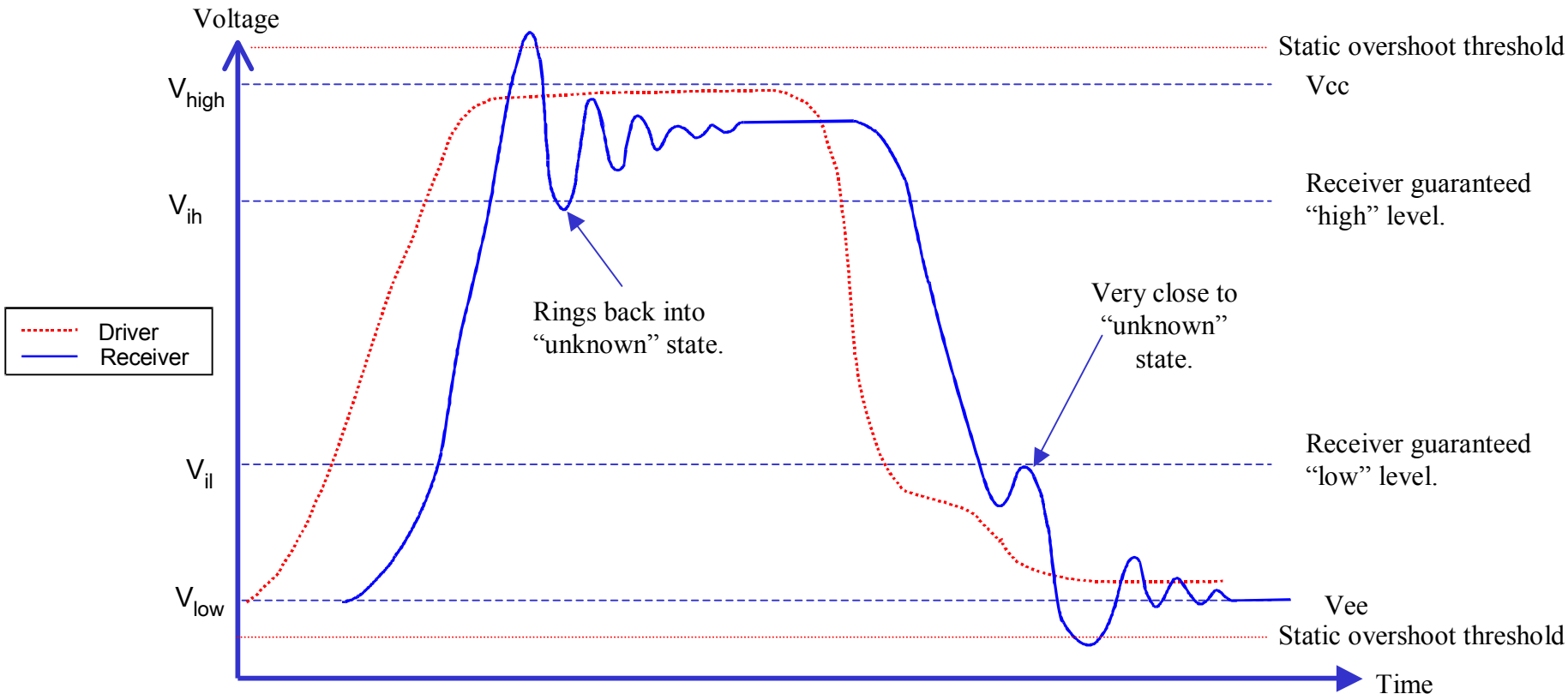
SI Tool Demonstration

- At this point a demonstration of an integrated Signal Integrity Analysis system will take place
- The components that will be demonstrated are:
  - Schematic Capture
    - (Mentor Graphics Inc, Design Capture)
  - PCB Layout Editor
    - (Mentor Graphics Inc, Expedition PCB)
    - Including layer stack editor
  - Interactive SI Analysis in the PCB Editor
    - (Mentor Graphics Inc, Signal Analyzer)
  - Interactive SI What-If Analysis Tool.
    - (Mentor Graphics Inc, Signal Vision)

IBIS Driver and Load Modeling

- Behavioral description of drivers and loads
  - Tables of current versus voltage and for drivers, voltage versus time.
- Can be used by ultra-fast transmission line simulators
- Standard interface
  - SI tools can build a description of the whole net
- Provides switching thresholds and other information needed to make measurements
- Hides IV Vendors Intellectual Property

IBIS Overshoot and Ringback Thresholds



Demonstration of IBIS Models

- At this point, the Mentor Graphics IBIS Librarian will be used to show some of the features of the IBIS modeling language

Problems with pure IBIS models

- Cannot directly model complex behavior
  - Drivers with pre-compensation
  - Slew rate sensitive loads
  - Multi-gigabit compensation filters

SPICE Driver and Load Modeling

- Transistor level models may be derived directly from the IC manufacturer's design process.
- No industry standard interface.
  - The user may have to create their own top level SPICE netlist manually.
- Are missing switching thresholds so measurements cannot be made automatically.
- Generally are slow to simulate
- Functionality must be built out of standard primitives (transistors, diodes etc)

SPICE plus IBIS

- IBIS version 4.1 introduces multi-lingual models
- The IBIS model provides
  - Switching thresholds
  - Mapping of the SPICE model ports to a standard interface.
- The SPICE portion of the model provides
  - Accurate and flexible description of behavior
- Still must use standard primitives and may be slow to simulate!

VHDL-AMS Plus IBIS

- IBIS 4.1 multi-lingual extensions support SPICE, VHDL-AMS and Verilog AMS.
- VHDL-AMS is a powerful industry standard general purpose analog and digital behavioral modeling language.
- It is very easy to create VHDL-AMS models for complex behavior.
- Simulation speed is much faster than with transistor level models.

Crosstalk

- So far we have assumed that we can analyze a net without taking into account it's neighbors
- This is OK for an initial approximation but it does not take into account:
  - Modification of the electrical characteristics of the net under analysis due to its neighbors
  - Crosstalk noise injected from the neighboring nets
    - This affects the delay since we have to wait until we have sufficiently settled beyond the crosstalk noise margin.

Crosstalk Simulation

- You may want to find if a net you are analyzing is subject to a significant level of crosstalk
  - Most tools have physical proximity rule checkers
  - Many tools have crosstalk estimators
  - Crosstalk simulation will provide more accurate values
- If so, you should simulate the net of interest and its neighbors as a coupled system.
  - Some SI tools have an automatic option to do this.

Ground Bounce and Voltage Collapse

- Totem pole drivers are commonly used in standard synchronous designs.
  - When the driver goes from low to high, significant currents are pulled from the power pins.
  - When the driver goes low, significant currents are pushed into the ground pins.
- Power and ground structures have impedance, so there will be losses in these structures.
- IBIS multilingual modeling allows these structures to be conveniently added to existing models

Source Synchronous Designs

- Many times used in wide multi-drop buses
- Data is sent out in fast bursts
- A local clock is sent out in parallel with the data.
- The system generally does not wait until one transition has reached the load before the next transition is sent out.
- Commonly used to achieve bandwidths of 100MB/s to 500MB/s
- Edge times are correspondingly short.

SI Problems at Higher Signaling Speeds

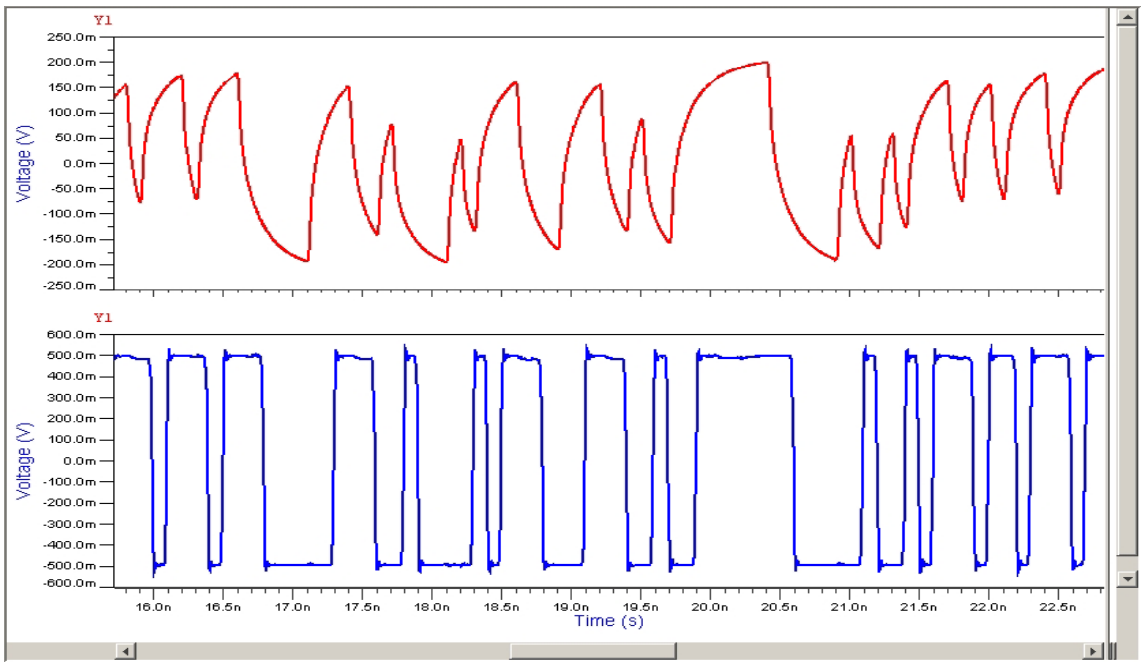
- The settling time of the net may be much longer than the data period
  - Particularly if there are predominantly inductive elements e.g. connectors
  - The response of the net becomes data pattern dependant
  - Frequency domain analysis can help find resonances
  - Waveform are most conveniently displayed in Eye Diagrams form
    - Allows inter-symbol interference to be seen

SI Problems at Higher Signaling Speeds (2)

- Skin and dielectric losses become more significant as edge rates increase.
  - Mandatory to model them in simulations
- Discontinuities in return paths have significant effects.
- Power planes become non-ideal

Eye Diagrams

- Eye Diagrams make it easy to see inter-symbol interference

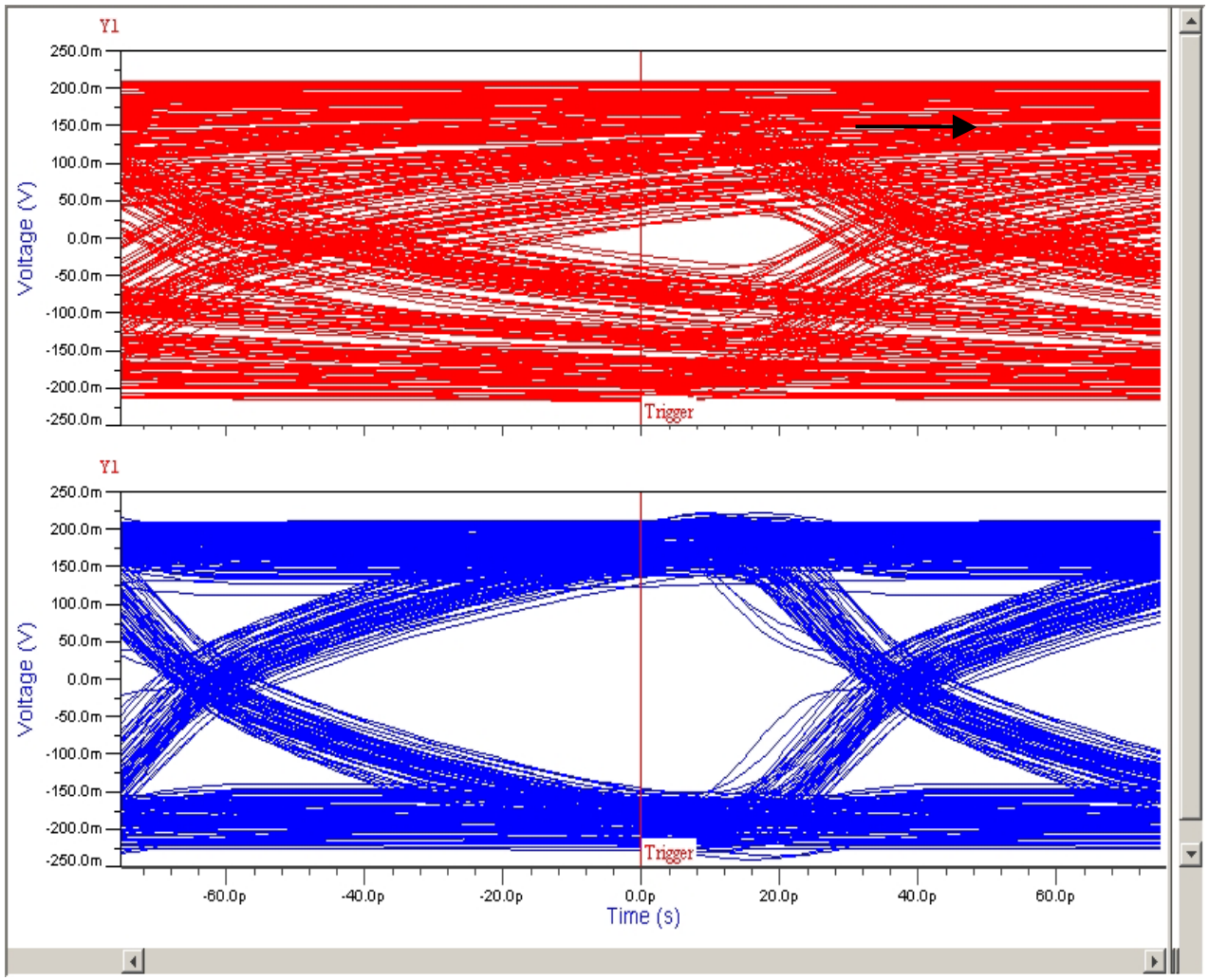


Waveform before equalization

Waveform after equalization

Conventional Waveform Display: Voltage versus Time

Eye Diagrams (2)



Eye diagram without pre-emphasis

Eye diagram with pre-emphasis

Non Ideal Return Paths

- Examples:
  - Conductive shapes or split power planes
  - Vias that change the plane that is used as a return path.
- The return currents need to have a short path otherwise there will be major discontinuities and coupling of noise.
  - Decoupling capacitors may need to be placed to provide this path.
- Need to do 3D modeling
  - Create S-parameter models and incorporate into SI simulation

Power Plane Analysis

- When a driver has a fast edge rate, the current needed to maintain that edge has to come from a local source.
  - On chip decoupling
  - Local portions of the power plane
  - Local decoupling capacitors
- At half the speed of light, the power supply is not local!

Multi-Gigabit Signaling

- Nets are differential
  - Losses are too high for single ended switching thresholds
- Nets are point to point
  - Single driver to single load
- Parallel Termination is usually used
  - May be on chip
- Data is self clocked
  - Clock is recovered using a phase locked loop
  - Eye Diagram diagrams should use the recovered clock.
  - Simple interconnect delays are no longer important

Multi-Gigabit Signaling (2)

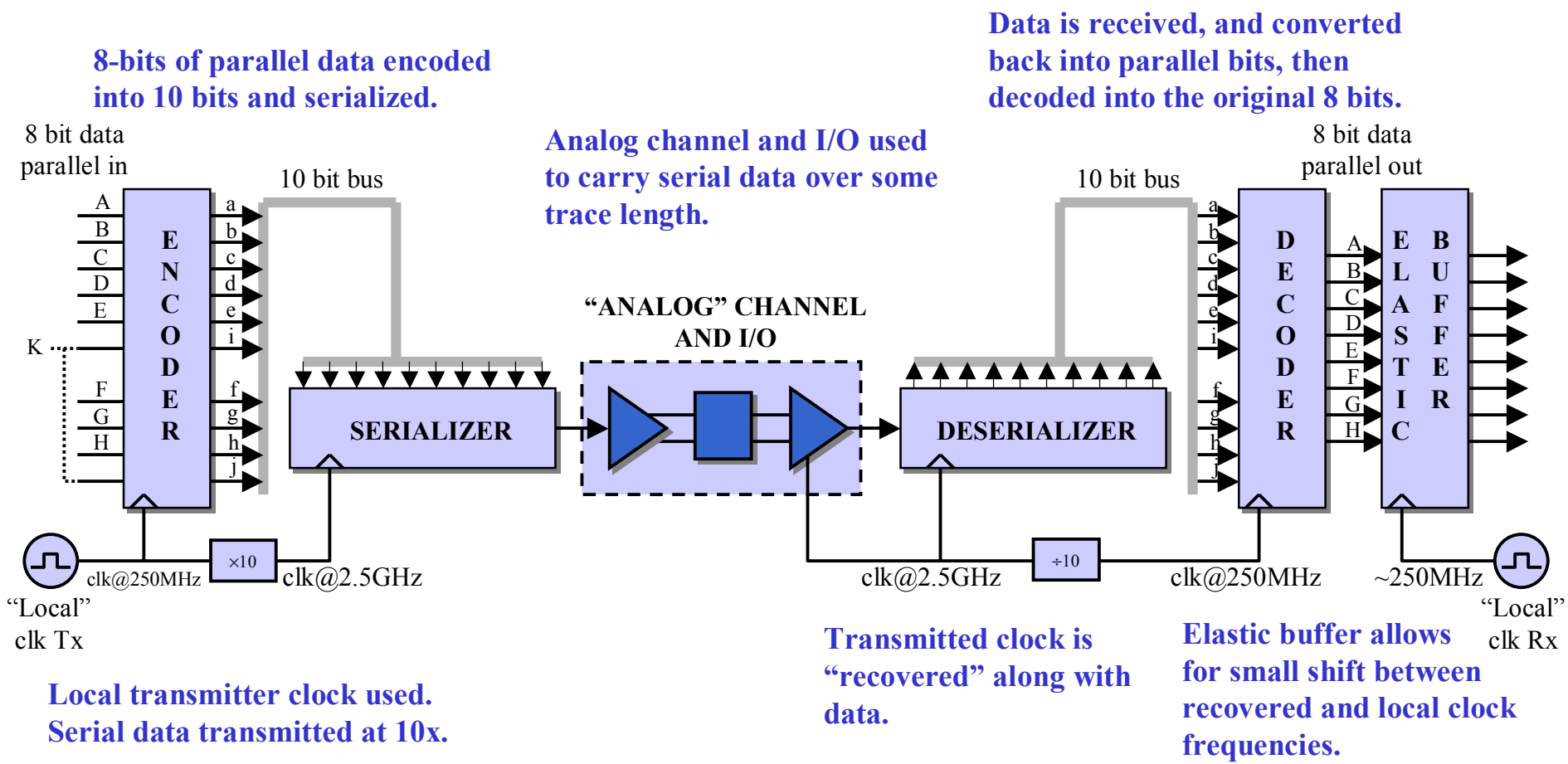
- Many designs use AC coupling
  - include series capacitors
  - Simulator needs to ensure steady state is reached before measurements or display are started
- Driver pre-compensation is commonly used
  - This will increase the crosstalk on neighboring nets
- Equalization filters, located at the receiver, may also be used for long traces.

SI Problems at Multi-Gigabit Speeds

- Discontinuities due to smaller structures become significant.
  - Must include accurate package and connector models
  - Frequently the best models for these elements are in S-parameter format.

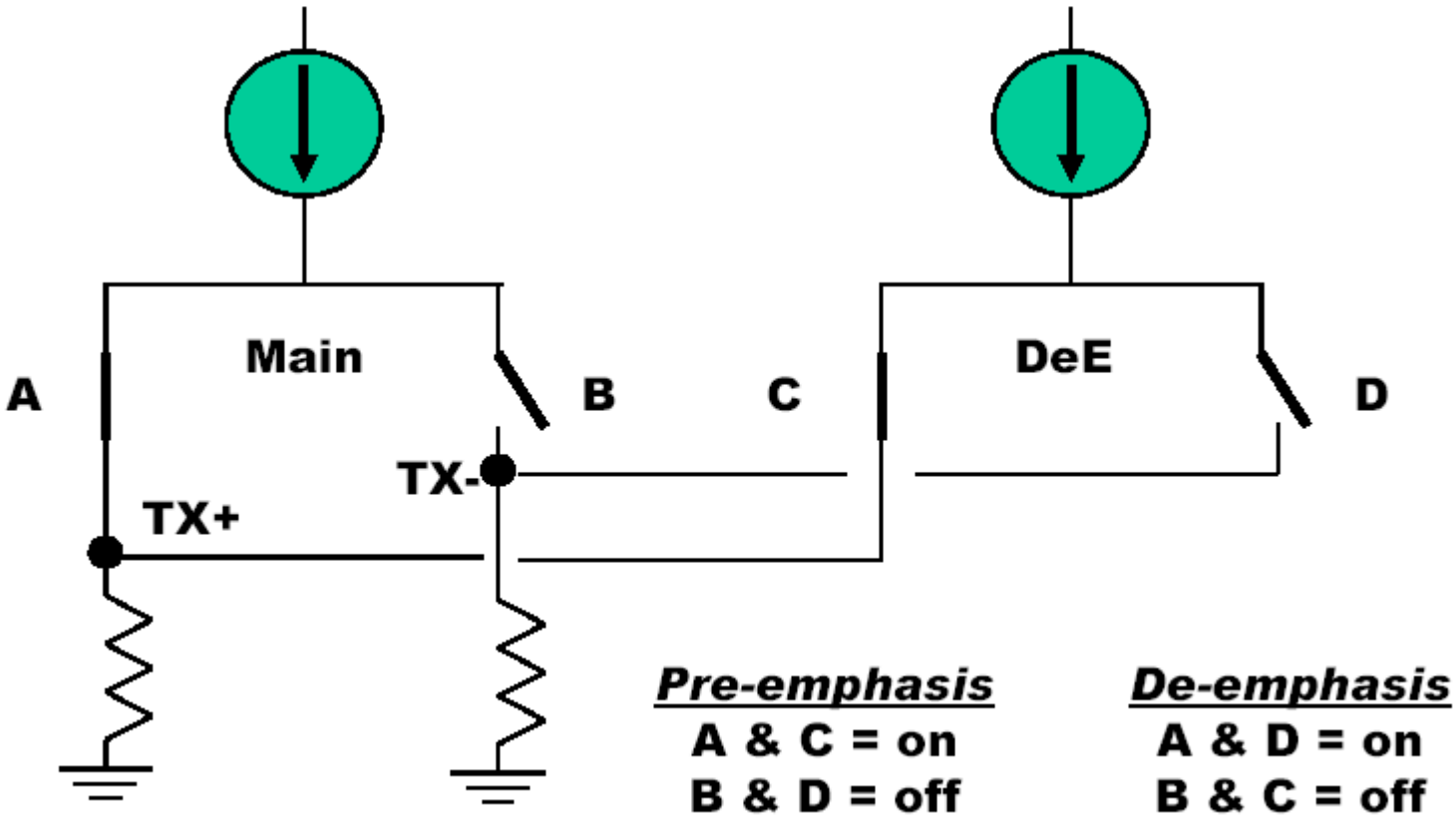
Typical Multi-gigabit Data Link

(with SERDES Data Encoding - e.g. 8b/10b)



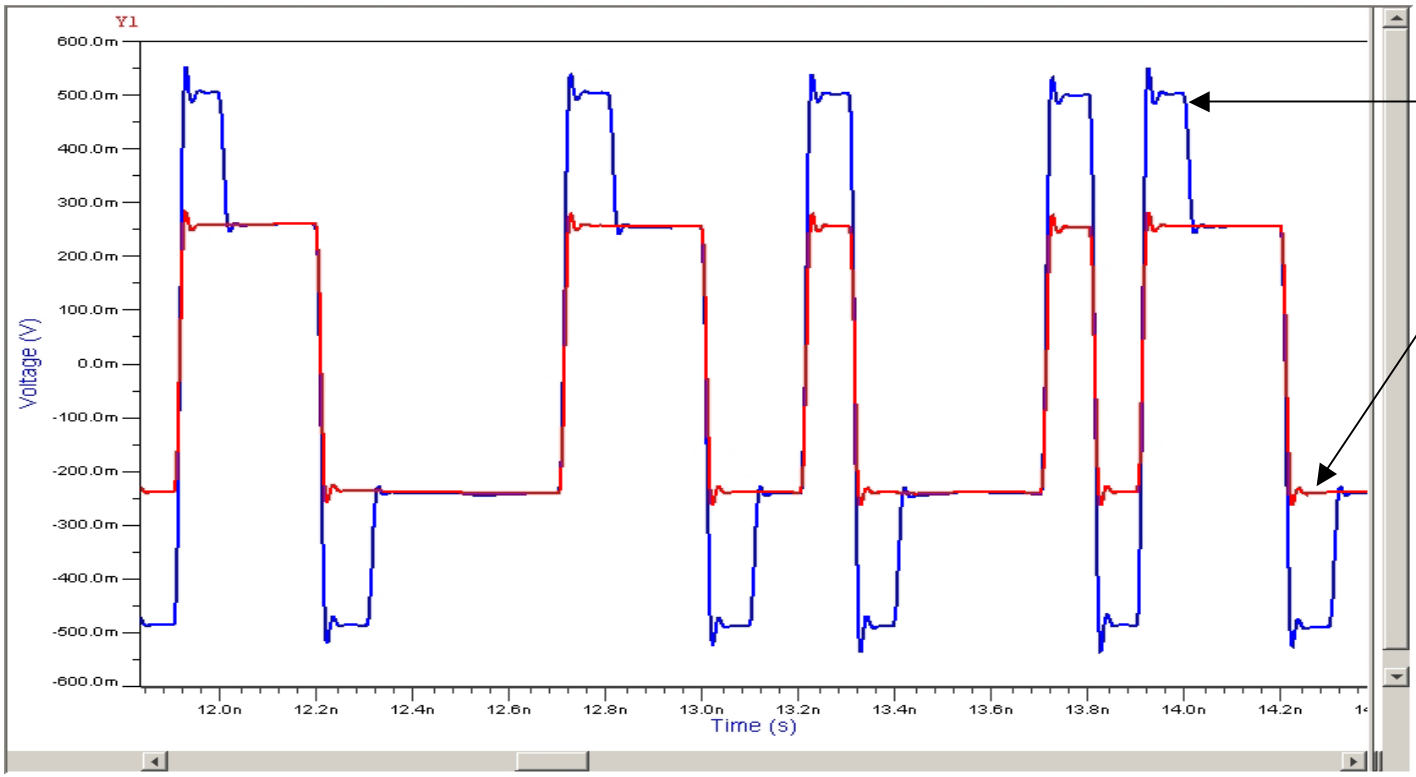
Block diagram of a Pre/De-emphasis buffer

- Pre-emphasis sums both sources through one “leg”
- De-emphasis “steals” current from non-driving leg
- Total current in system always the same



Slide: Courtesy Arpad Muranyi, Michael Mirmak, Intel Corporation (used by permission)

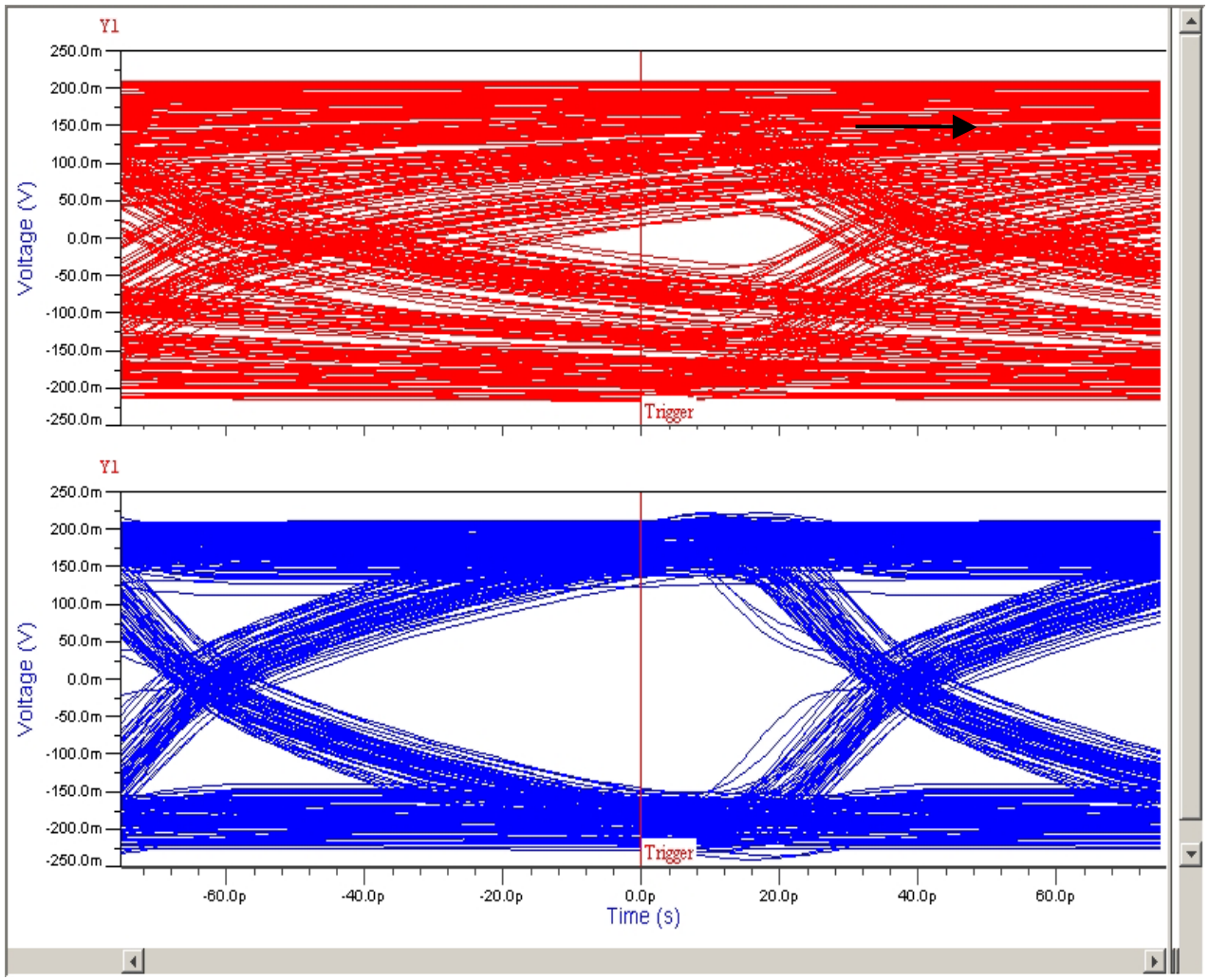
Effect of Pre-compensation on the Driver Waveform



Waveform with pre-emphasis

Waveform without pre-emphasis

Effect of Pre-compensation on the Load Waveform



Eye diagram without pre-emphasis

Eye diagram with pre-emphasis

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