Introduction to Deep Submicron CMOS Device Technology & Its Impact on Circuit Design

Alvin L.S. Loke, Tin Tin Wee & James R. Pfiester
Agilent Technologies, Fort Collins, CO

IEEE Solid-State Circuits Society
December 8, 2004

Outline

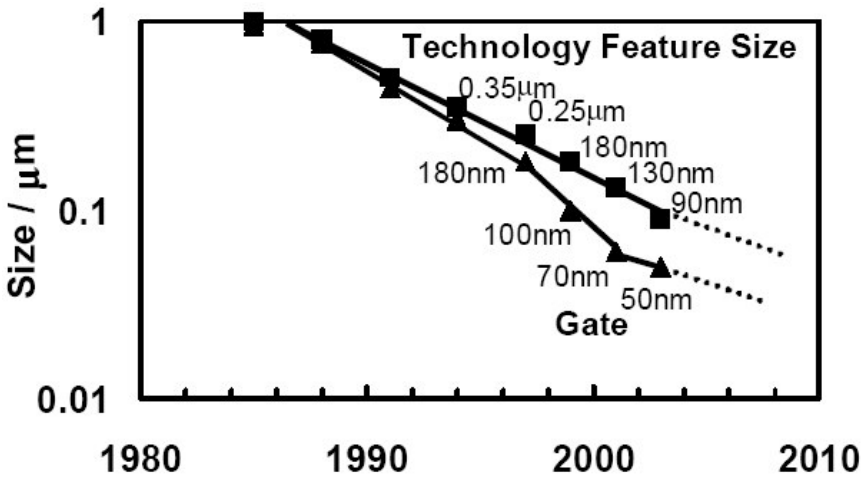
- CMOS Technology Trends
- MOSFET Basics
- Deep Submicron FET Fabrication Sequence
- Enabling Technologies
- Second-Order Consequences
- Dealing with Process Variations in Manufacturing
- Conclusions

Disclaimer

- A proper *introduction* alone would take weeks, let alone a whole semester
- Need to omit lots of nitty-gritty yet important process details
- Hopefully, we'll still learn lots of *cool* device physics ☺ ☺ ☺ ☺ ☺ ☺ ☺ ☺

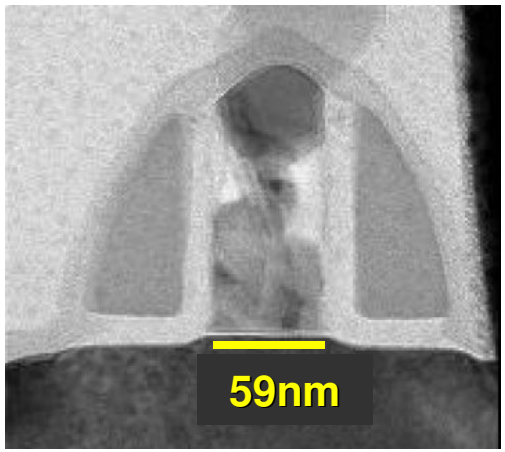
Where is CMOS Technology Today?

- Scaling is still alive & well
  - 130nm now standard fare
  - 90nm already in volume manufacturing
  - 65nm integration tough but not insurmountable
- Some key trends:
  - Aggressive scaling of gate CD (critical dimension)
  - Scaling driven by exclusively by digital circuit needs



Source: Thompson *et al.*, Intel (2002)

90nm Technology



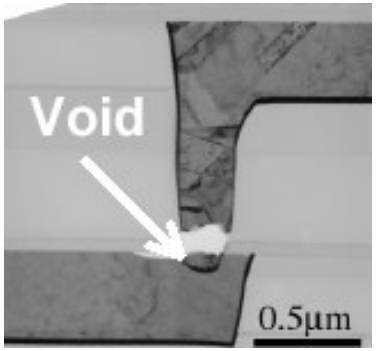
Source: Wu *et al.*, TSMC (2002)

Why Aggressive FET Scaling?

$$t_{delay} \approx \frac{C_{load}\,\Delta V}{I_{FET}}$$

- The road to higher digital performance
  - $C_{load}\downarrow$ → reduce parasitics (largely dominated by interconnect now)
  - $\Delta V \downarrow$ → reduce V_{DD} or logic swing, need for core & I/O FET's
  - $I_{FET} \uparrow$ → all about moving charge quickly
- Hiccups along the way
  - Interconnect scaling much more difficult than anticipated, especially Cu/low-K reliability
  - FET leakage doesn't go well with V_{DD} scaling
- How to beef up I_{FET}?
  - Tweak with μ, C_{ox}, L & V_T

Stress-Induced Voiding



Got redundant vias?

$$I_{dsat} \approx \tfrac{1}{2}\,\mu C_{ox}\,(W/L)\,(V_{GS} - V_T)^2$$

- Technology upgrades not necessarily compatible with analog design

The Most Basic MOS Concept – V_T

- V_T = FET ON voltage, i.e., gate voltage required to form inversion layer connecting source & drain; shorts out back-to-back pn-junctions with substrate

$$V_T = V_{FB} + 2\phi_b + \frac{Q_{dep}}{C_{ox}}$$

depletion charge per unit area
$= qN_A x_{dep} \propto \sqrt{N_A}$ $(x_{dep} \propto 1/\sqrt{N_A})$

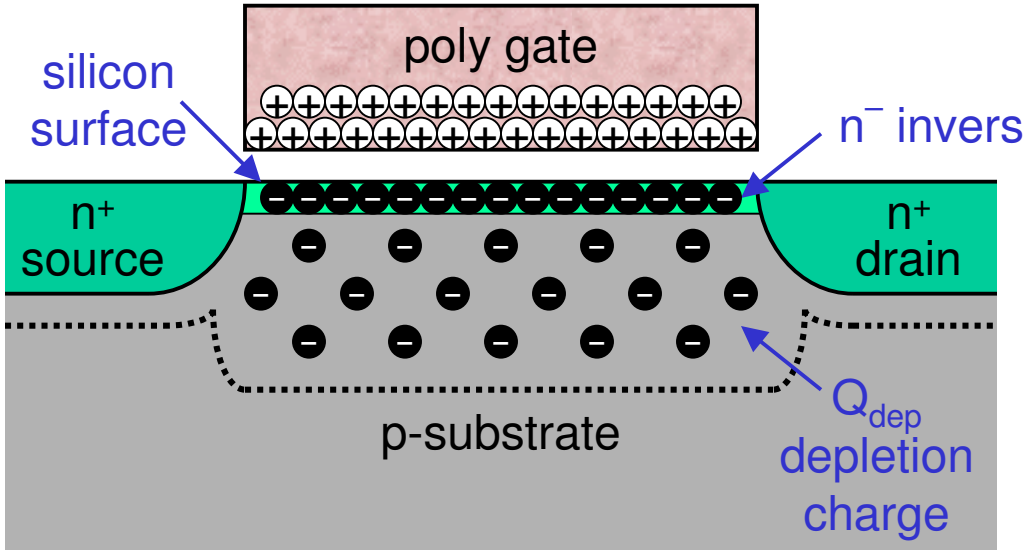
Remember $\nabla \cdot \mathbf{E} = \rho / \varepsilon$?

flatband (offset) voltage due to oxide charge & work function difference

bulk potential

$$\phi_b = \frac{k_B T}{q} \ln \frac{N_A}{n_i}$$

oxide capacitance per unit area = $\varepsilon_{ox} / t_{ox}$

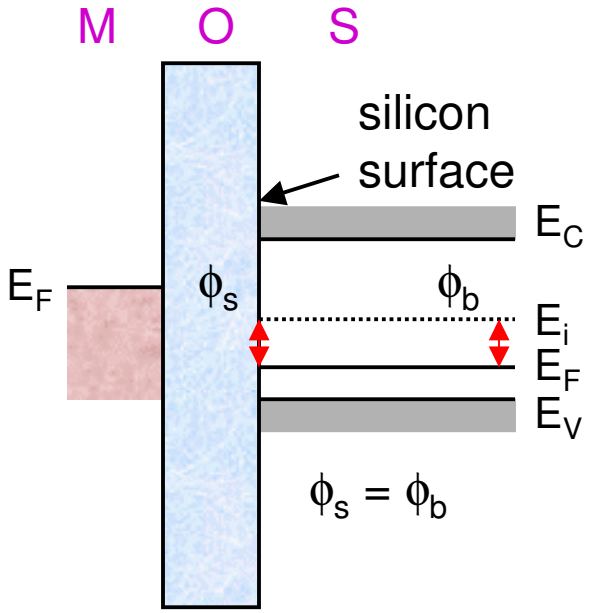


More MOS Fundamentals (Energy Band Diagram)

Formation of Inversion Layer

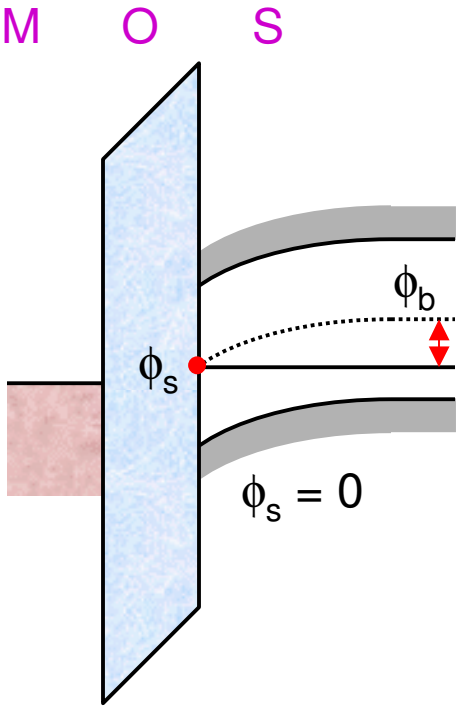
V_T = gate voltage required to reverse doping of silicon surface, i.e., move ϕ_s by $2\phi_b$

flatband
(no field in silicon)



$$\phi_b = \frac{k_B T}{q} \ln \frac{N_A}{n_i}$$

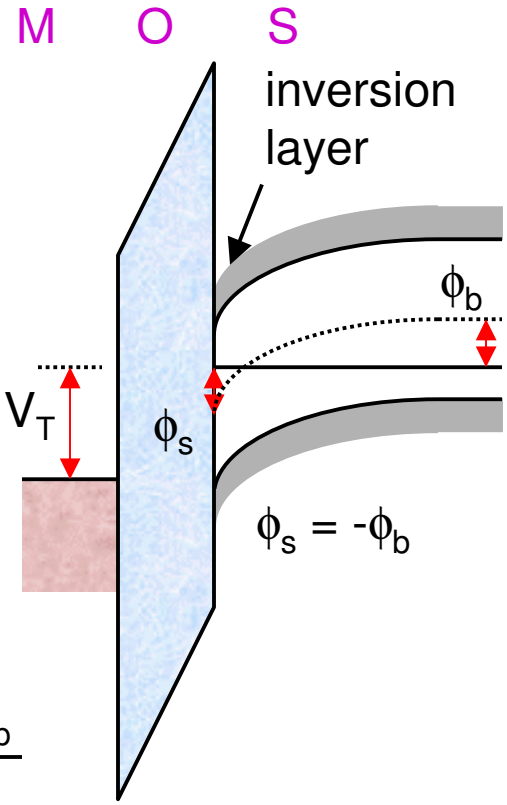
onset of inversion
(surface is undoped)



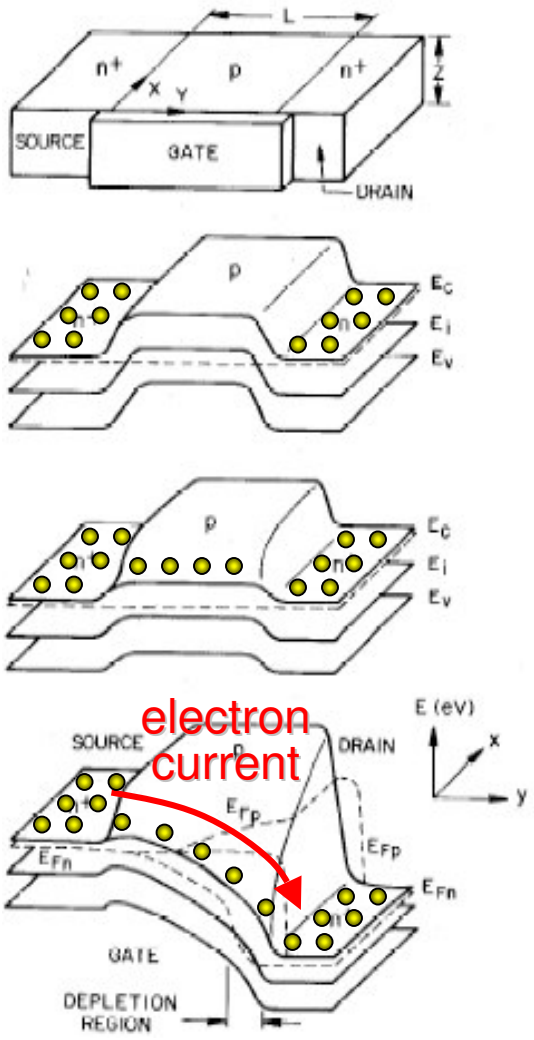
$$V_T = V_{FB} + 2\phi_b + \frac{Q_{dep}}{C_{ox}}$$

offset **bulk drop** **oxide drop**

onset of strong inversion
(V_T condition)



Reintroducing (…drum roll…) the MOSFET



Source: Sze (1981)

$V_{GS} = 0$
$V_{DS} = 0$ (no net current flow)
Large source barrier
(back-to-back diodes)

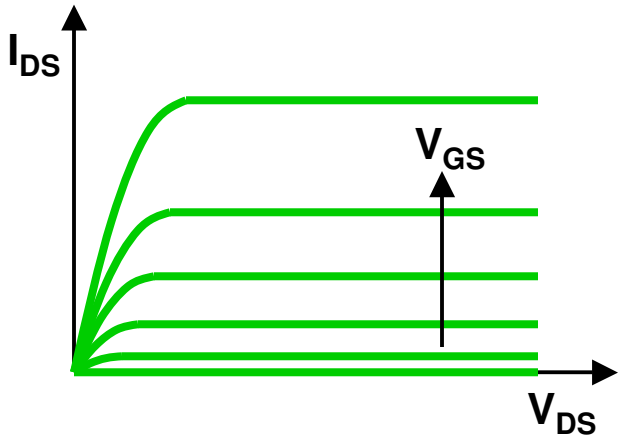
$V_{GS} \approx V_T$
$V_{DS} = 0$ (no net current flow)
Source barrier is lowered
Surface is inverted

$V_{GS} > V_T$
$V_{DS} > 0$ (net source-to-drain current flow)
Carriers easily overcome source barrier
Surface is strongly inverted

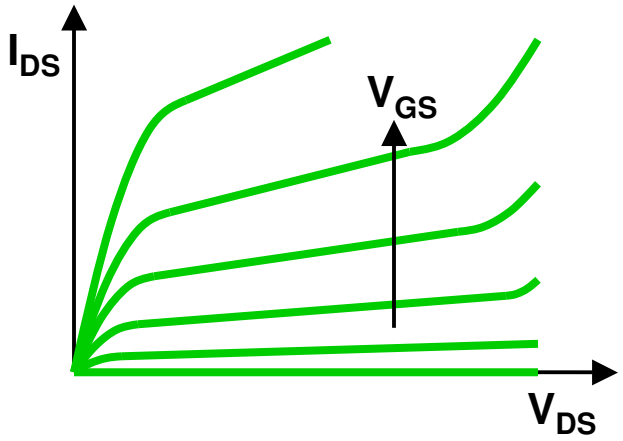
Life's Never So Perfect

Ideal MOSFET = voltage-controlled current source

Ideal

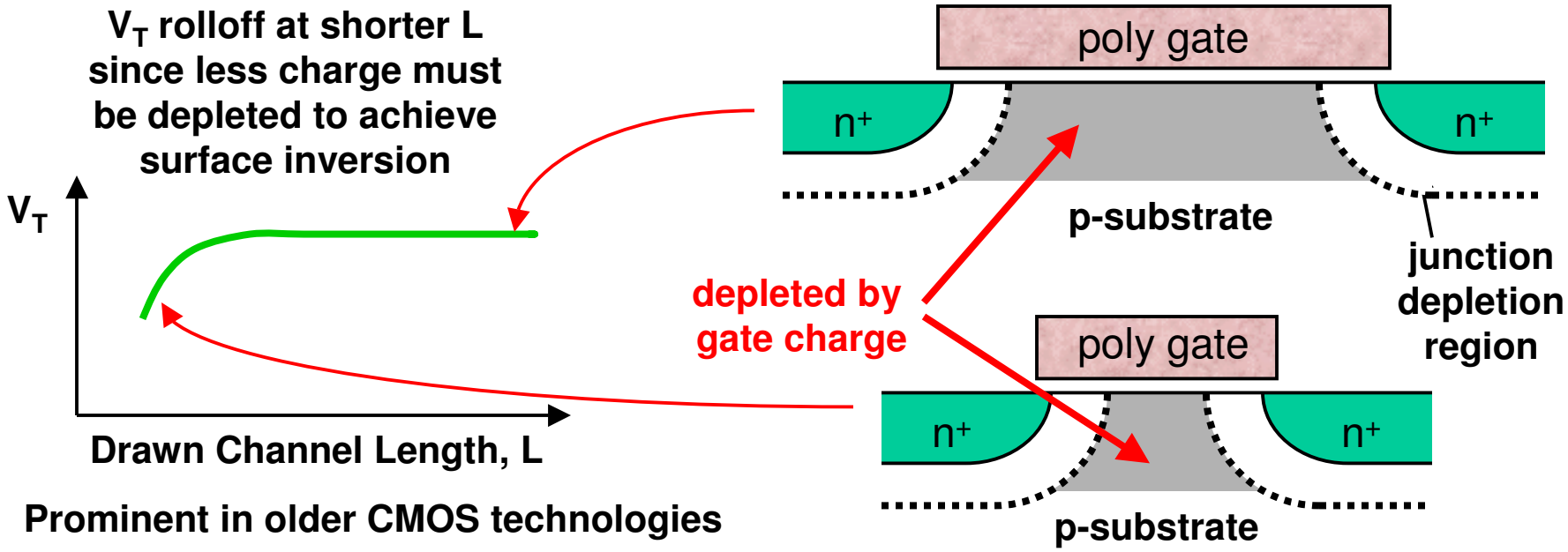


Reality



Now plunging deep into a lot of interesting second-order effects…

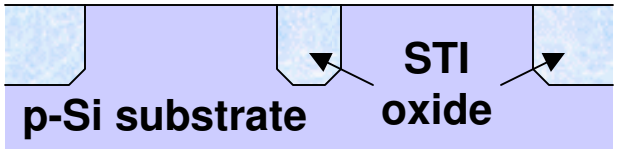
Warp Speed Ahead → Short-Channel Effect (SCE)



- Prominent in older CMOS technologies
- How to minimize SCE?
  - Minimize volume of charge depleted by source/drain junctions
    - Higher substrate doping for thinner junction depletion regions ($x_{dep} \propto 1/\sqrt{N}$)
      - Higher V_T & junction capacitance → not consistent with scaling
    - Shallower source/drain junctions
      - Higher source/drain resistance → smaller drive currents
  - Tighter gate coupling to surface potential
    - Thinner gate oxide of surface potential → direct tunneling leakage
    - Higher K gate dielectrics
- Other SCE problems: large electric fields → carrier v_{sat} & μ degradation

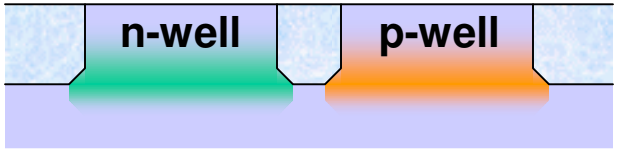
Deep Submicron FET Fabrication Sequence

1



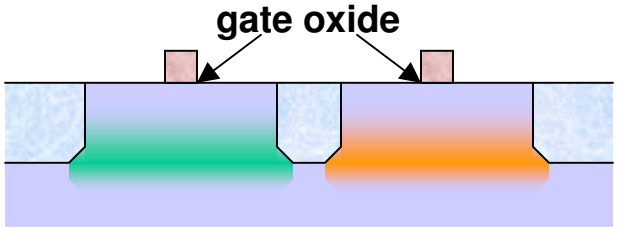
Shallow Trench Isolation

2



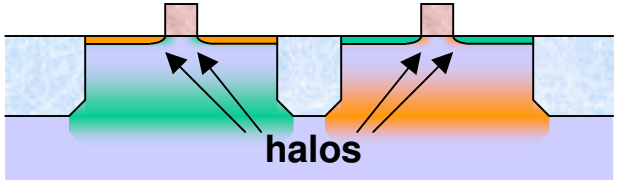
Well Implantation

3



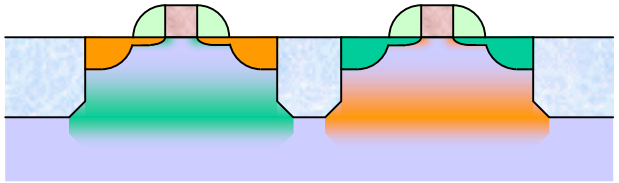
Gate Oxidation &
Poly Definition

4



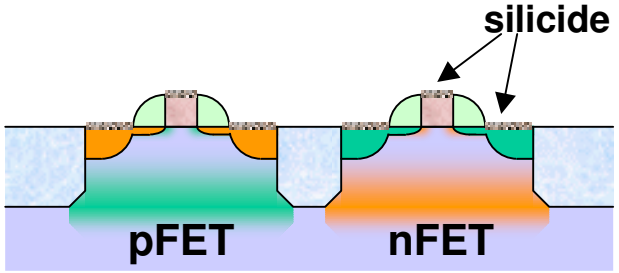
Source/Drain Extension
& Halo Implantation

5



Spacer Formation &
Source/Drain Implantation

6



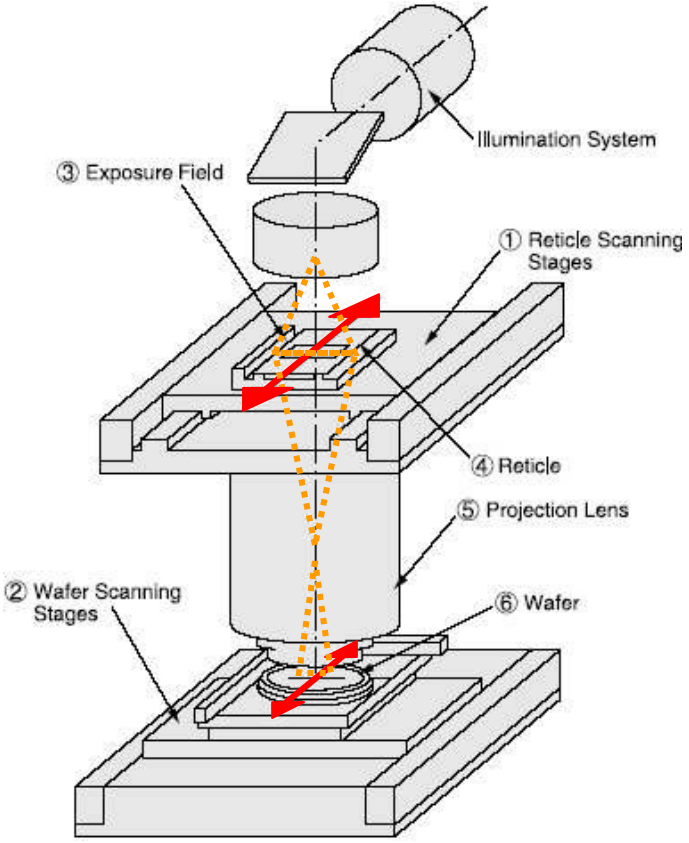
Salicidation

Step-and-Scan Projection Lithography

Rayleigh's Equation: Resolution $\propto \lambda$ / NA

- **Previous generations used G-line (436nm) & I-line (365nm) steppers (refractive 4X-projection optics)**
- **Technology trends**
  - **More aggressive CD's → shorter λ**
  - **Higher NA lenses → $$$**
  - **Larger reticle field sizes → $$$**
- **Step-and-scan enabled resolution & CD control for critical layers beyond 0.35µm node**
  - **Slide reticle & wafer across narrow slit of light**
  - **Aberration-free high-NA optics only required along 1-D but now requires high-precision constant-velocity stages**
  - **Still much cheaper than optics optimized in 2-D**
  - **Rectangular reticle size → shorter edge limited by slit width**
  - **Relatively weak intensity of deep-UV source required development of very sensitive *chemically-amplified* resists for throughput**

Deep-UV *Slit* Source
Excimer Laser
KrF (248nm) or ArF (193nm)



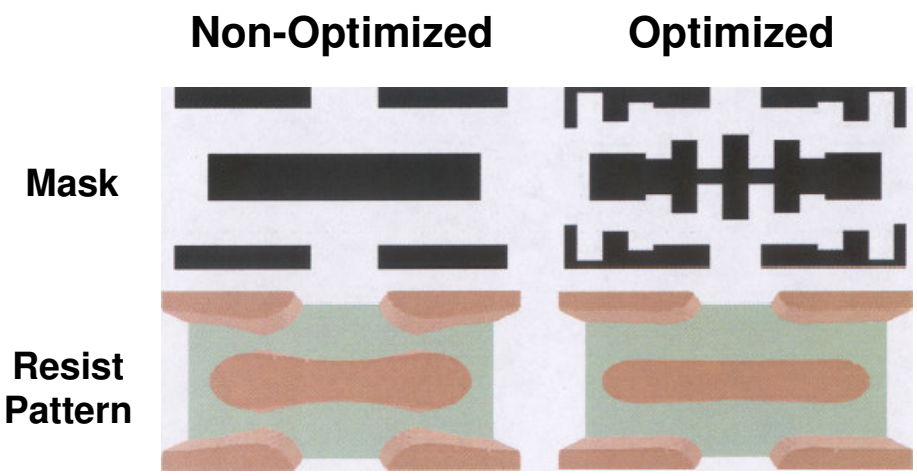
Source: Nikon

More Lithography Tricks

- Sharp features (e.g., corners) are lost because diffraction attenuates & distorts higher spatial frequencies (low-pass optical filtering)
- Compensate for diffraction effects for features much smaller than exposure λ → manage sub-λ constructive & destructive interference
- Software complexity during mask fabrication

Optical Proximity Correction (OPC)

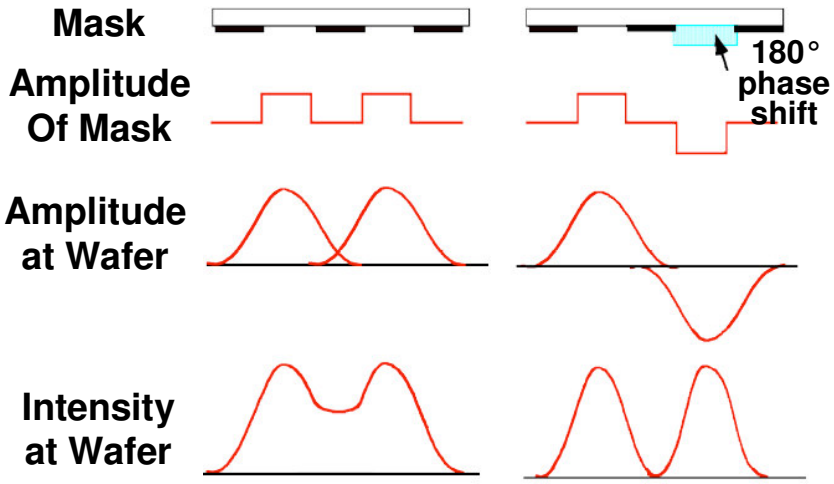
- **Add scattering features to sharpen corners**
- **Used extensively for poly gate definition**



Source: Socha, ASML (2004)

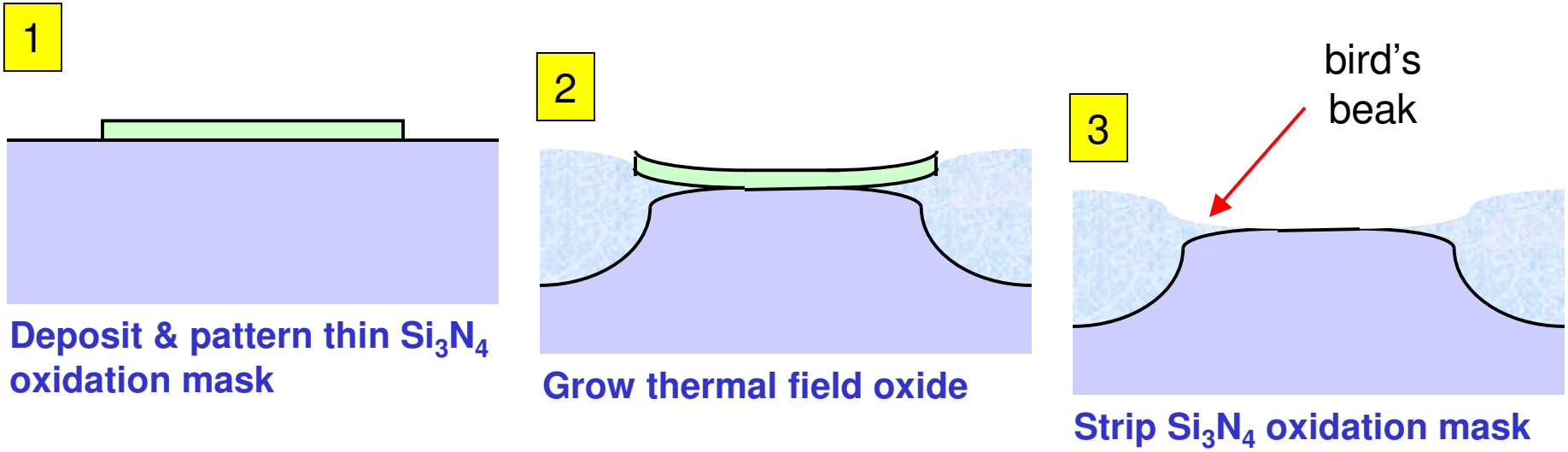
Phase Shift Masking (PSM)

- **Modulate optical path through mask**
- **Used extensively for contacts & vias**
- **Complicated for irregular patterns**



Source: Plummer, Stanford (2004)

Basics of LOCOS Isolation – 0.35µm & Earlier



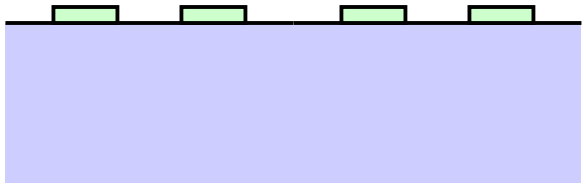
- Industry played lots of tricks to reduce width of bird's beak & make field oxide coplanar with active areas

$$\text{Depth of Focus} \propto \text{Resolution} / \text{NA}$$

- Required very careful understanding of visco-elastic properties of oxide during thermal oxidation
- LOCOS ran out of gas beyond 0.25um

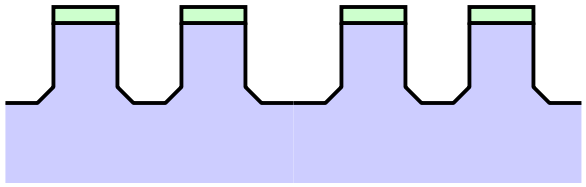
Shallow Trench Isolation (STI) – 0.25 µm & Beyond

1

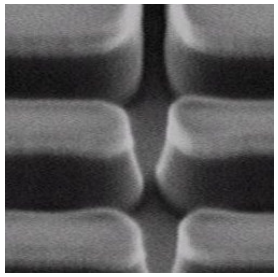


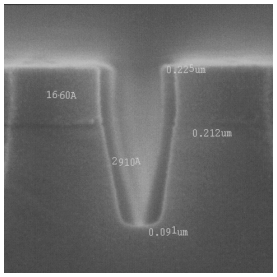
Deposit & pattern thin Si_3N_4 etch mask & polish stop

2

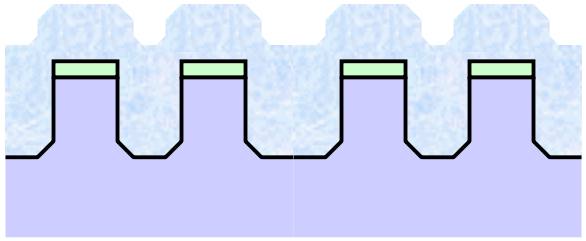


Etch silicon around active area – profile critical to minimize stress



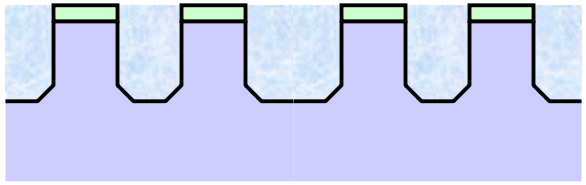


3



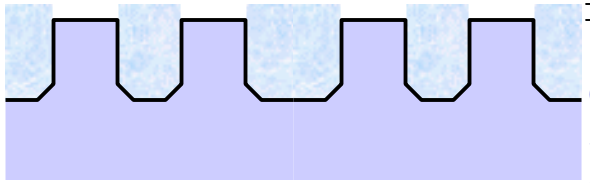
Grow liner SiO_2, then deposit conformal SiO_2 – void-free deposition is critical

4



CMP excess SiO_2

5



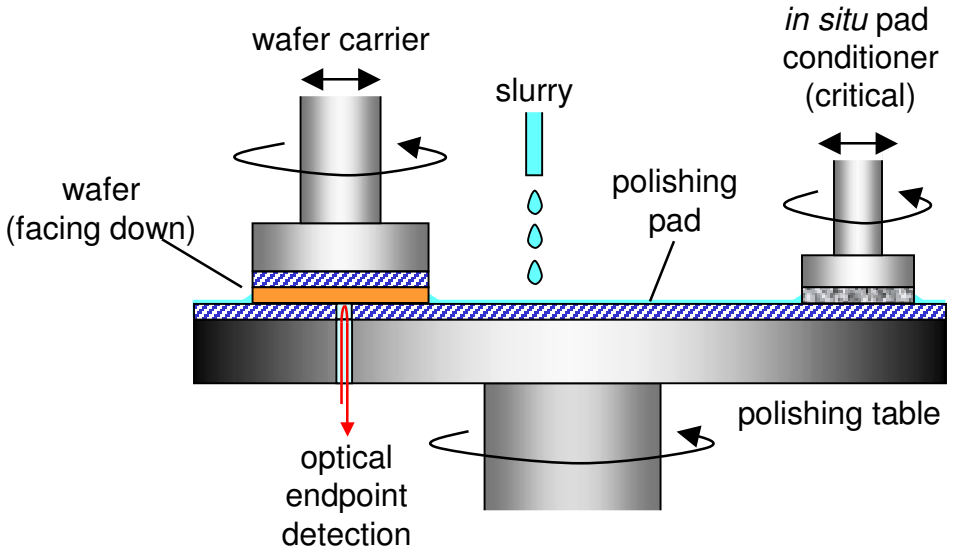
etched away in subsequent oxide cleans

Strip Si_3N_4 polish stop

Advantages over LOCOS technologies

- Reduced active-to-active spacing (no bird's beak)
- Planar surface for gate lithography

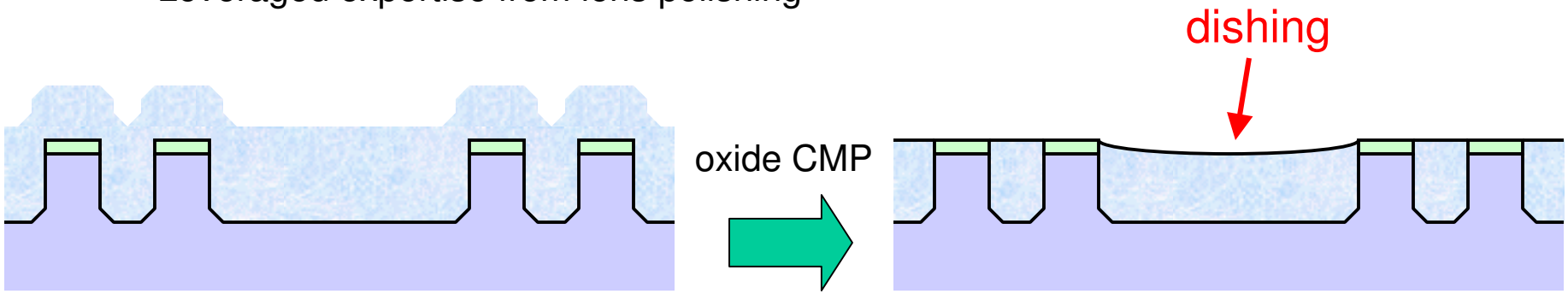
Let's Think a Little Bit More About CMP



- Ideal world for CMP: want *perfect* periodicity of patterns throughout wafer
- Need to throw in dummy features to minimize pattern density variations → optimize planarity
- Polishing pad will flex

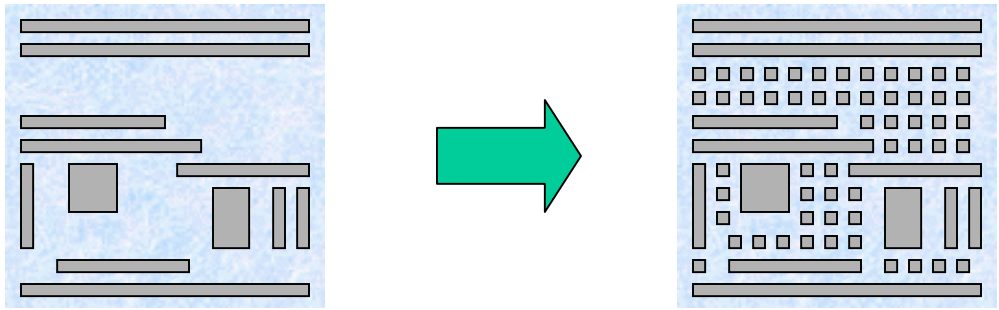
CMP technology pioneered by IBM

- Leveraged expertise from lens polishing

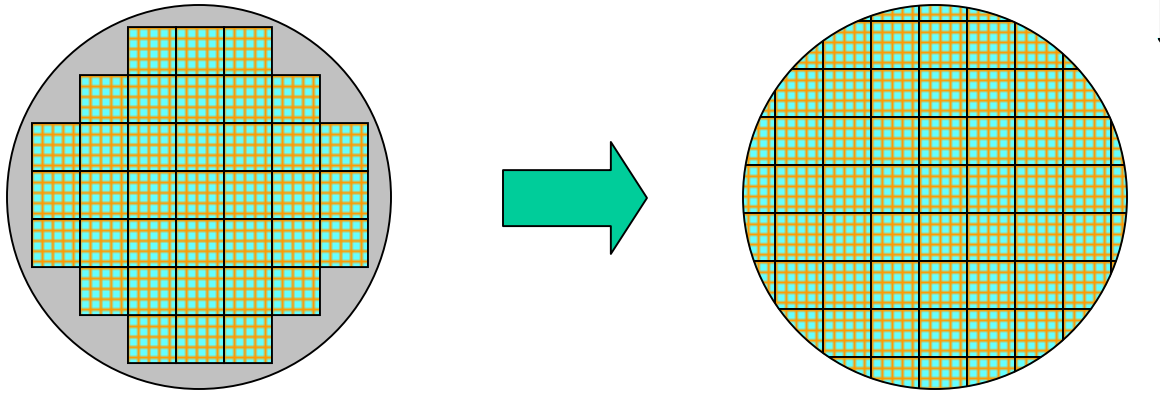


Always Think Dummies in Any CMP Process

- Dummification is key to minimize topography in any CMP process
- Add dummy patterns to open spaces to minimize layout density variations
  → Added design complexity to check layout density & insert dummy patterns

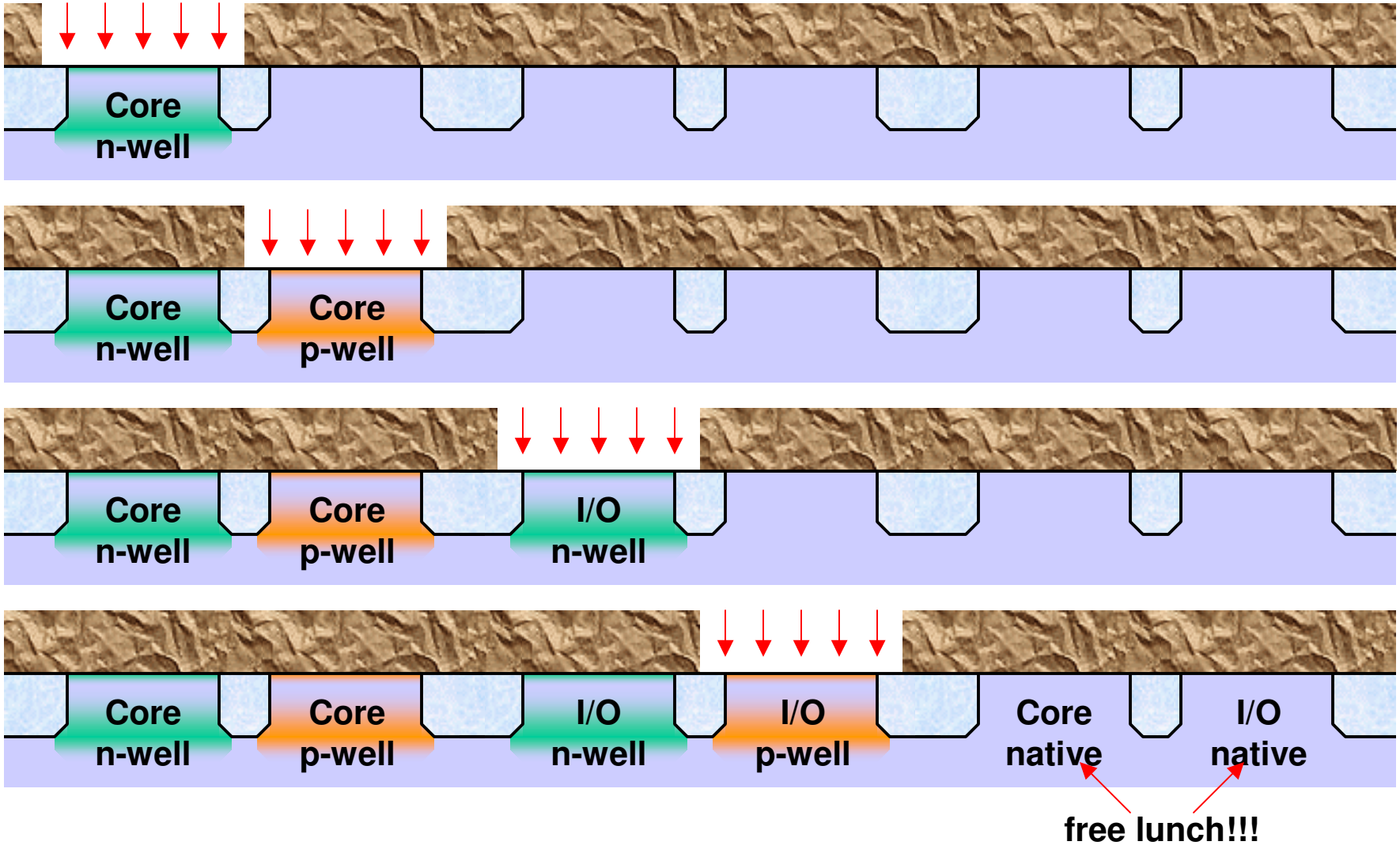


- Also critical to step dummy dies along wafer circumference



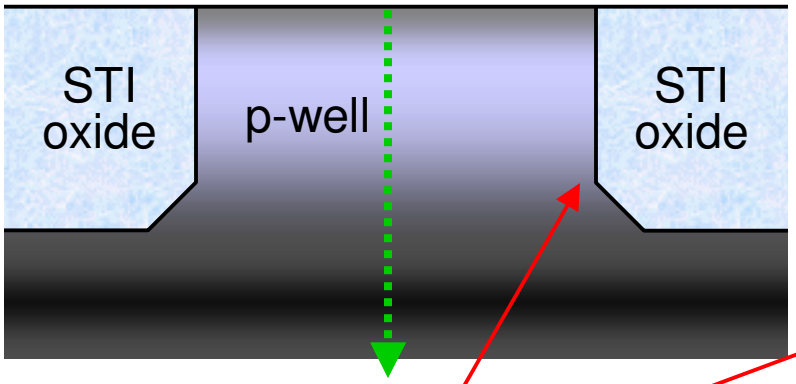
Well Implants – Lots of Transistor Variants

- core vs. I/O FET's, core low-/nom-/high-V_T variants, native vs. implanted

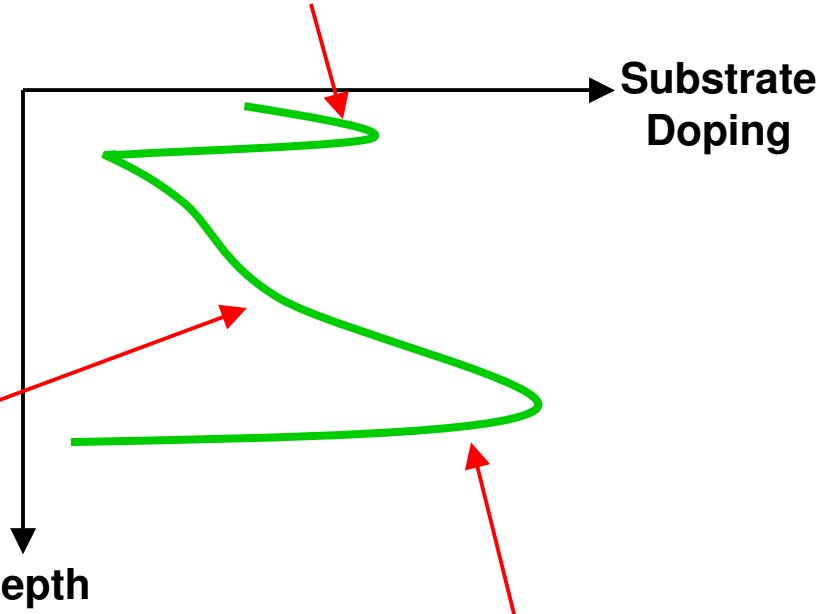


Well Engineering

Retrograded well dopant profile
(implants before poly deposition)



Shallow & steep surface channel implant
- V_T control
- Slow diffusers critical (Ga, Sb)



Deeper subsurface implant
- Extra dopants to prevent subsurface punchthrough under halos
- Prevent parasitic channel formation on active sidewall beneath source/drain
- Faster diffusers OK (B, As/P)

Very deep high-dose implant
- Latchup prevention
- Noise immunity
- Faster diffusers OK (B, As/P)

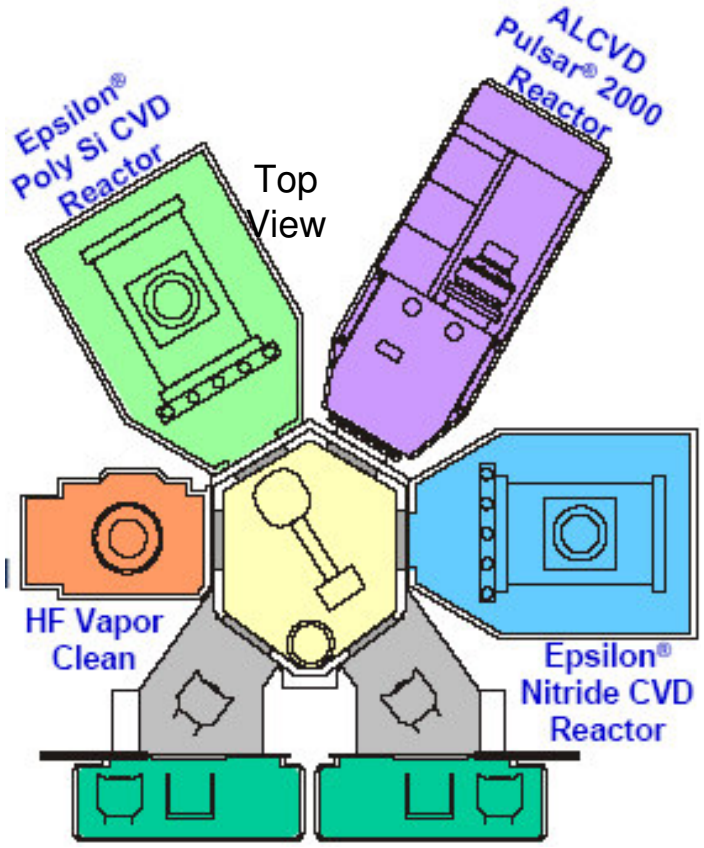
Implant order matters to prevent ion channeling, especially for the shallow implant

Gate Oxidation

- Need two gate oxide t_{ox}'s – thin for core FET's & thick for I/O FET's
  - Grow 1st oxide, strip oxide for core FET's, grow 2nd oxide
- Gate oxide is really made of silicon oxynitride (SiO_xN_y)
  - N content prevents boron penetration from p+ poly to channel in pFET's
  - Side benefit – increased ε_{ox}

Subroutine on Equipment Technology

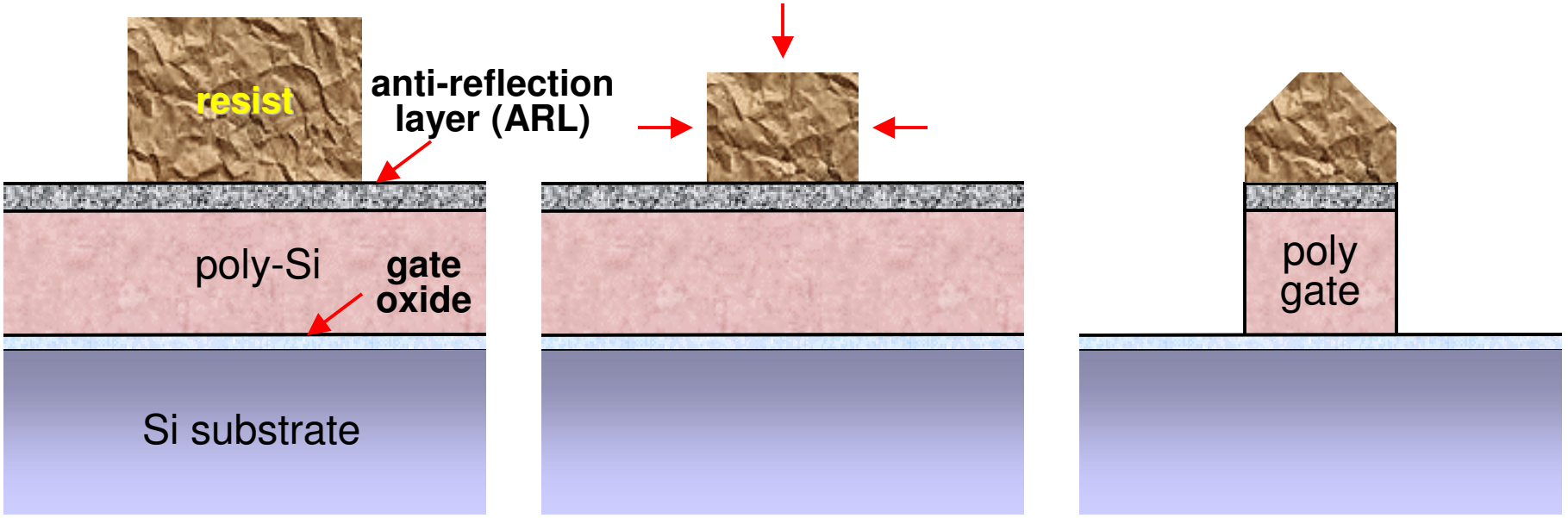
- Gate oxide no longer furnace grown
- Multi-chamber *cluster tools* now ubiquitous
- Pre-oxidation clean, gate oxidation & poly/ARL deposition performed in separate chambers without breaking vacuum
- Better thickness & film compositional control (native SiO_2 grows instantly when exposed to air)
- Fast – minutes-seconds per wafer vs. hours per wafer batch



Source: Maex, IMEC (2002)

Poly Gate Definition

- Gate CD way smaller than lithography capability, even with mask tricks



1 Pattern resist

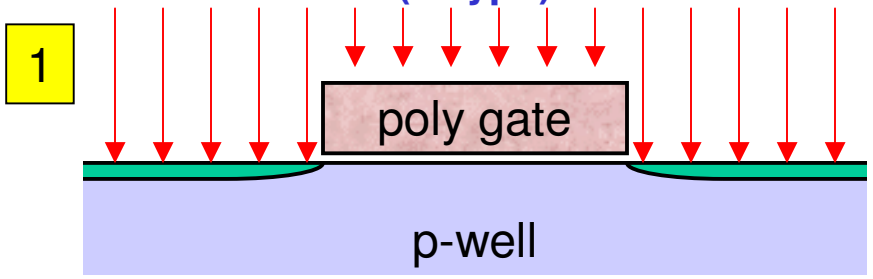
2 Trim resist (oxygen ash)

3 Etch gate stack

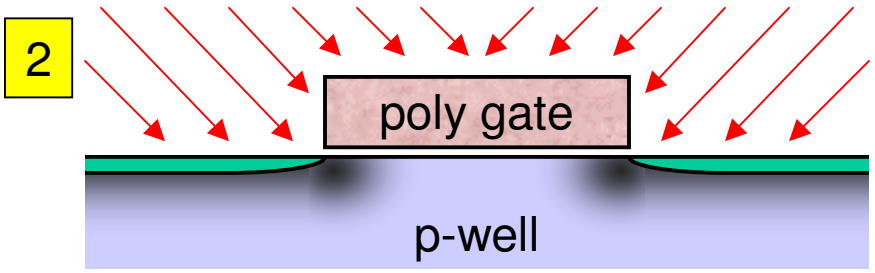
- *Process control is everything* – resist & poly etch chamber conditioning is critical (lesson to remember: don't clean those residues in tea cups or woks)
- Way to get smaller CD's to trim more (requires tighter control)
- Dummification also necessary for poly mask

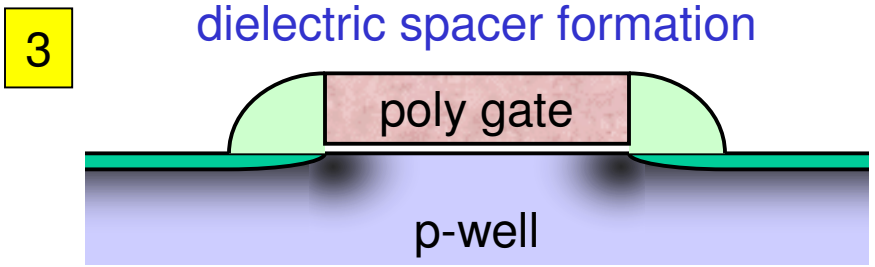
Source/Drain & Channel Engineering

self-aligned source/drain extension implant (n-type)

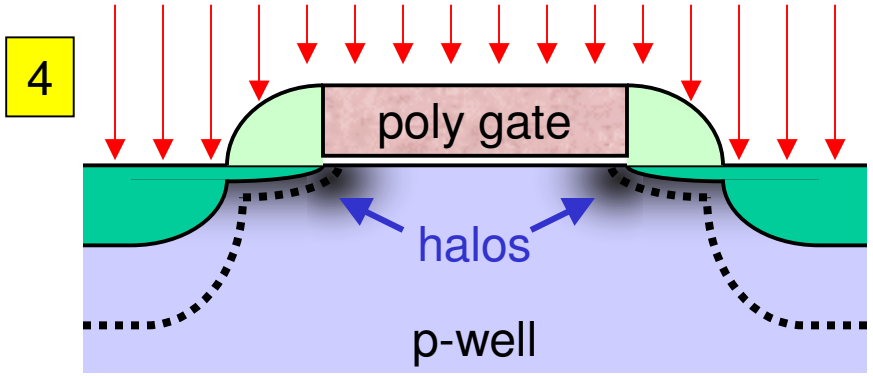


self-aligned high-tilt halo/pocket implant (p-type)





self-aligned source/drain implant (n-type)



Resulting structure has:

- **Smaller SCE**
- **Shallow junction where needed most**
- **Low junction capacitance**

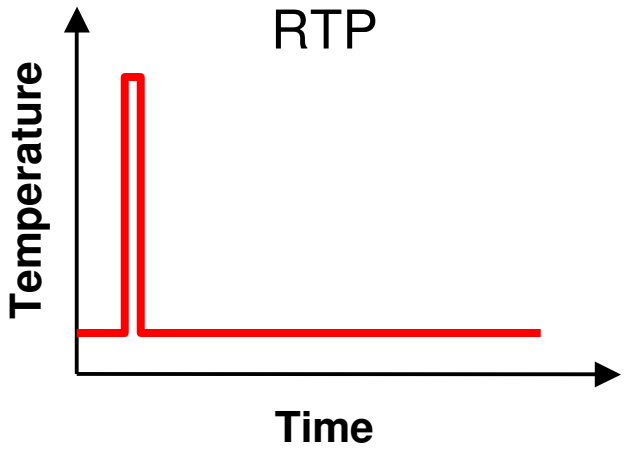
Not to be confused with LDD's in I/O FET's

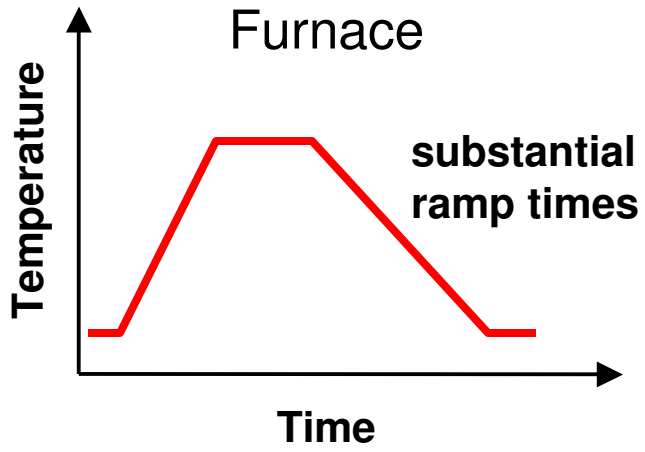
- **Same process with spacers but lightly doped drain (LDD) is used for minimizing peak *E* fields that cause hot carriers & breakdown**
- **Extensions need to be heavily doped to minimize series resistance**

Different halo & extension/LDD implants for each FET variant

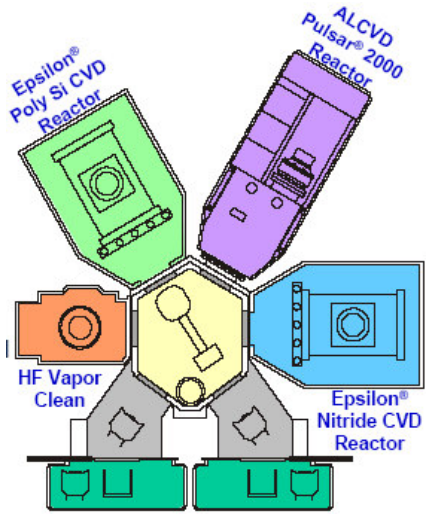
Rapid Thermal Processing (RTP)

Wasabi vs. Curry





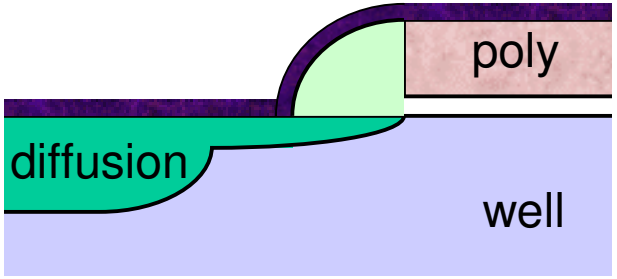
- Initially developed for short anneals
  - Impossible to control short thermal cycles in furnaces
  - Want minimum diffusion for shallow & abrupt junctions
- Process steps:
  - Annealing → repair implant damage
  - Oxidation → gate oxide
  - Nitridation → spacers, ARL
  - Poly deposition → gate
- RTP in single-wafer multi-chamber cluster tools



Self-Aligned Silicidation (Salicidation)

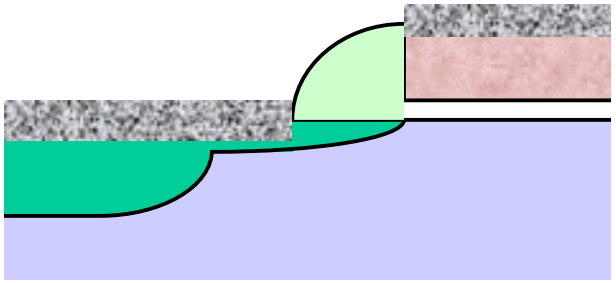
- **Need to reduce poly & diffusion R_s, otherwise get severe IFET degradation due to voltage drops from contacts to intrinsic FET (source degeneration)**

1



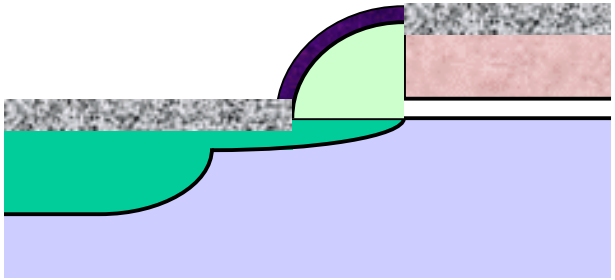
Deposit sicilide metal (Ti, Co, Ni)

3



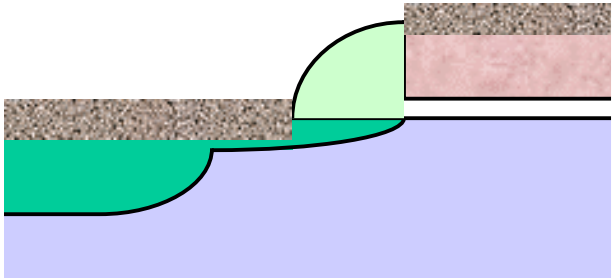
Strip unreacted metal

2



RTA1 (low temperature)
Selective **formation of metal silicide from direct metal reaction with Si**

4

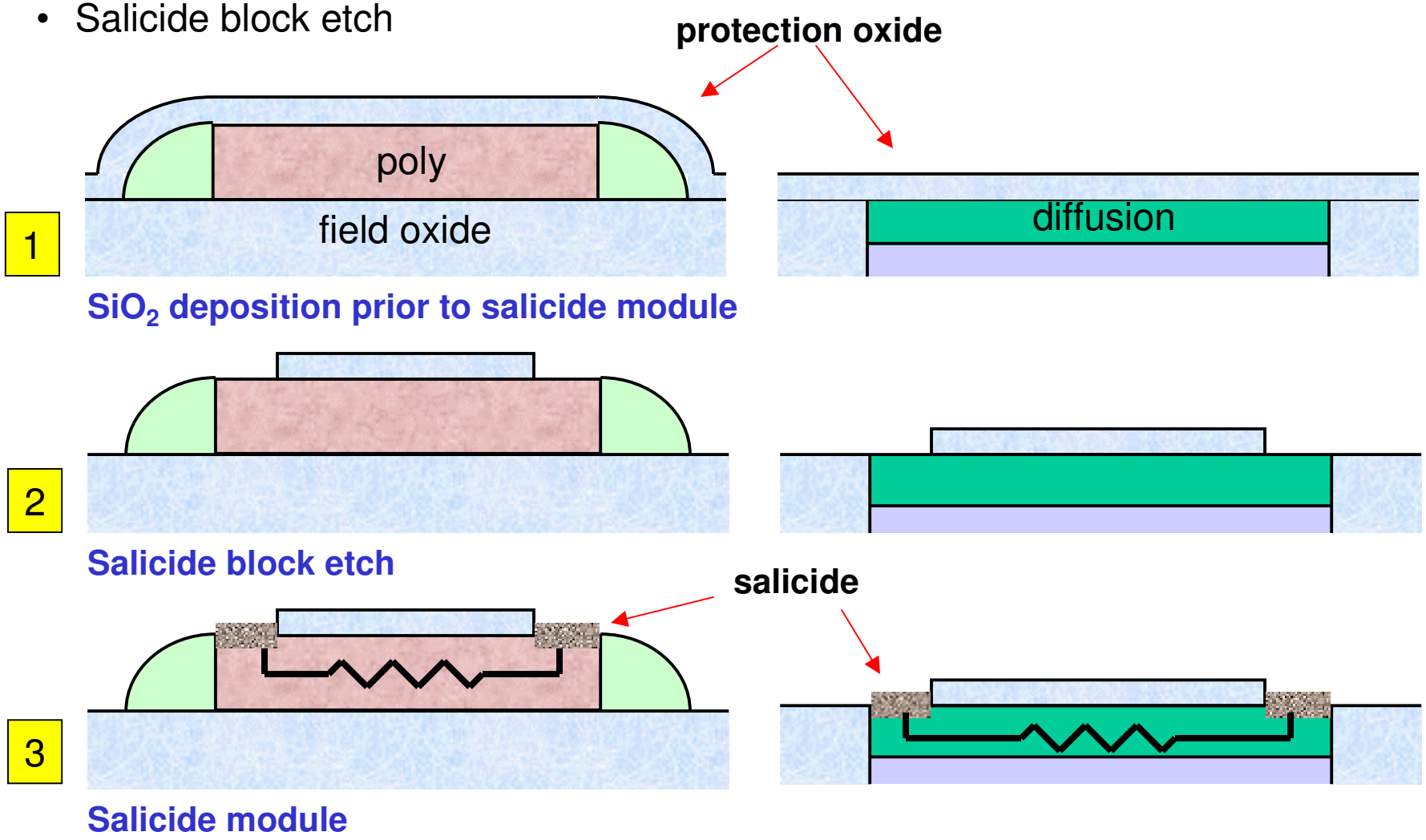


RTA2 (high temperature)
Transforms metal silicide into low-ρ phase by consuming more Si

- Selectivity degraded at RTA2, i.e., metal over SiO_2 & Si_3N_4 will form silicide
- Technology progression: $TiSi_x$ → $CoSi_x$ → $NiSi_x$
  - Scaling requires smaller silicide grain size to minimize R_s variations

Making Cheap Resistors

- Only one extra mask can buy you unsalicided poly & diffusion resistors
- Salicide block etch



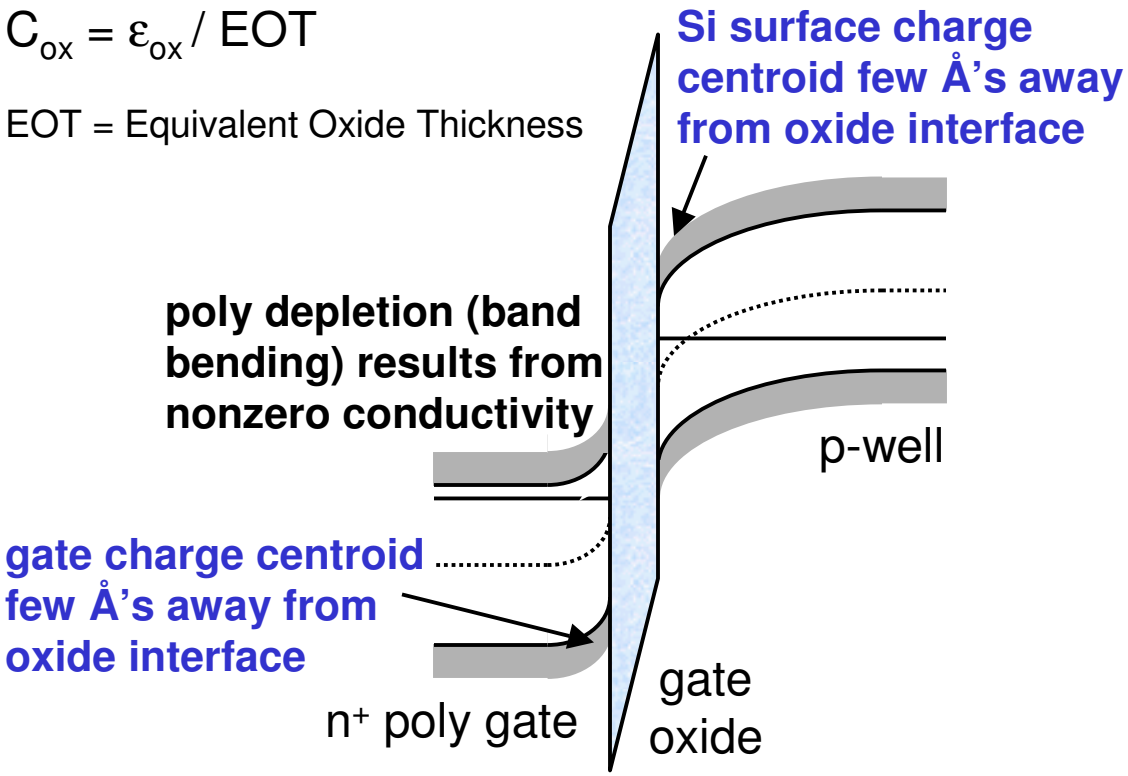
So What Do All These Cool Process Upgrades Mean To Designers?

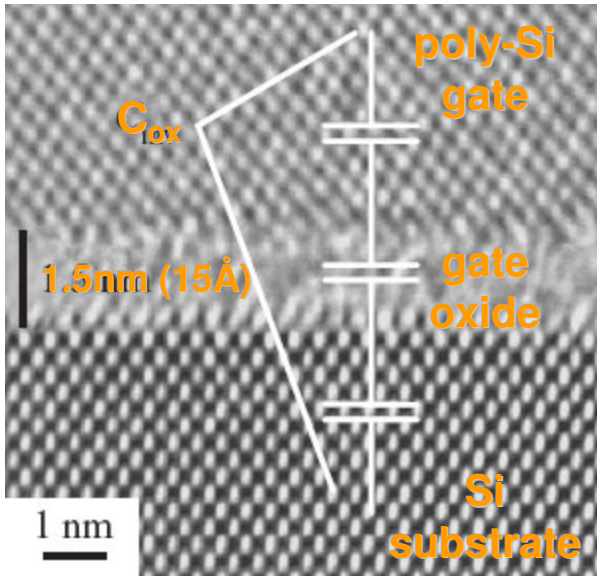
- Short answer…
  some extras but plenty more non-idealities to worry about,
  especially in analog land !!!
- We'll look at:
  - Poly depletion & charge centroid effects
  - V_T effects
    - Reverse short- & narrow-channel effects
    - Well proximity effect
  - Active area mechanical stress effect
  - Leakage current mechanisms
  - Multiple V_T devices
  - Impact of halos
  - Manufacturability

Poly Depletion & Surface Charge Centroid Effects

$C_{ox} = \varepsilon_{ox} / EOT$

EOT = Equivalent Oxide Thickness



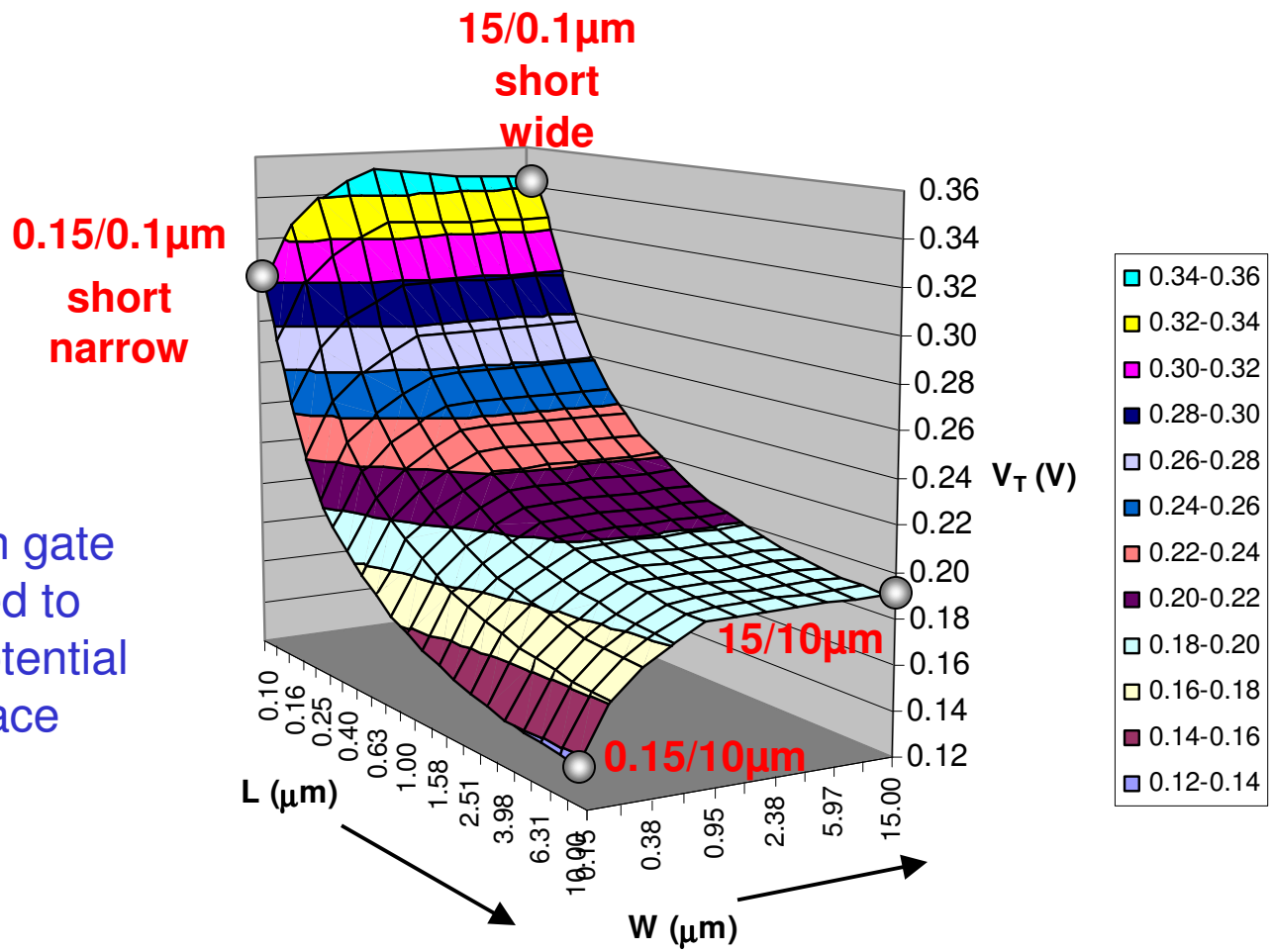


Source: Wong, IBM (2002)

- **Increasing discrepancy between electrical & physical gate oxide thicknesses since charges are not intimately in contact with oxide interface → C_{ox} not as small**
- **C_{ox} must account for gate & Si surface charge centroids as well as ε_{Si}**
- **Modeled in BSIM4 → more accurate I-V & C-V calculations**
- **Motivation for high-K gate dielectrics & metal/silicided gate technology**

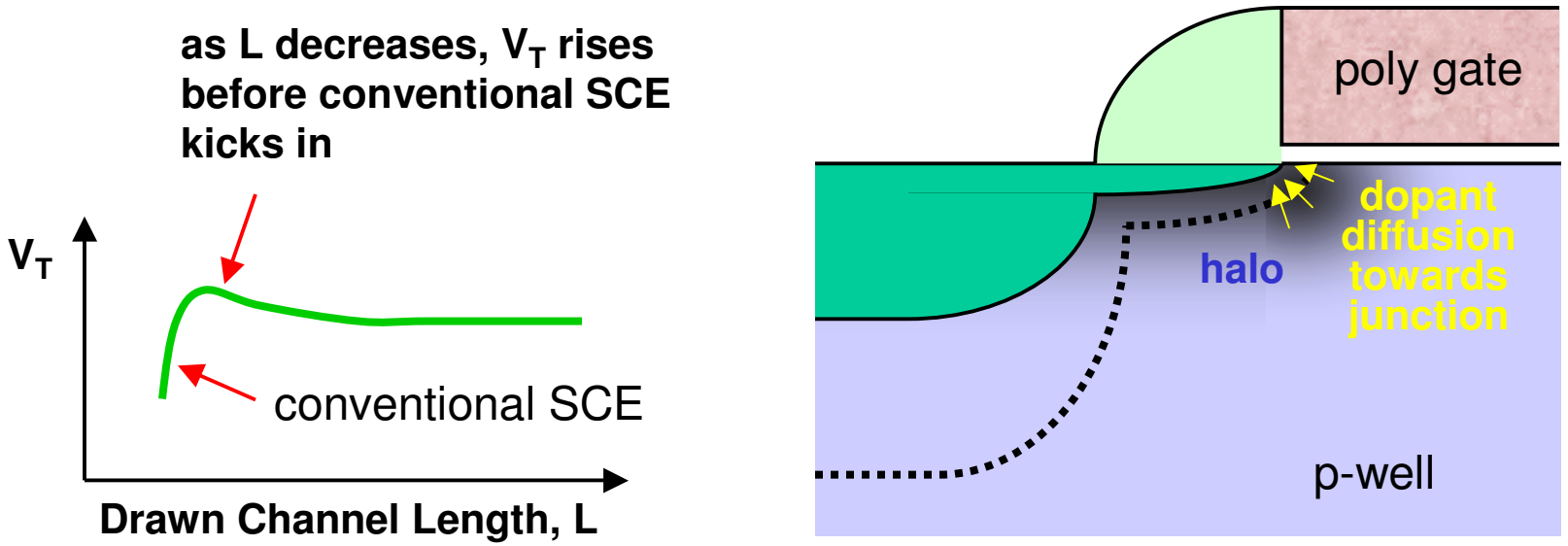
V_T Variations Across FET L & W in 90nm

- Wondered why so many transistor L & W bins in SPICE models?
- e.g., SPICE model linear V_T's for 90nm nom-V_T core nFET @ 85℃
  - V_T↑ as L ↓
  - V_T↓ as W ↓
  - WHY?



- Think how much gate charge is needed to raise surface potential needed for surface inversion

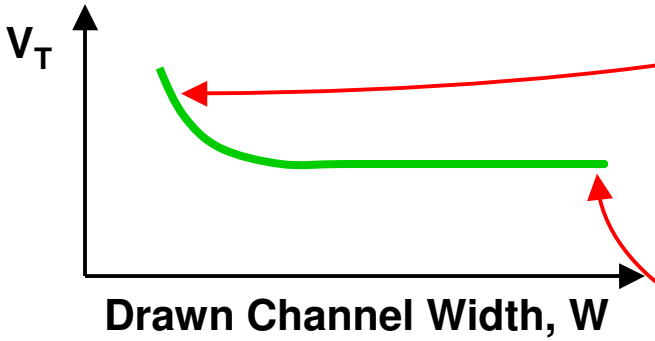
Reverse Short-Channel Effect (RSCE)

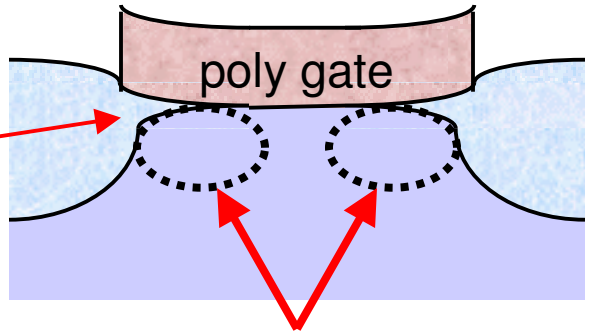


- **Mechanism – Transient Enhanced Diffusion (TED)**
  - **Damage from halo implant creates crystalline defects that accelerate diffusion of dopants in subsequent anneals where damage is eventually repaired**
  - **Dopants migrate to source-to-substrate junction & raise source-to-channel barrier height**
  - **V_T increases**
- **Target L_{min} at V_T peak for good process margin, i.e., minimize V_T sensitivity to poly-CD variations**

Narrow-Channel Effect (NCE)

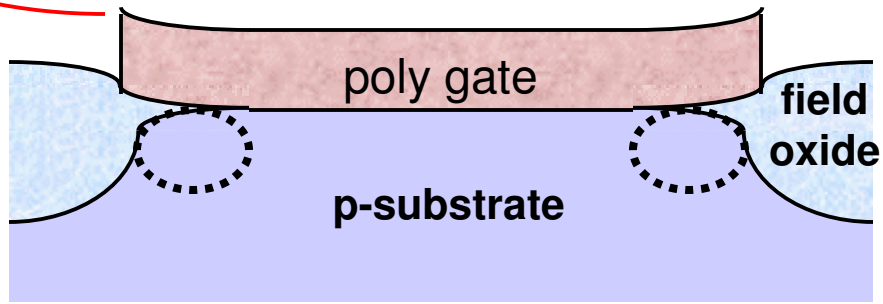
V_T increases for narrower W since more gate charge is required to deplete edge of active area under gate





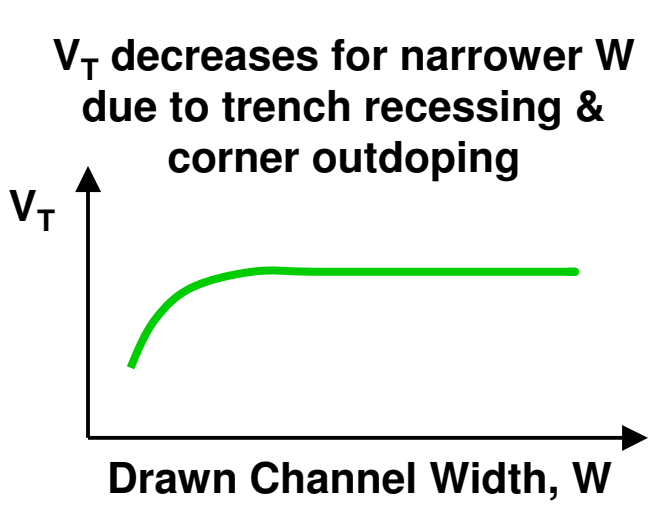
Thicker oxide under gate edge

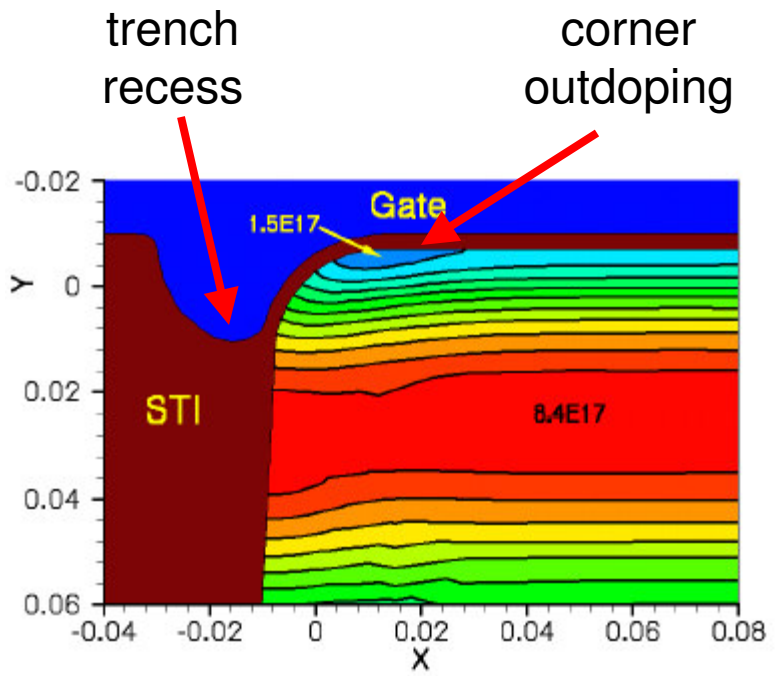
- **Tougher to deplete**
- **More gate charge needed for inversion**



- Prominent with LOCOS isolation
- Does not exist in STI

Reverse Narrow Channel Effect (RNCE)





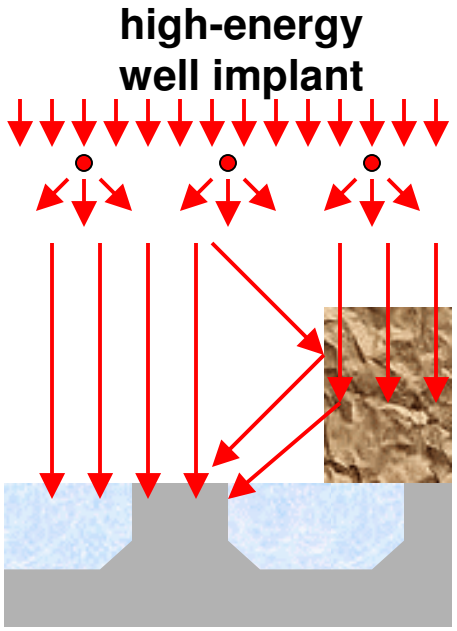
Source: Burenkov & Lorenz, Fraunhofer Institut (2003)

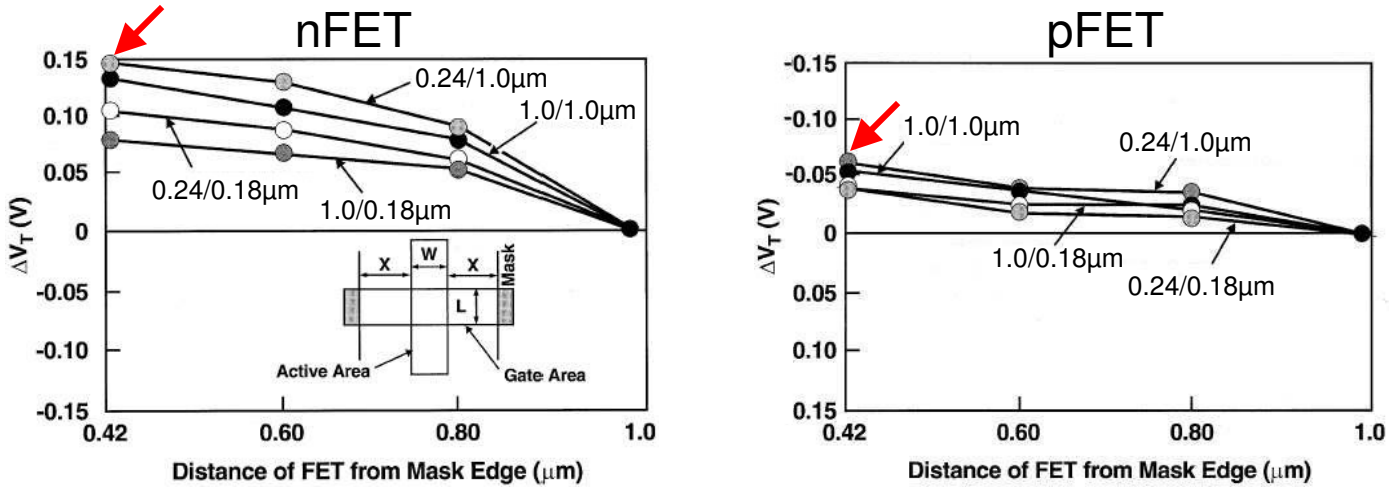
- Prominent in STI technologies
- Concentration of electric field lines terminating at corner
- Trench recess results from faster oxide etch rate at STI edge during pre-oxidation HF wet-cleans

- Edge device turns on before center device → I-V kink in very narrow devices

Well Proximity Effect

- $|V_T| \uparrow$ if FET is too close to edge of well resist mask due to extra channel dopants from lateral scattering off resist sidewall into active area during well implants
- $|\Delta V_T|$ depends on:
  - FET distance to well mask edge
  - FET orientation
  - implanted ion species/energy
- Most impact on narrow- & long-channel devices
- No impact on native FET's
- Well mask matching critical especially in analog layout
- Not modeled in BSIM4

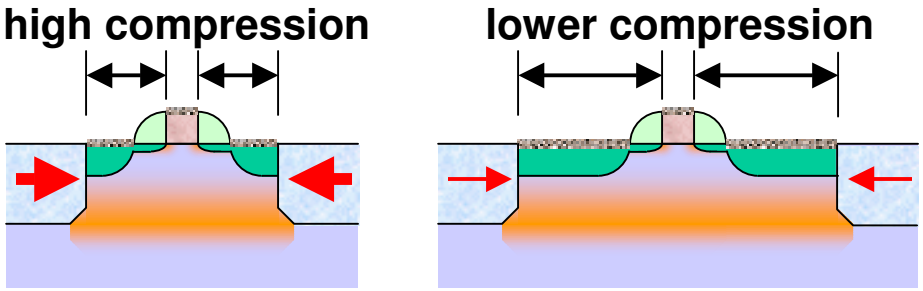




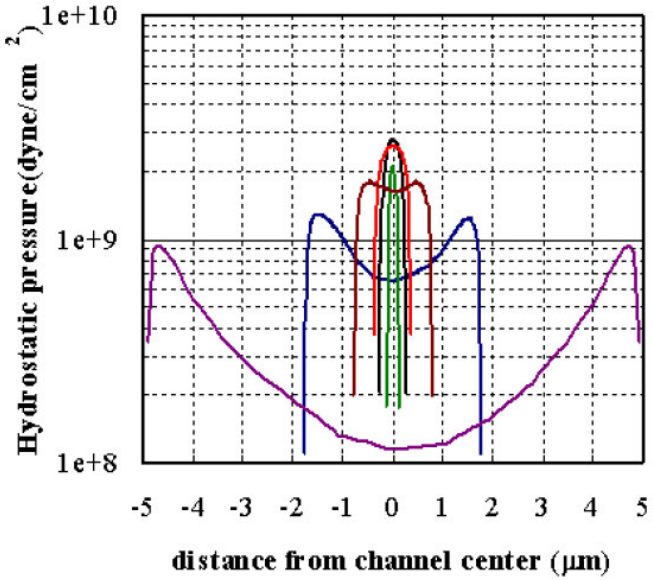
Source: Hook *et al.*, IBM (2003)

Active Area Mechanical Stress Effect

- Silicon is *piezoresistive* – electrical properties depends on mechanical stress state
  - Stress affects m*, μ, E_g, V_T, body effect, DIBL, …
  - Compression → slower nFET, faster pFET
  - Tension → faster nFET, slower pFET
- STI → compression in Si channel due to 10x CTE mismatch between Si & SiO_2
  - I_{dsat}'s can change by as much as 10-15% → affects digital device ratios
  - Channel stress is strong function of distance from poly to active edge

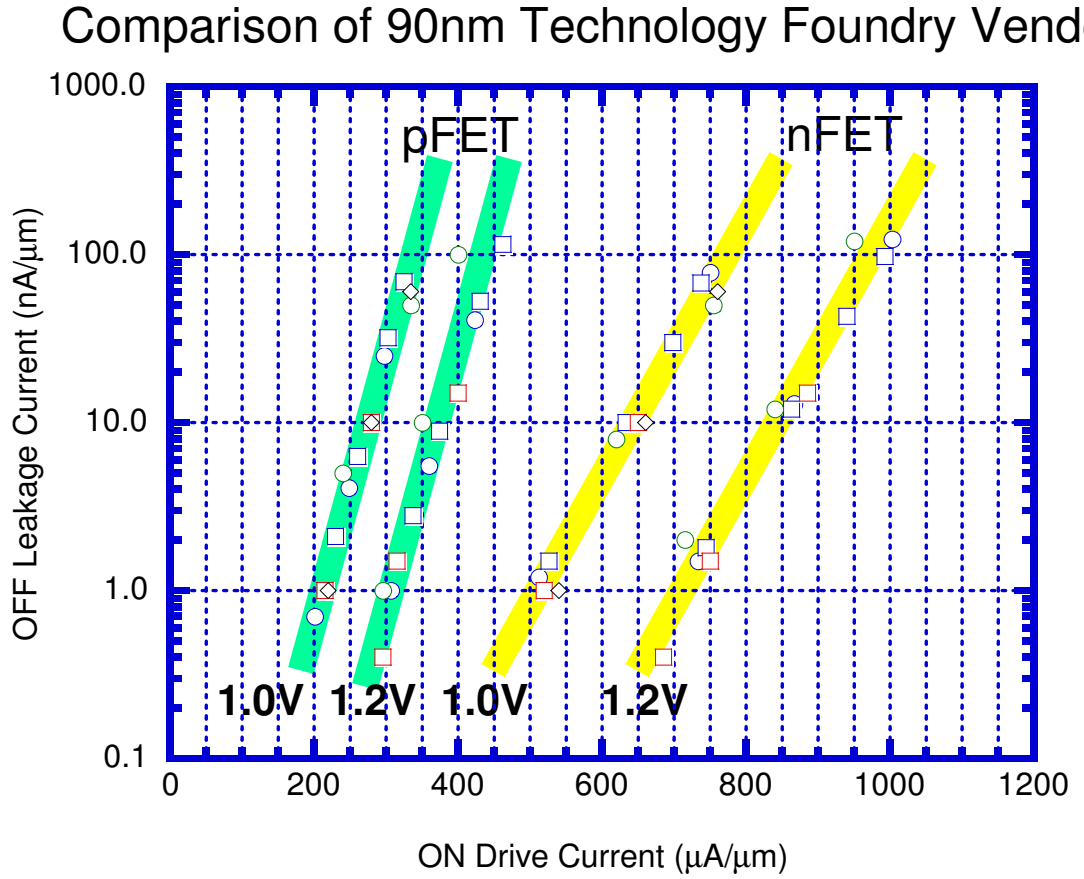


- Known for some time
  - Can play tricks with tensile spacer & silicide films to relieve channel stress
  - Basis of high-μ_n strained-Si technology
- Modeled in BSIM4 not BSIM3 (SA, SB)



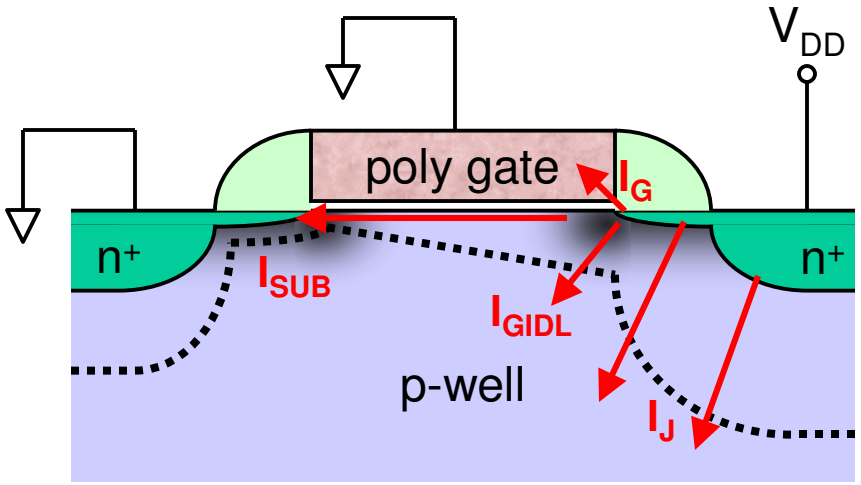
Source: Xi *et al.*, UC Berkeley (2003)

ON vs. OFF Current Benchmark

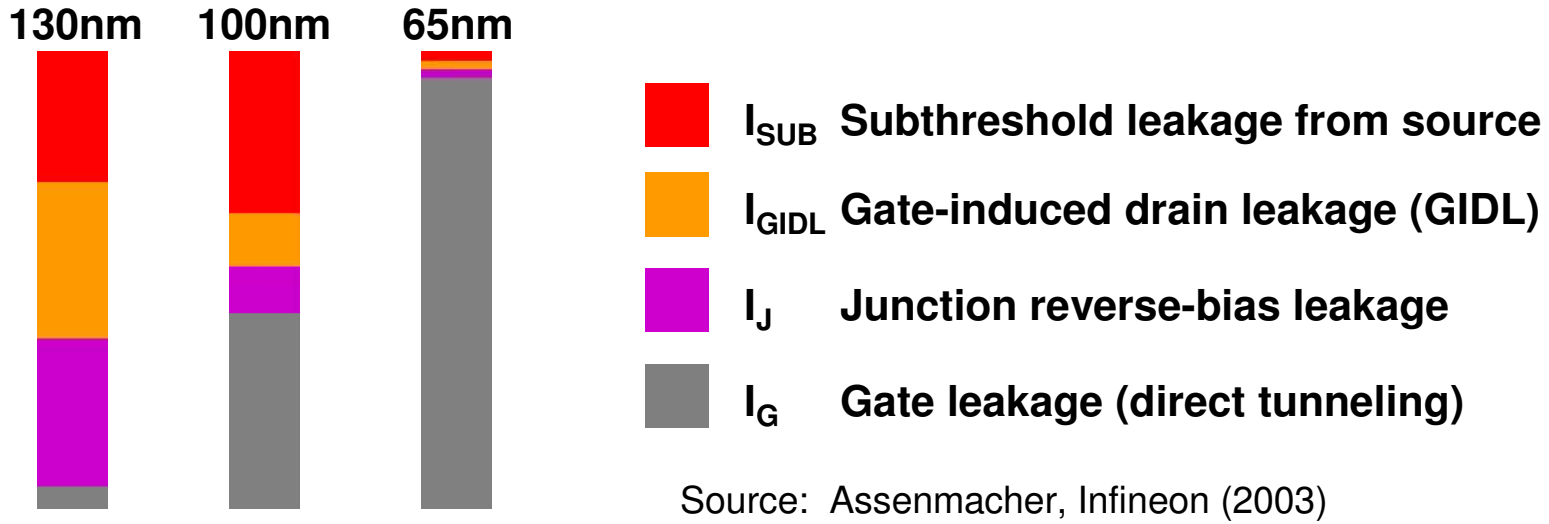


- "No free lunch" principle prevails again: high I_{ON} → high I_{OFF}
- V_T's not scaling as aggressively as V_{DD}
- Technology providers offer variety of V_T's on same die to concurrently meet high-speed vs. low-leakage needs

Leakage Current Contributions



- Relative contributions of OFF-state leakage

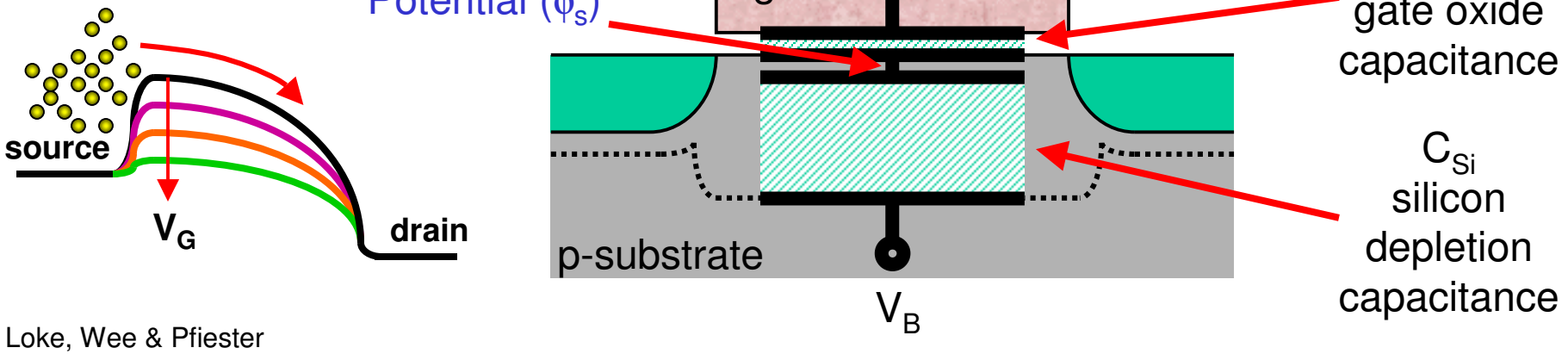


Source: Assenmacher, Infineon (2003)

Subthreshold Conduction

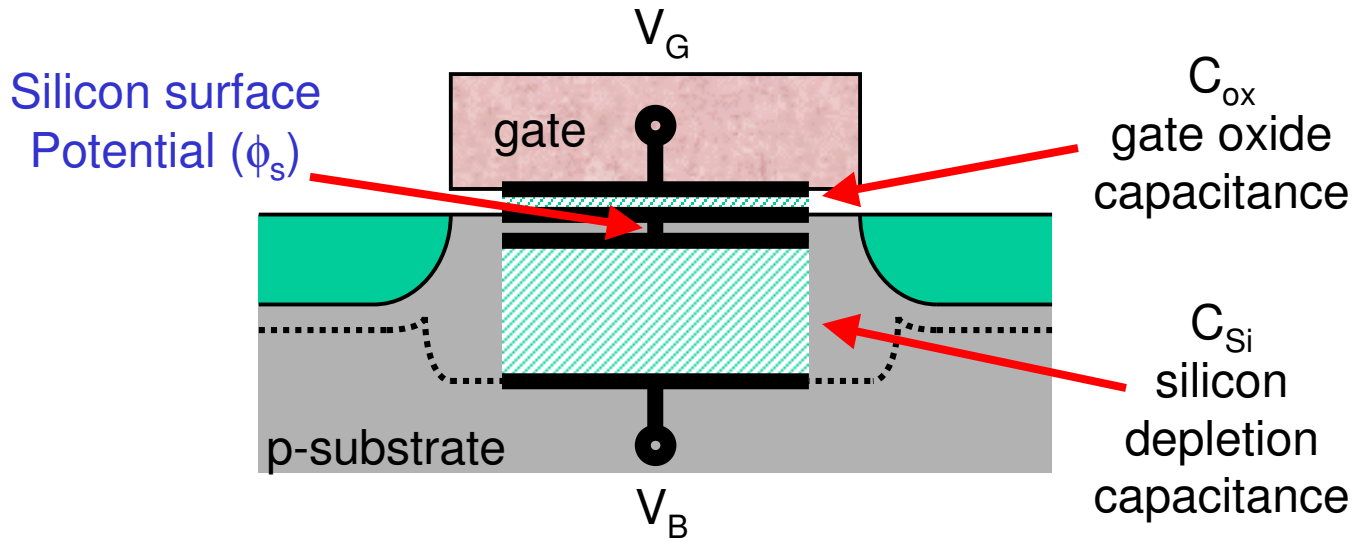
- **ON vs. OFF current – big issue with V_{DD} & V_T scaling**
  - **FET does not abruptly turn on: large I_{ON} → low V_T → large I_{OFF} leakage**
- **Diffusion current due to carriers from source spilling over source barrier into channel due to application of V_G to lower ϕ_s (weak dependence on V_{DS} in long-channel FET)**
- **Want to maximize coupling of V_G to ϕ_s but have capacitive sharing with substrate**
  - **Large C_{ox} → high-K gate dielectrics, thinner gate oxides**
  - **Small C_{Si} → low substrate doping, fully-depleted SOI**
  - **Inverse subthreshold slope (S) ≈ 100mV/decade at 300K (ideally 60mV/decade)**
    - **e.g., V_T=0.2V & I_{ON}= 100µA → I_{OFF}=1µA !!!**

$$\Delta\phi_s = \Delta V_G \times \frac{C_{ox}}{C_{ox} + C_{Si}} \qquad S = \frac{k_B T}{q} \ln(10) \times \frac{C_{ox} + C_{Si}}{C_{ox}}$$



Basic Intuition on Body Effect

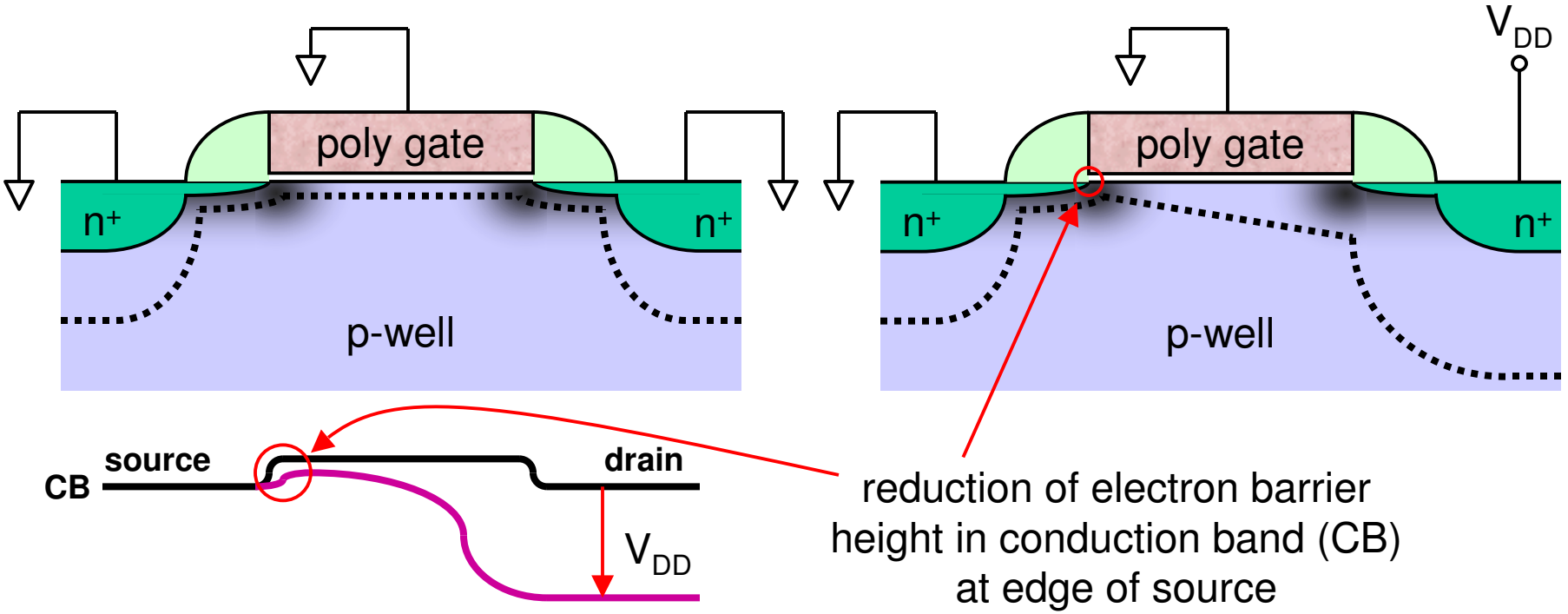
- **Body or backgate effect**
  - **Applying reverse bias between substrate (body) & source increases $|V_T|$**
- **Basic equation:** $V_T = V_{T0} + \gamma\,(\sqrt{2\phi_b + V_{SB}} - \sqrt{2\phi_b}\,)$
- Tug-o-war between V_G & V_B to control surface potential through C_{ox} & C_{si}
- Inversion layer forms when ϕ_s is lowered sufficiently with respect to source (that's where carriers come from)



- C_{si} decreases with increasing $|V_B|$
- Steeper subthreshold slope with body effect – only valid for long channel

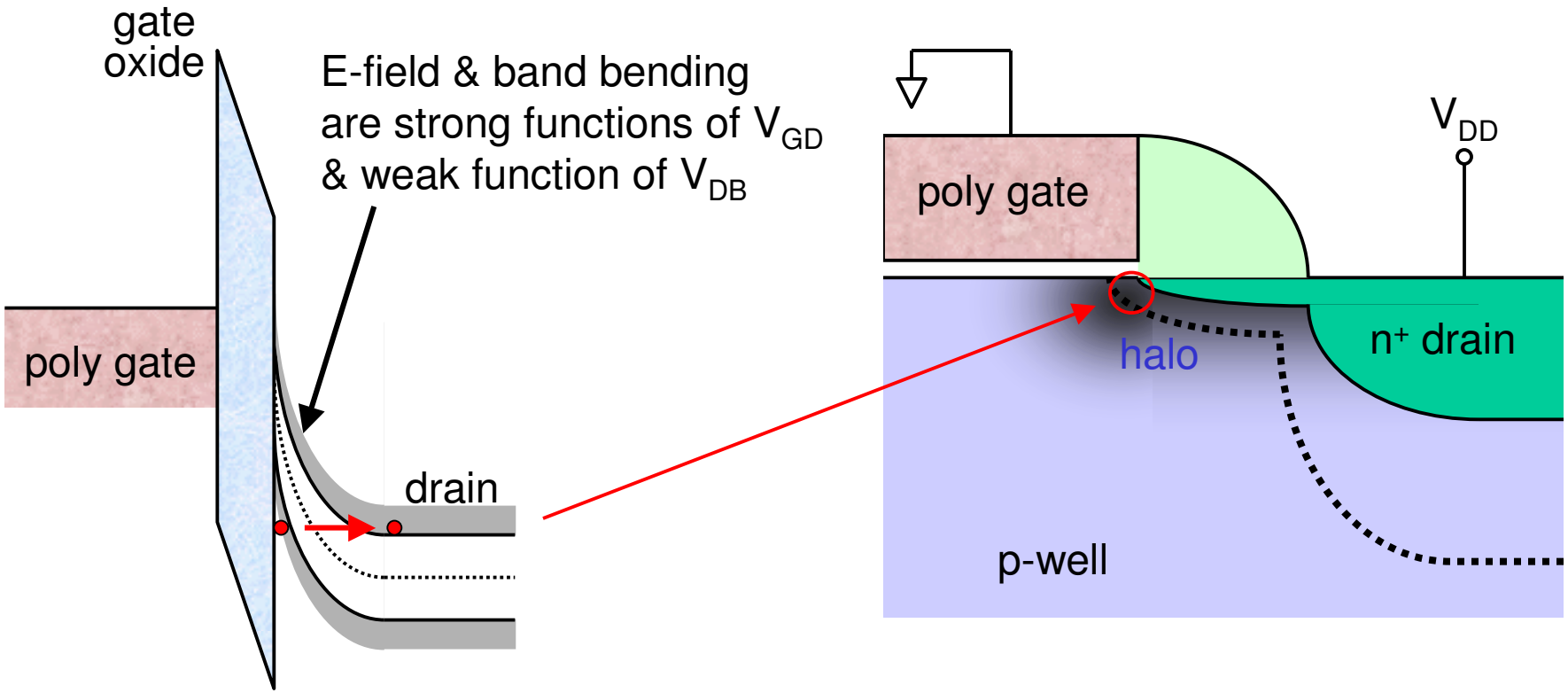
Drain-Induced Barrier Lowering (DIBL)

- Soft punchthrough induced by drain-to-substrate depletion region
  - $|V_T| \downarrow$ as $V_D \uparrow$ (drain-induced SCE)
  - $V_D \uparrow \rightarrow$ drain-to-substrate depletion region grows with more reverse bias
  - Lateral electric fields in drain-induced depletion region lowers source-to-channel barrier, allowing more carriers to diffuse from source to channel
- Typical DIBL magnitude: $\Delta V_T = -0.12V$ for $\Delta V_D = +1.2V$ in 90nm



Gate-Induced Drain Leakage (GIDL)

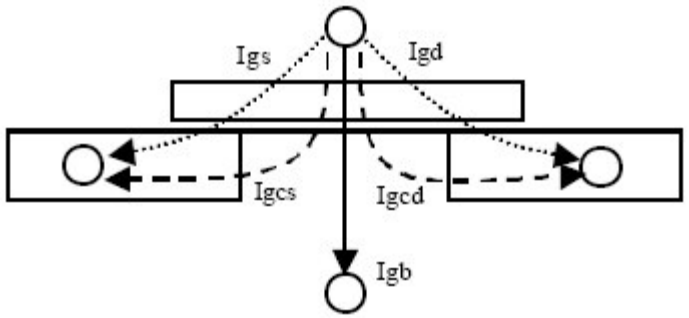
- Drain-to-substrate leakage due to band-to-band tunneling current in very high-field depletion region in drain overlap region



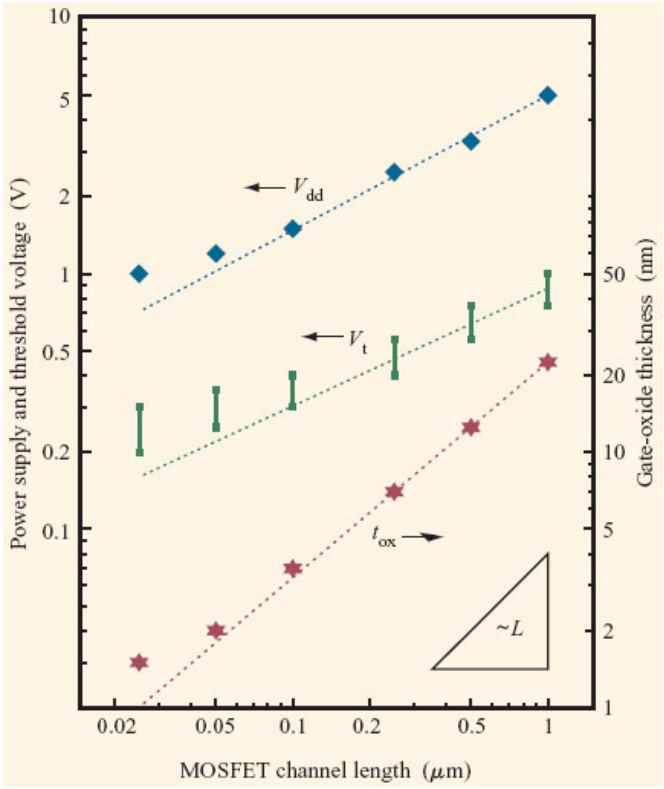
- Similar gate-induced source leakage (GISL) mechanism exists when source is raised above gate potential
- Modeled in BSIM4 not BSIM3

Gate Leakage (Direct Tunneling)

- t_{ox} has been scaling aggressively with L_{min}
  - higher I_{FET}
  - tighter gate control → less SCE
- Significant direct tunneling for $t_{ox} < 2nm$
- Gate leakage = $f(t_{ox}, V_G)$
  - Tunneling probability $\propto \exp(-\alpha\, t_{ox})$
  - V_G dependence from Fermi-Dirac statistics & density-of-states considerations
- Hole & electron tunneling in CB & VB
- High-K gate dielectric achieves same C_{OX} with much thicker t_{ox}
- Modeled in BSIM4 not BSIM3



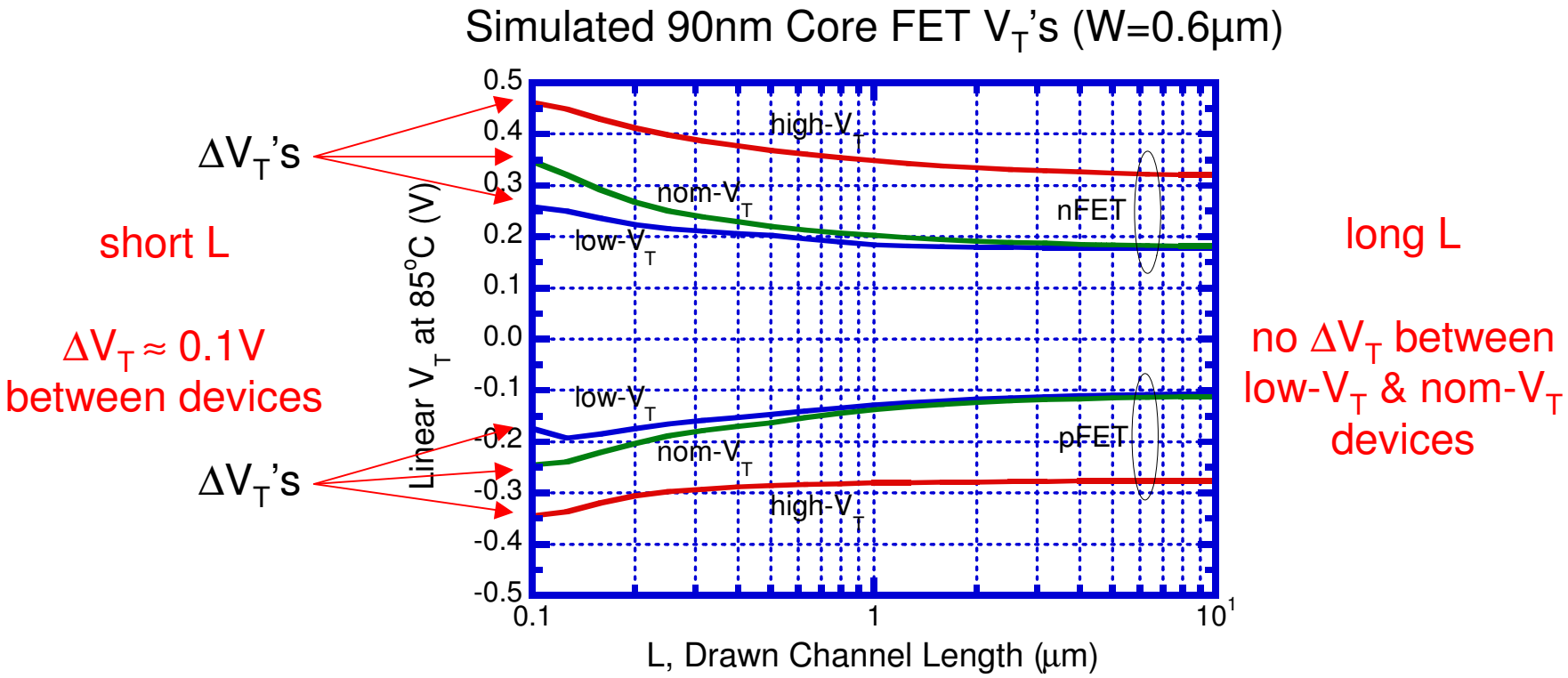
Historical Trends



Source: Taur, IBM (2002)

Using FET's with Multiple V_T's

- Be very careful when using multiple-V_T FET's, *especially in analog land*
  - V_T separation typically advertised only for $L \approx L_{min}$



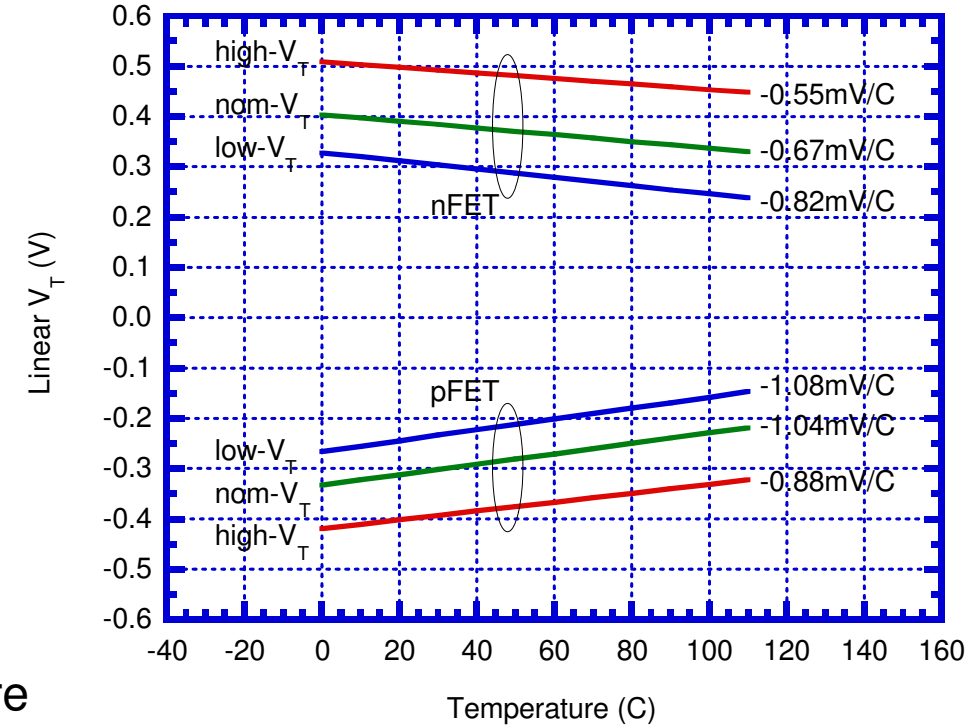
- Different mechanisms for setting V_T in low-V_T vs. high-V_T devices
  - Want to share as many implant masks as possible to save $$$
  - V_T adjustment: channel implant vs. halo implant

V_T vs. Temperature

- $|V_T| \downarrow$ as $T \uparrow$
  - $T \uparrow$
    - $\rightarrow E_g \downarrow$
    - $\rightarrow n_i \uparrow$
    - $\rightarrow \phi_b \downarrow$ for constant N_A
    - $\rightarrow |V_T| \downarrow$

$$\phi_b = \frac{k_B T}{q} \ln \frac{N_A}{n_i}$$

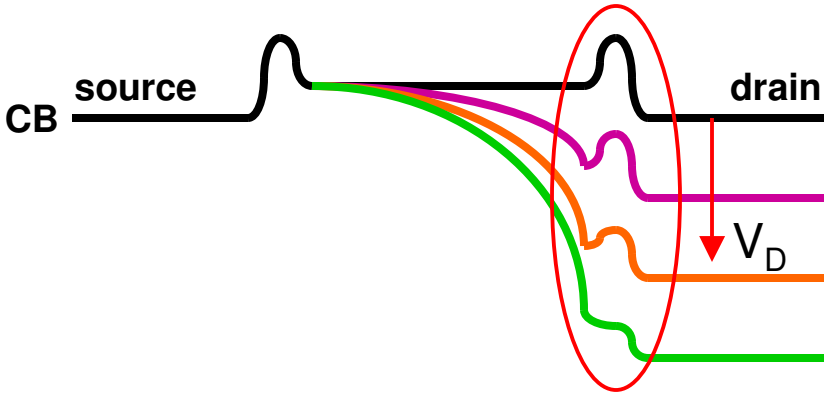
Simulated Linear V_T for 0.6/0.1µm Core FET's

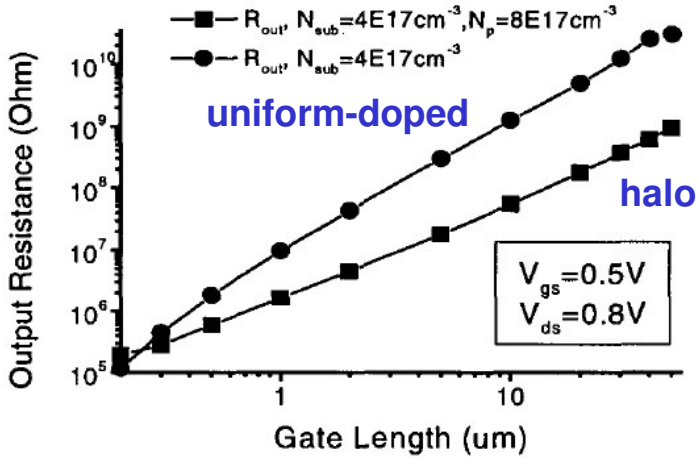


- V_T can vary a lot with temperature
- Worse I_{OFF} due to $|V_T| \downarrow$ & S $\uparrow$
- Temperature sensitivity depends on W & L
- Analog implication: With V_T becoming increasing % V_{GS} given reduced V_{DD}, cold temperatures may yield worst headroom

Impact of Halos on Analog Design

- Halo at source side suppresses SCE & DIBL in *short-channel devices*
- Halo at drain side creates *Drain-Induced Threshold Shift* (DITS) in *long-channel devices*
  - Drain bias very effective in modulating drain halo barrier → $V_T \downarrow$ → $I_{ds} \uparrow$
  - Worse DIBL compared to uniform-doped FET
  - Can degrade FET r_{out} by 10-100x!!!
  - Critical limitation for building current sources (cascoding difficult with low V_{DD})
  - Asymmetric FET's with only source-side halo shown to improve r_{out} significantly



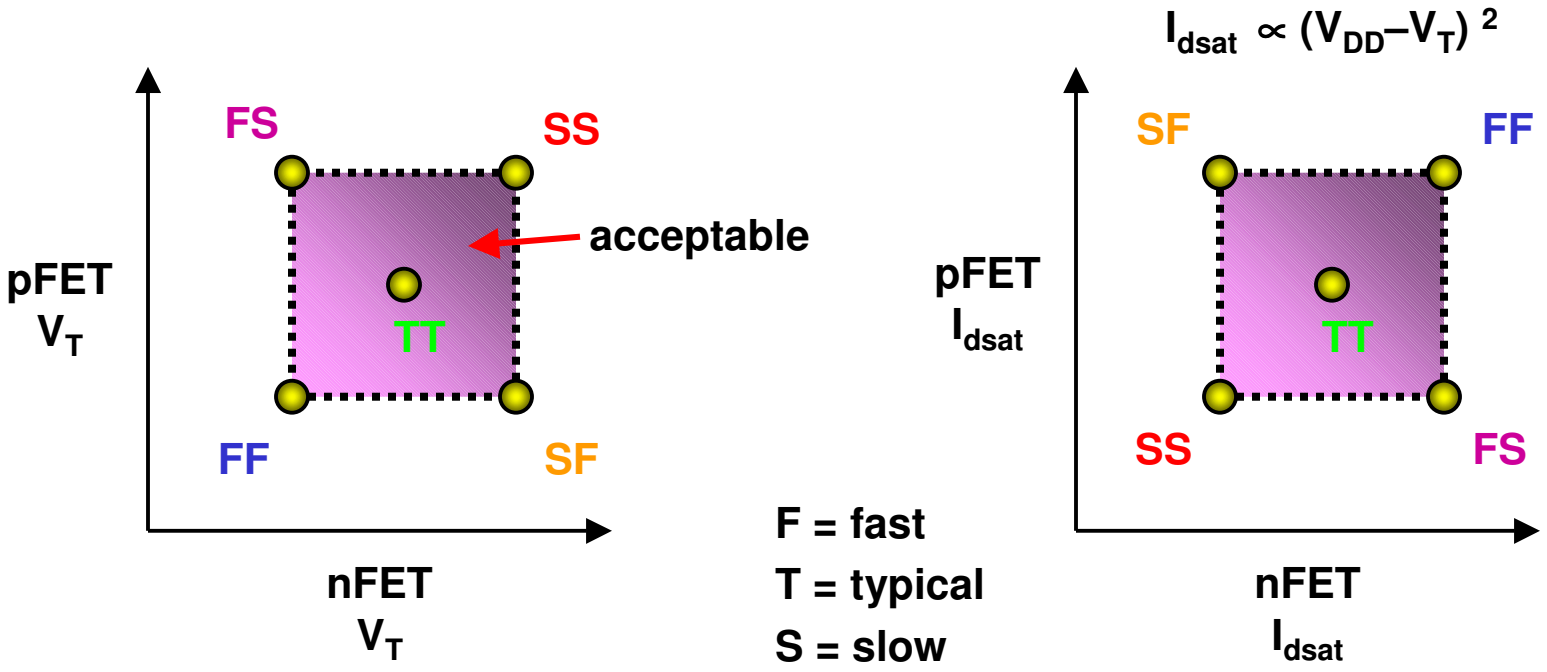


Source: Cao *et al.*, UC Berkeley (1999)

- Halos increase C_{gb} when FET is not in inversion
- Modeled in BSIM4 not BSIM3, but still need improvement

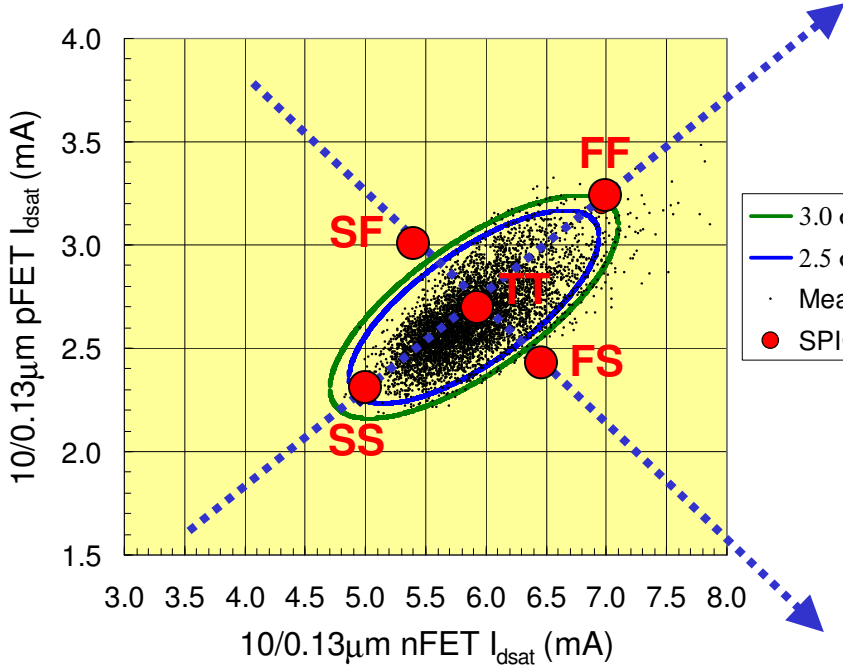
Characterizing Process Variations

- Statistical variations in IC manufacturing → variations in FET characteristics
- Circuits must function across operating V_{DD} & temperature but also across statistically acceptable process tolerances
- Statistical variations summarized by spread in nFET & pFET V_T's, or in I_{dsat}'s, i.e., use V_T or I_{dsat} to summarize cumulative effect of ALL process variances
- Consider die-to-die, wafer-to-wafer & lot-to-lot variations



Correlated vs. Uncorrelated Process Variations

- Elliptical 2-D Gaussian distribution from natural variations with no deliberate retargetting of process parameters



correlated variations due to common processes e.g., poly photo/etch CD & gate oxide thickness

uncorrelated variations due to uncommon processes e.g., channel & well ion implants

- Tougher to control poly CD than implant doses

Skew Process for Design Margin Verification

- Process wafers with I_{dsat}'s that target SPICE corners of acceptable distribution
- Statistical distribution is cumulative result of ALL variations for processes targetted as NOMINAL
- Countless possibilities of tweaks to achieve skew nFET/pFET I_{dsat} combination
- Fab typically employs *SIMPLE* means of retargetting nFET & pFET I_{dsat}'s with very few *deliberate* non-nominal process tweaks
  - FF vs. SS
    - Adjust poly CD, no change in gate oxide thickness
    - Nominal implant doses
  - FS vs. SF
    - Adjust surface channel or halo implant dose
    - Nominal poly CD & gate oxide thickness
- Consequences
  - Nominal & skew results frequently miss intended targets since nominal (by definition) can land anywhere in distribution
  - Not 100% representative of natural process corners
  - Decent approximation for vanilla digital circuits
  - May be bad approximation for some analog & high-speed digital circuits if they are insensitive to selected tweaks

Additional Commentary
Manufacturing Impact on Design

- Importance of poly gate orientation – align FET gate along x or y?
  - Preferred orientation will likely exist due to step-and-scan nature of gate lithography
- FET mismatch
  - Symmetric circuits that are built asymmetric may fail
  - DFM (design for manufacturability) is a big buzz word now
    → need for Monte Carlo simulations to statistically validate design
- Exposure λ is *not* scaling as aggressively as L_{min}
  - Roadmaps are just guidelines
  - Huge industry resistance to move to 157nm
    - Requires *reflective* optics → $$$
  - Expect more gate resist trimming & relatively worse CD/overlay control at 65nm node
- Whole business of minimum vs. recommended design rules
  - Who is willing to design let alone *pay* for poor yield?
- Statistical design considerations & *layout engineering* becoming more critical than ever

Conclusions

- CMOS scaling continues to be driven by digital circuit needs
- Should expect incremental changes in 65nm CMOS technology
  - Hopefully no major surprises
- Increasing mechanical engineering opportunities in IC technology
- Always a time lag for SPICE models to account for new effects
  - Pressing issue since tapeout mistakes are costlier than ever
  - Need to work closely with technology providers to quickly find out about these new effects
  - Account for them or avoid them!!!
- Statistical design & layout considerations more critical than ever
- Analog designers have to keep living with what they get from digital
  - Designers with intimate knowledge of technology constraints will be best positioned to avoid pitfalls & to turn bugs into features
  - Could you think of a better time to be doing design? ☺

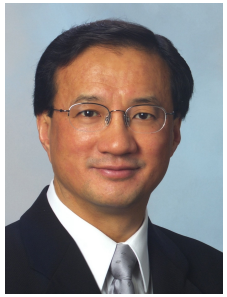
References

- T. B. Hook *et al.*, "Lateral Ion Implant Straggle and Mask Proximity Effect," *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1946-1951, Sept. 2003.
- J. Assenmacher, "BSIM4 Modeling and Parameter Extraction," *Technical Univ. Berlin Analog Integrated Circuits Workshop*, Mar. 2003.
- X. Xi *et al.*, BSIM4.3.0 MOSFET Model – User's Manual, *The Regents of the University of California at Berkeley*, 2003.
- International Technology Roadmap for Semiconductors, *Front End Processes* (2003 Edition), 2003.
- H.-S. P. Wong, "Beyond the Conventional Transistor," *IBM Journal of Research & Development*, vol. 46, no. 2/3, pp. 133-168, Mar. 2002.
- Y. Taur, "CMOS Design Near the Limit of Scaling," *IBM Journal of Research & Development*, vol. 46, no. 2/3, pp. 213-222, Mar. 2002.
- C. R. Cleavelin, "Front End Manufacturing Technology," *IEEE IEDM Short Course on The Future of Semiconductor Manufacturing*, Dec. 2002.
- D. Harame, "RF Device Technologies," *IEEE IEDM Short Course on RF Circuit Design for Communication Systems*, Dec. 2002.
- S. Thompson *et al.*, "A 90nm Logic Technology Featuring 50nm Strained Silicon Channel Transistors, 7 Levels of Cu Interconnect, Low k ILD, and 1µm^2 SRAM Cell," *IEEE IEDM Tech. Digest*, pp. 61-64, Dec. 2002.
- C. C. Wu *et al.*, "A 90nm CMOS Device Technology with High-Speed , General-Purpose, and Low-Leakage Transistors for System on Chip Applications," *IEEE IEDM Tech. Digest*, pp. 65-68, Dec. 2002.

References (cont'd)

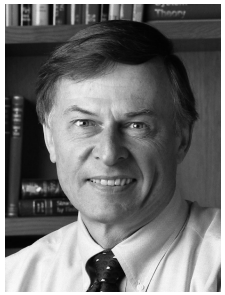
- R. Rios *et al.*, "A Three-Transistor Threshold Voltage Model for Halo Processes," *IEEE IEDM Tech. Digest*, pp. 113-116, Dec. 2002.
- R.A. Bianchi *et al.*, "Accurate Modeling of Trench Isolation Induced Mechanical Stress Effects on MOSFET Electrical Performance," *IEEE IEDM Tech. Digest*, pp. 117-120, Dec. 2002.
- B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2001.
- J. D. Plummer *et al.*, *Silicon VLSI Technology– Fundamentals, Practice and Modeling*, Prentice-Hall, 2000.
- K. M. Cao *et al.*, "Modeling of Pocket Implanted MOSFETs for Anomalous Analog Behavior," *IEEE IEDM Tech. Digest*, pp. 171-120, Dec. 1999.
- A. Chatterjee *et al.*, "Transistor Design Issues in Integrating Analog Functions with High Performance Digital CMOS," *IEEE Symp. VLSI Technology Tech. Digest*, pp. 147-148, June 1999.
- T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 1998.
- D. P. Foty, *MOSFET Modeling with SPICE: Principles and Practice*, Prentice-Hall, 1996.
- A. Beiser, *Concepts in modern Physics (4th ed.)*, McGraw-Hill, 1987.
- S.M. Sze, *Physics of Semiconductor Devices (2nd ed.)*, John Wiley & Sons, 1981.

Acknowledgments (My Device & Circuits Teachers)

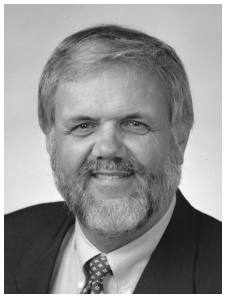


Prof. Simon Wong
Stanford University

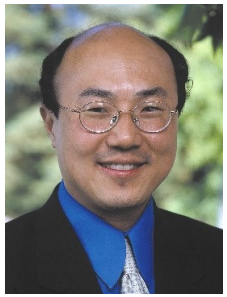
Prof. Krishna Saraswat
Stanford University



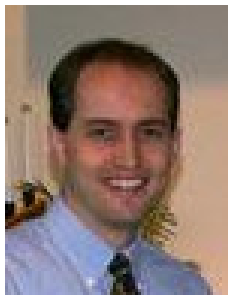
Prof. James Plummer
Stanford University



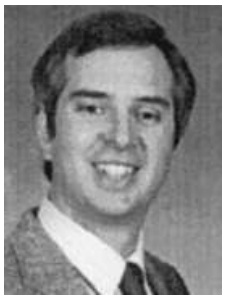
Prof. Bruce Wooley
Stanford University



Prof. Tom Lee
Stanford University



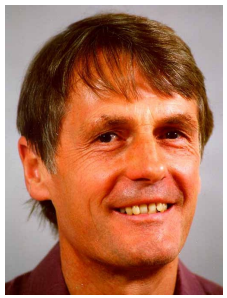
Dr. Stephen Kuehne
Agere



Dr. Gary Ray
Novellus

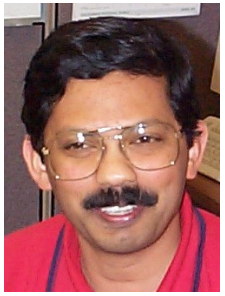
Dr. Jeff Wetzel
Sematech

Prof. Martin Wedepohl
University of B.C.



Prof. David Pulfrey
University of B.C.

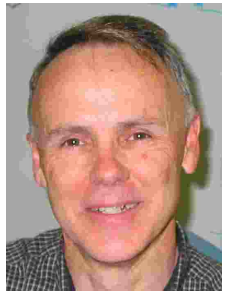
Tom Cynkar
Agilent



Dr. Peter George
Agilent

Mike Gilsdorf
Agilent

Dr. Chintamani Palsule
Agilent



Bob Barnes
Agilent