

A 90nm Variable Frequency Clock System for a Power- Managed Itanium® Architecture Processor

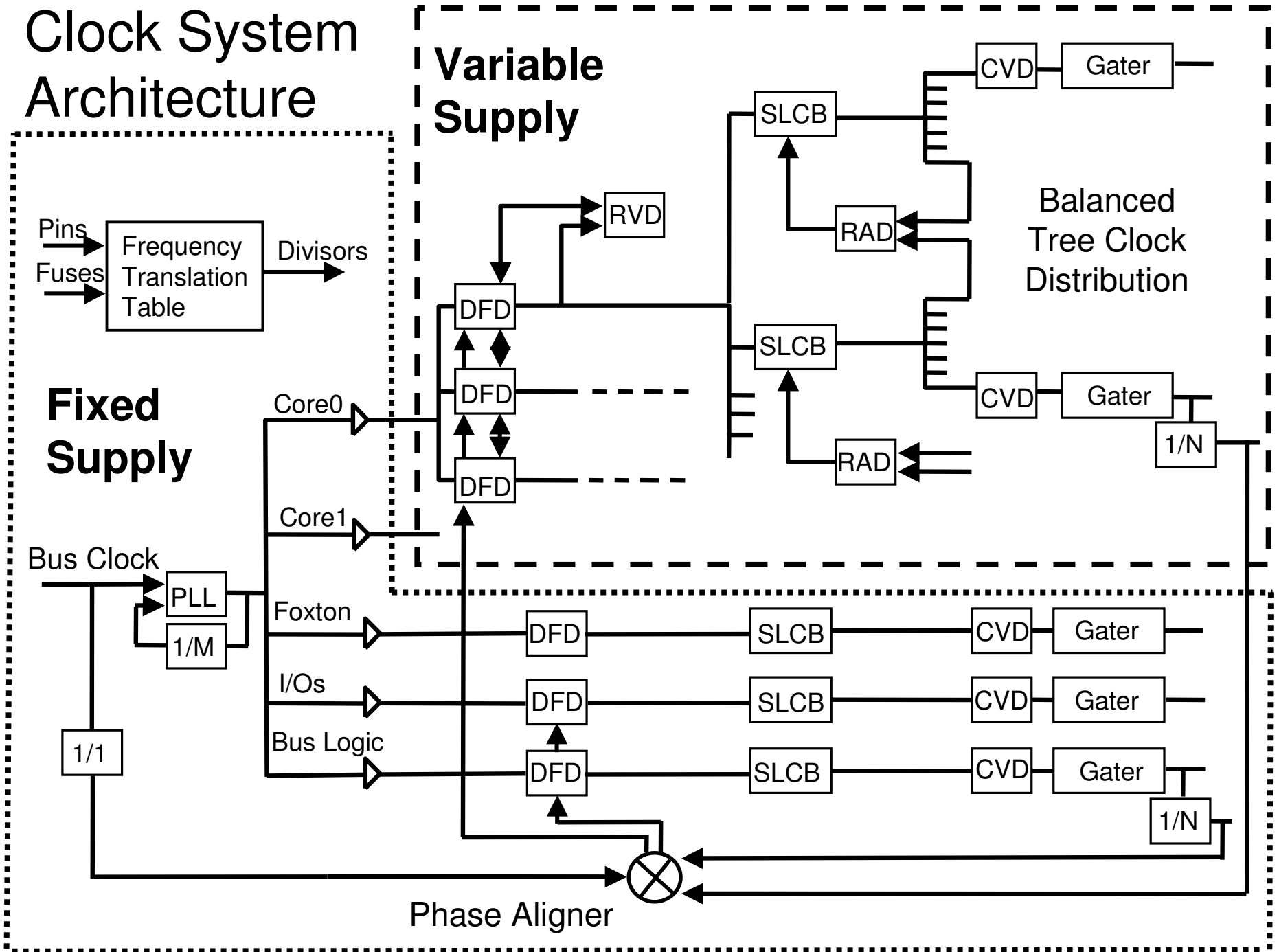
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Presentation Overview

- Montecito Clock System Architecture
- Montecito Voltage to Frequency Converter (VFC) Architecture
 - Digital Frequency Divider (DFD)
 - Regional Voltage Detector (RVD)
- Results
- Summary and Acknowledgements

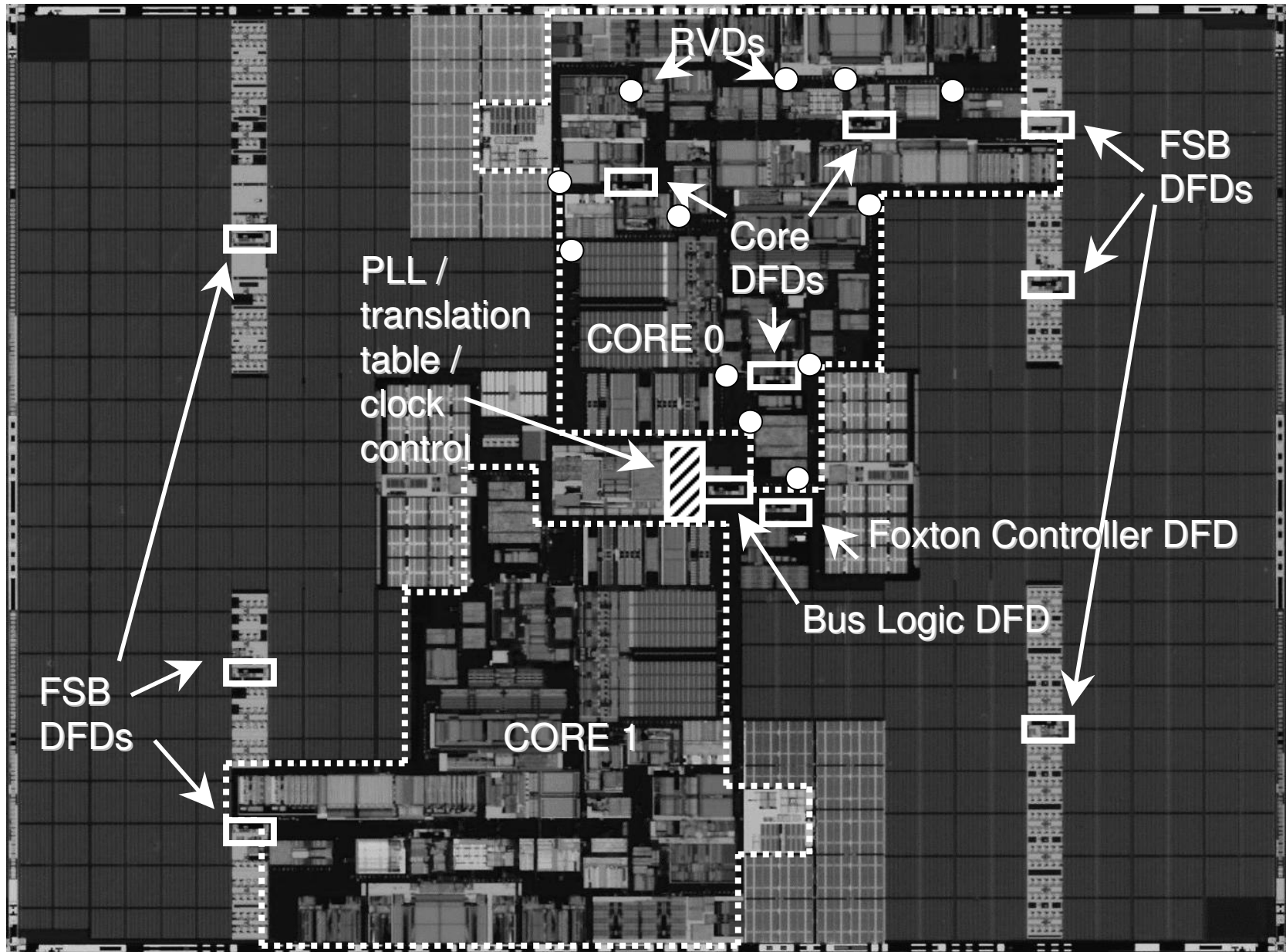
Clock System Architecture



Montecito Clock Generation Overview

- PLL generates master clock: $F_{\max} = M * F_{\text{bus_clock}}$
- DFDs lock on F_{\max} using local DLLs
 - Synthesize core / uncore frequencies in 1.6% F_{\max} steps (*ticks*)
 - DFD range is $F_{\max} * 1.0$ to $F_{\max} * 0.504$
 - Translation table sets DFD frequency at startup
- Supply / Clock Domains
 - 2 Cores : variable V, F
 - Uncore (bus logic): fixed V, $F = N * \text{bus clock}$
 - Foxtan controller : fixed V, $F = 1 \text{ GHz}$, DSP algorithms
 - Master PLL : fixed V, F, within clock system only

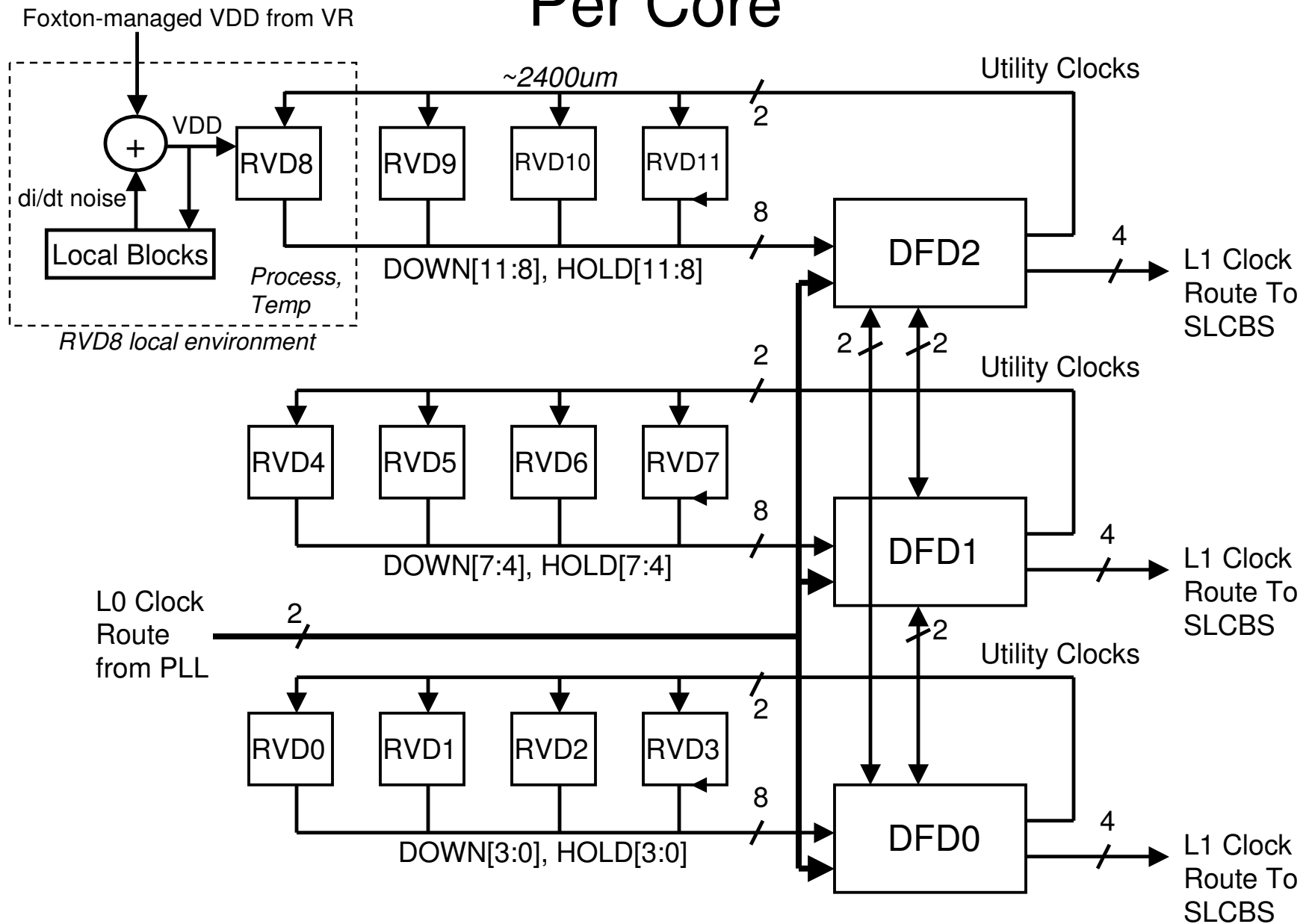
Montecito Clock System Floorplan



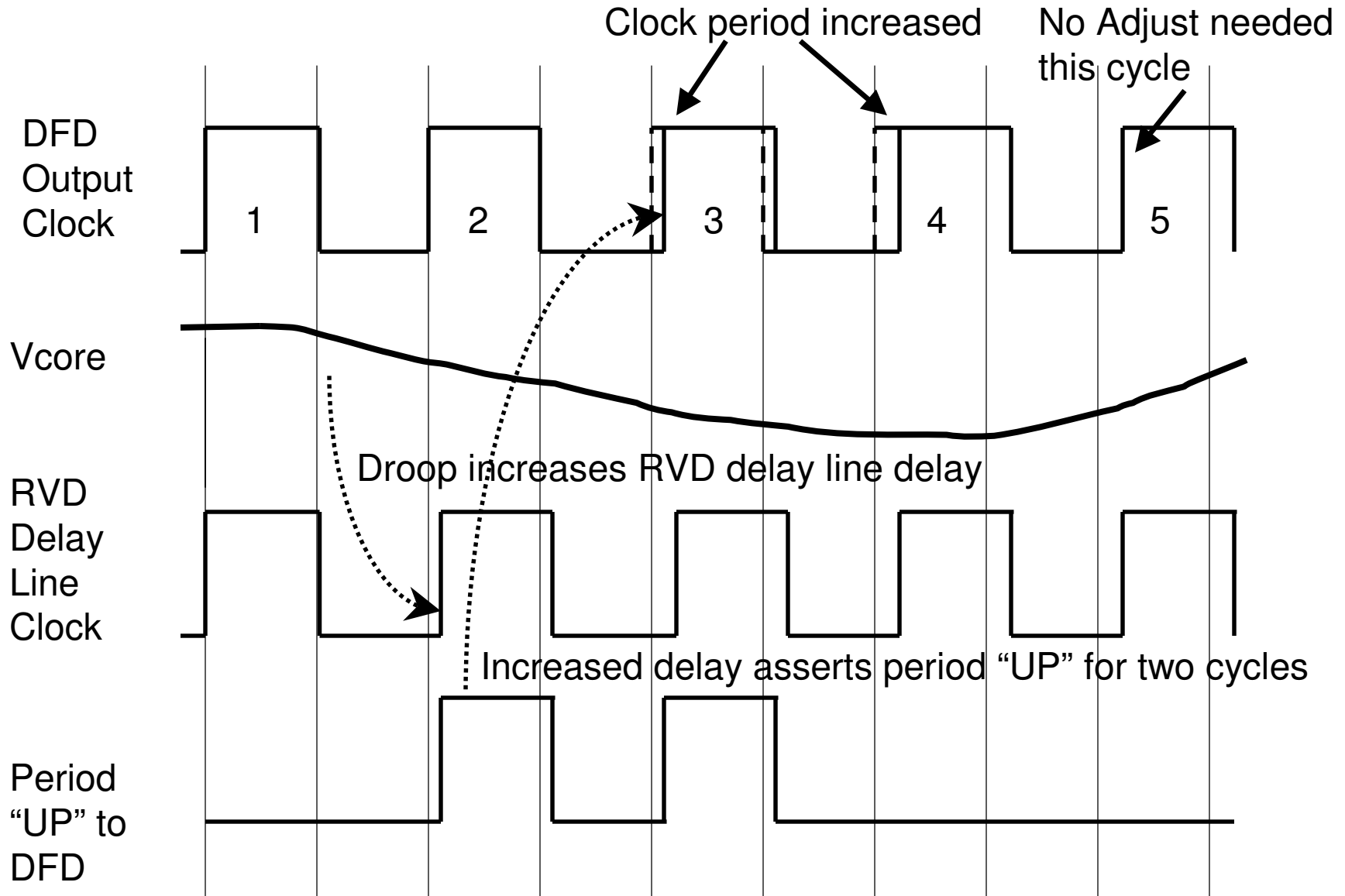
Clock System Modes

- Fixed Frequency (FFM)
 - Cores/Uncore are frequency and phase aligned
 - Cores/Uncore interfaces synchronous
- Variable Frequency (VFM)
 - Core supply modulated by Foxtan Controller to manage power envelope
 - Core frequencies track V_{core} via Regional Voltage Detector (RVD) V-F curves
 - Respond to Foxtan modulation and local transients
 - V-F curves match worst-scaling paths on chip
 - Core/Uncore interfaces asynchronous

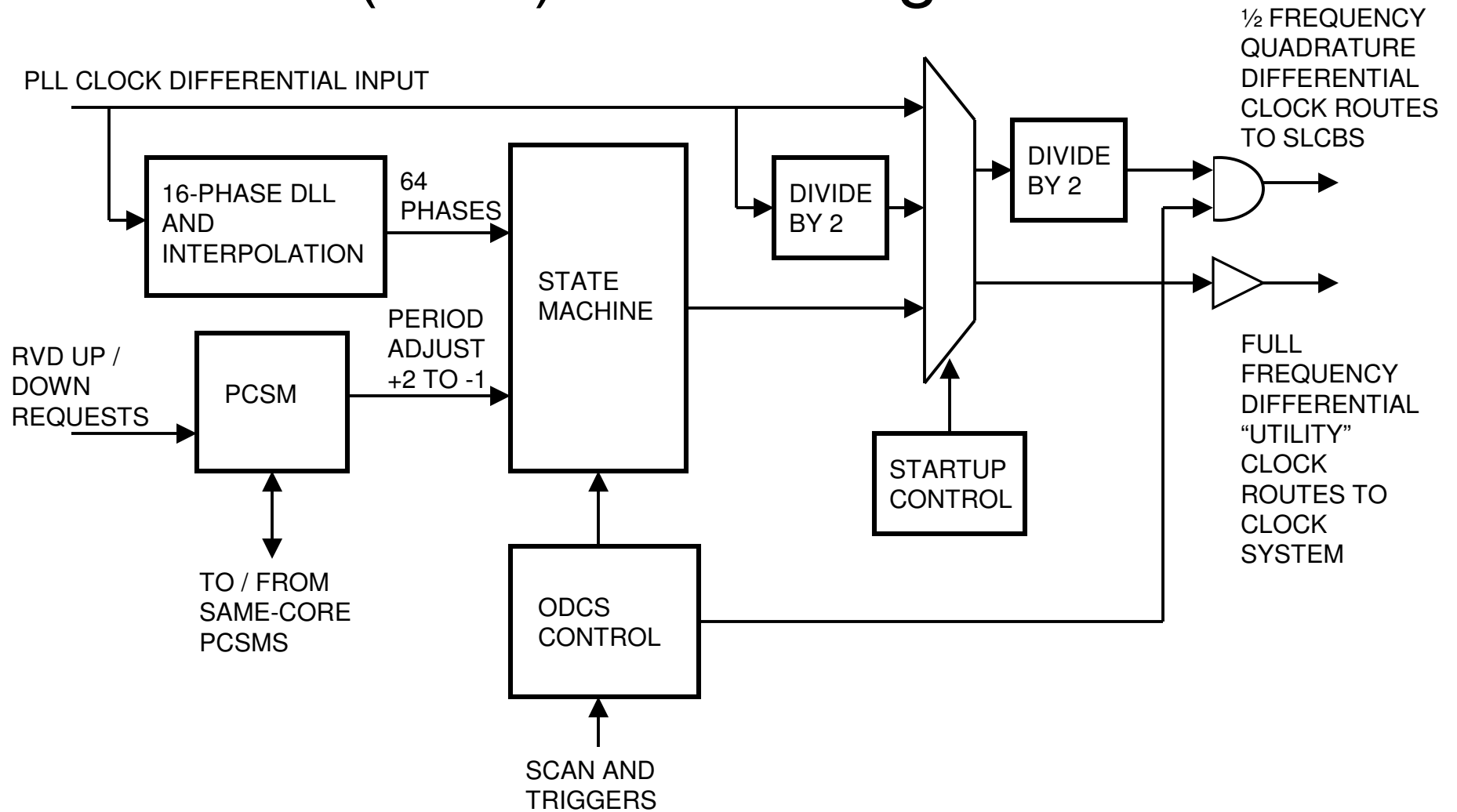
Voltage-to-Frequency Conversion (VFC) Per Core



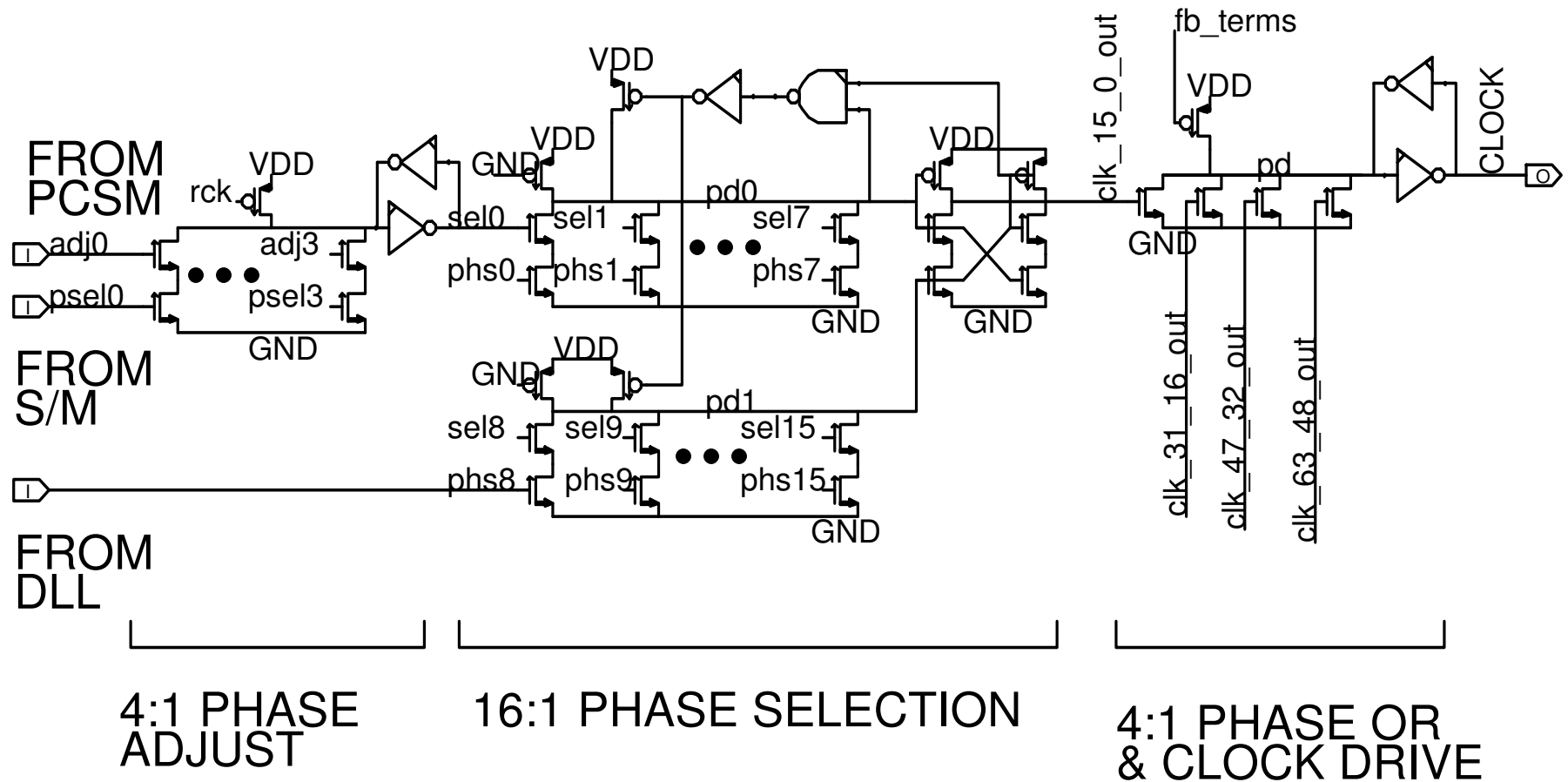
Example VFC Supply Droop Response



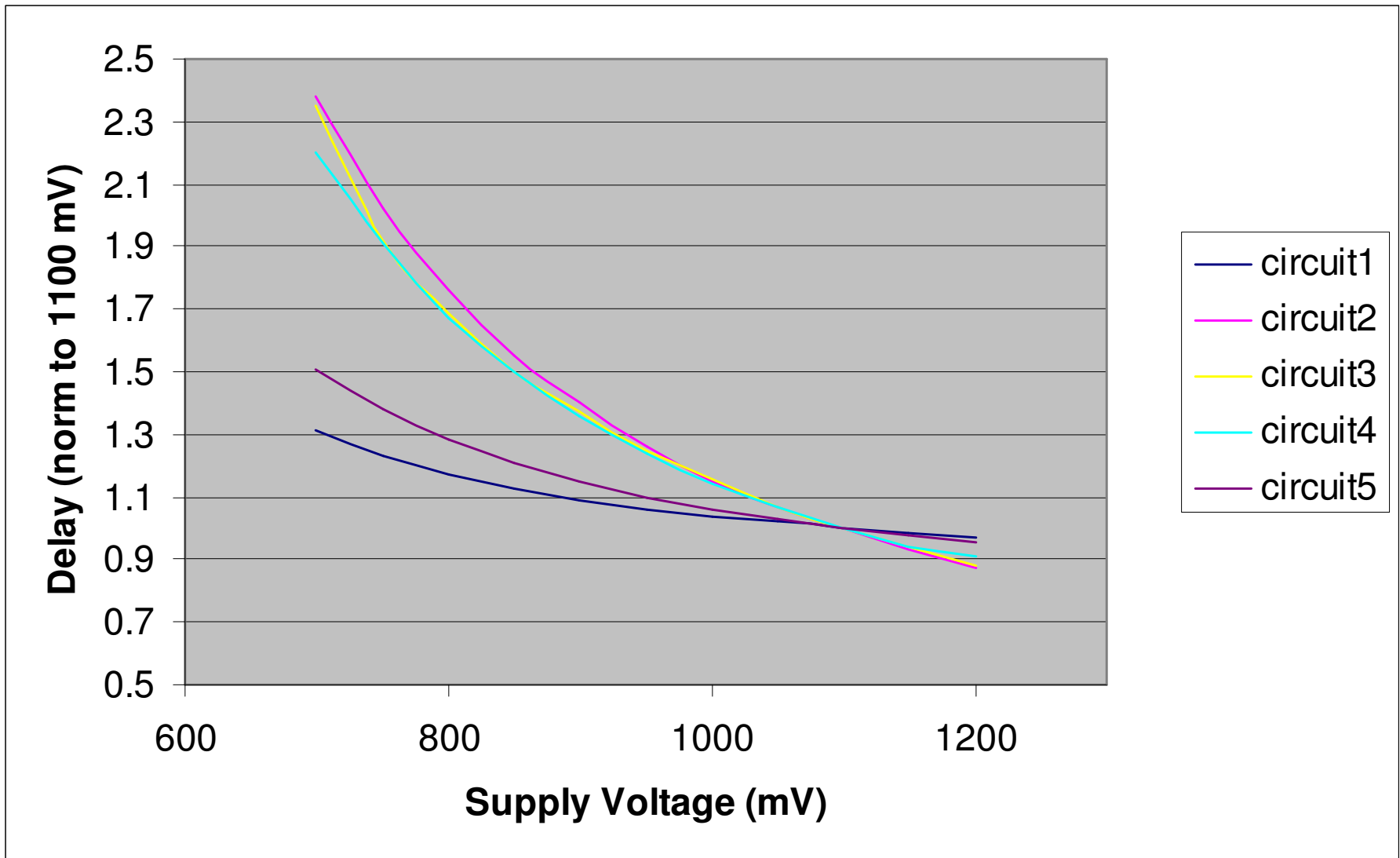
Digital Frequency Divider (DFD) Block Diagram



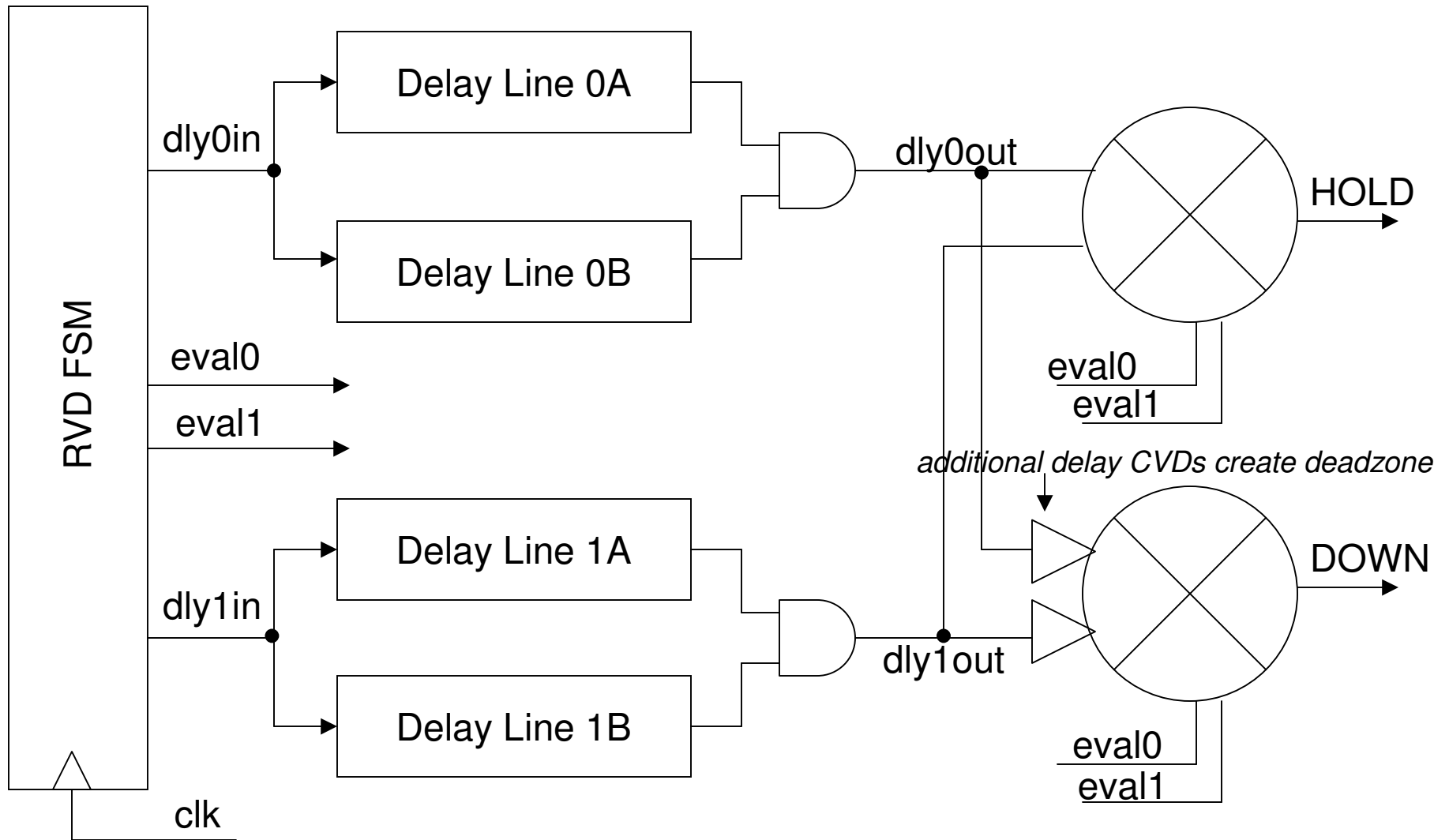
DFD Phase Selection Datapath



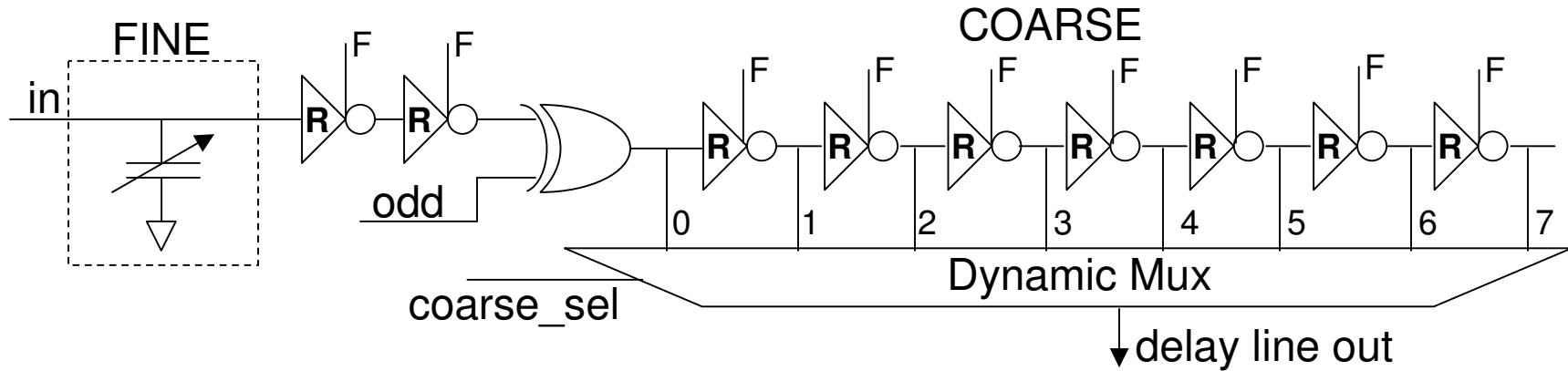
VFC/RVD Voltage Tracking and CMOS Critical Path Scaling



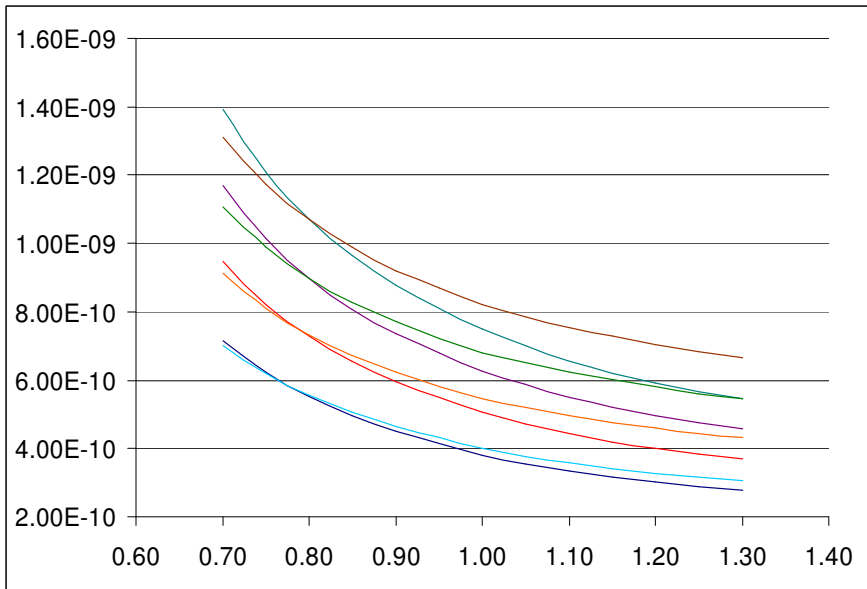
RVD Block Diagram



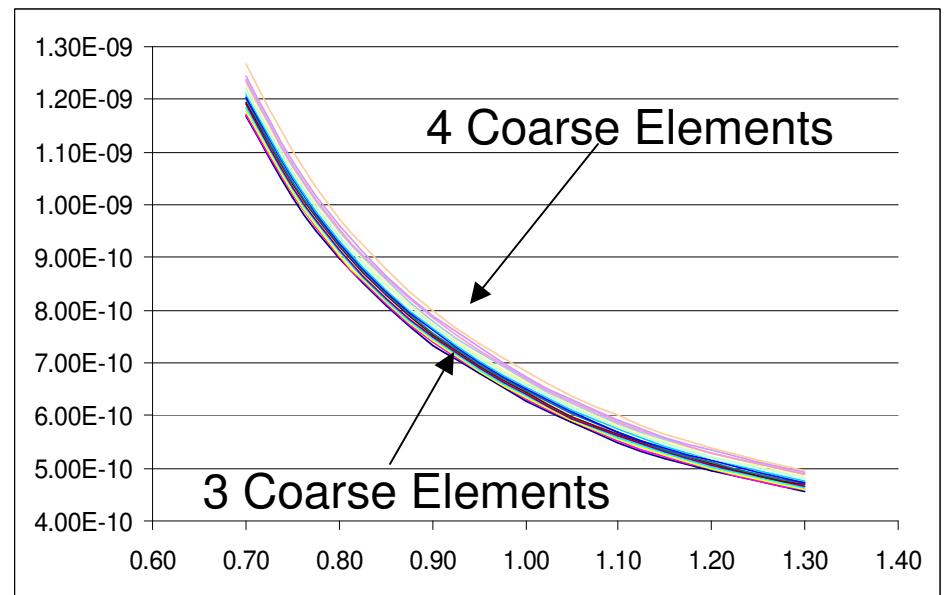
RVD Delay Line



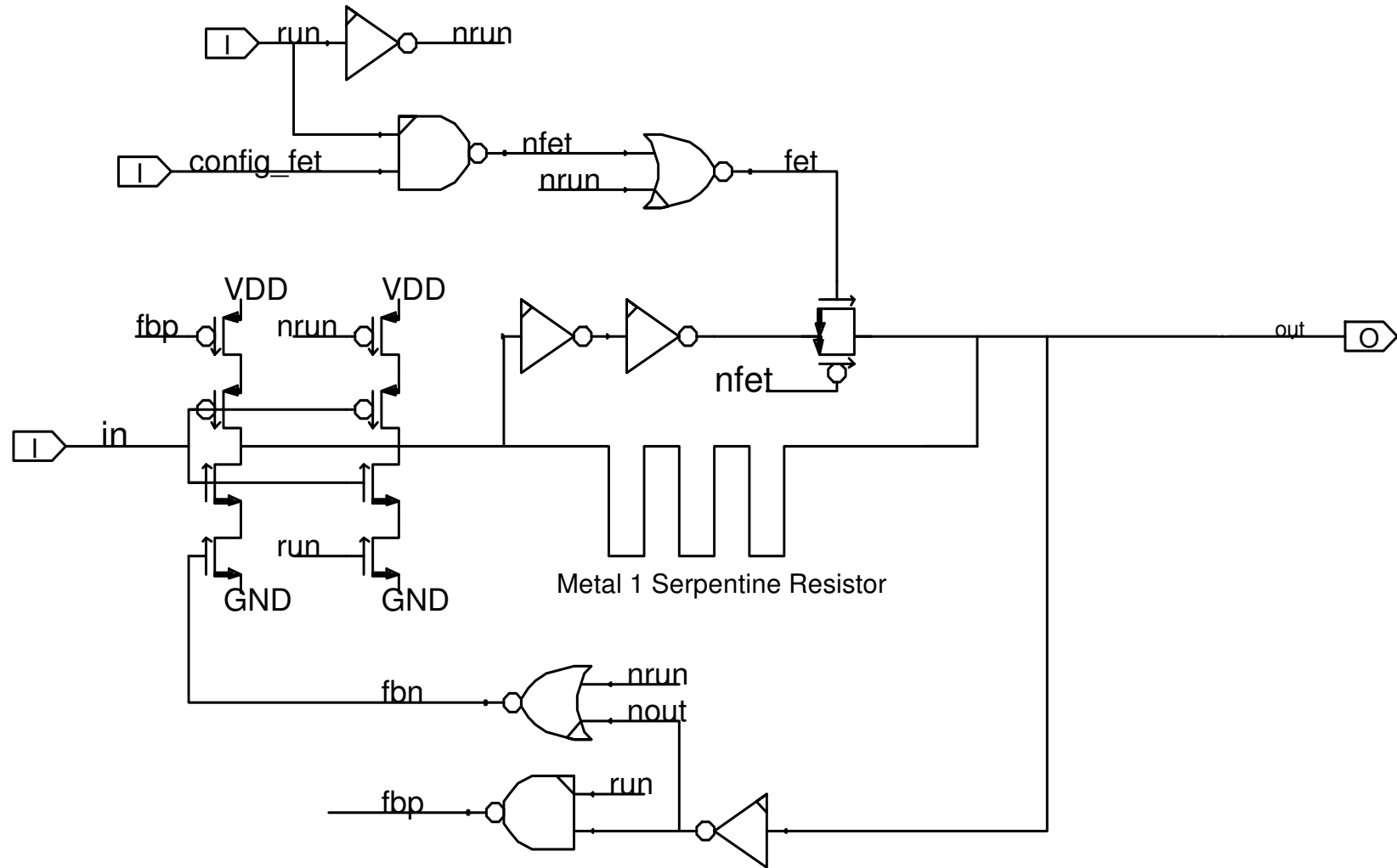
Coarse Delay Incremental Curves



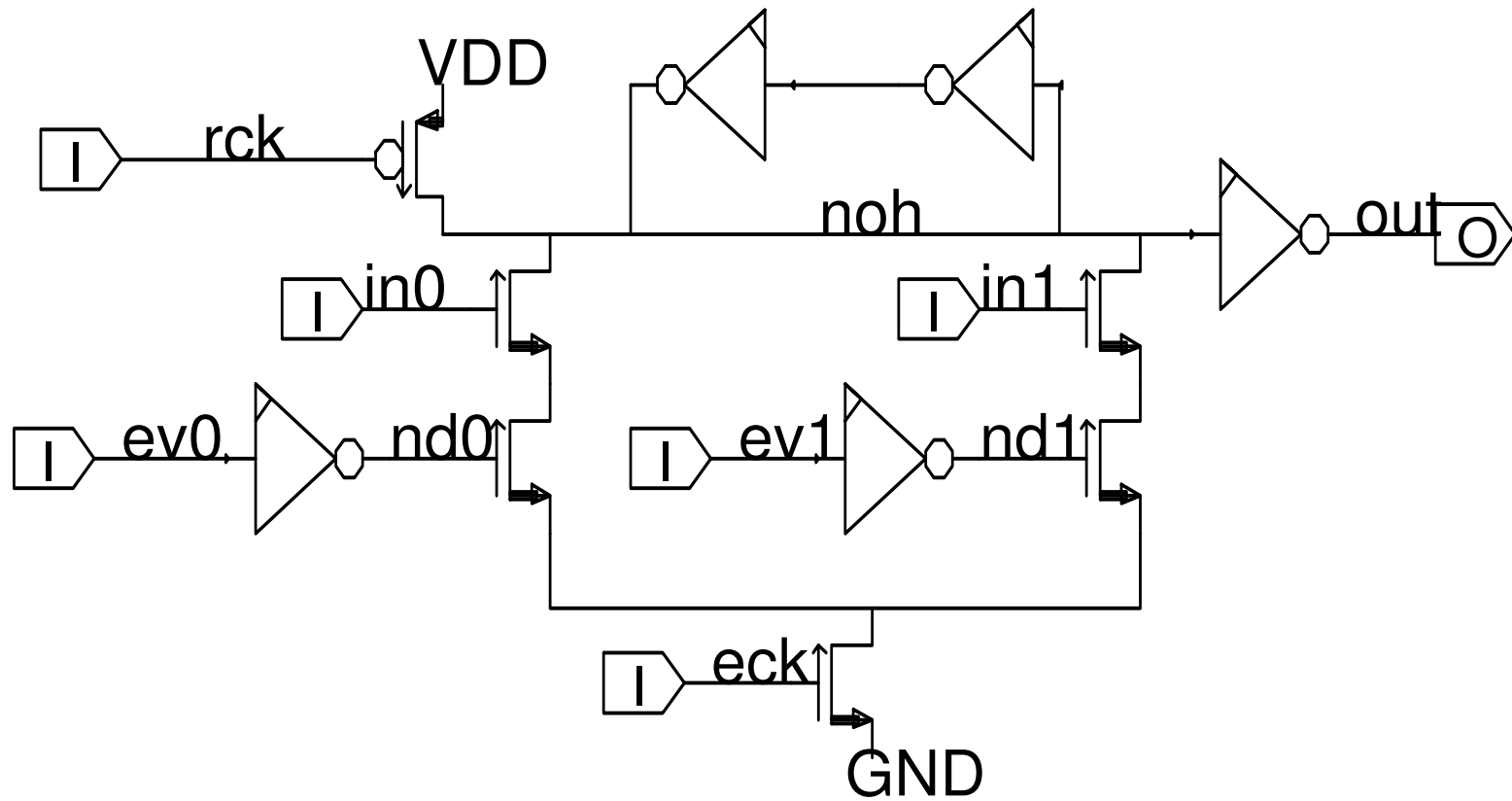
Fine Delay Incremental Curves

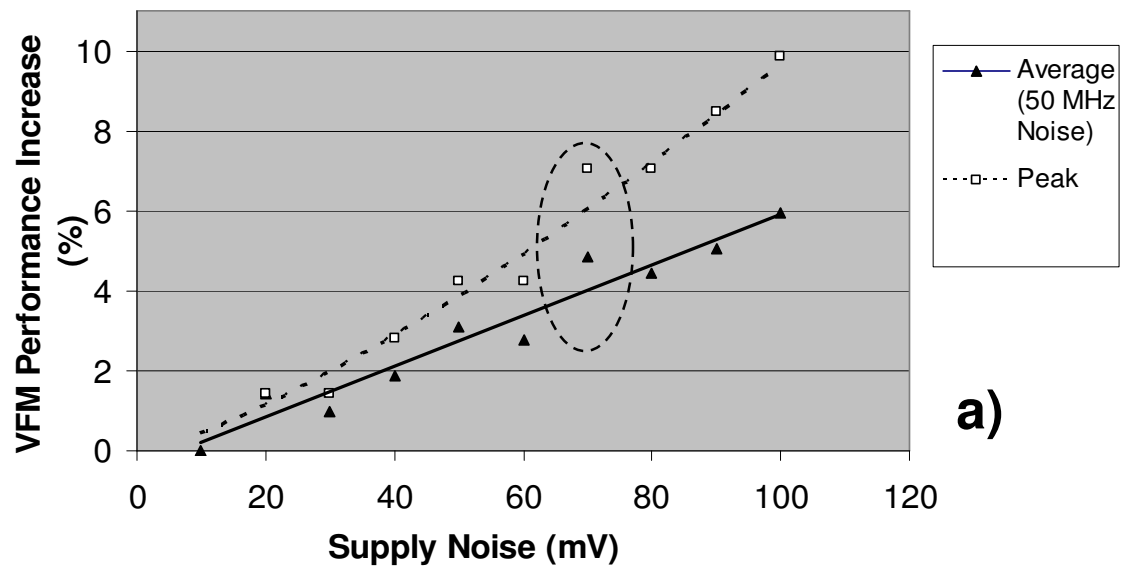


RVD Coarse Delay Element

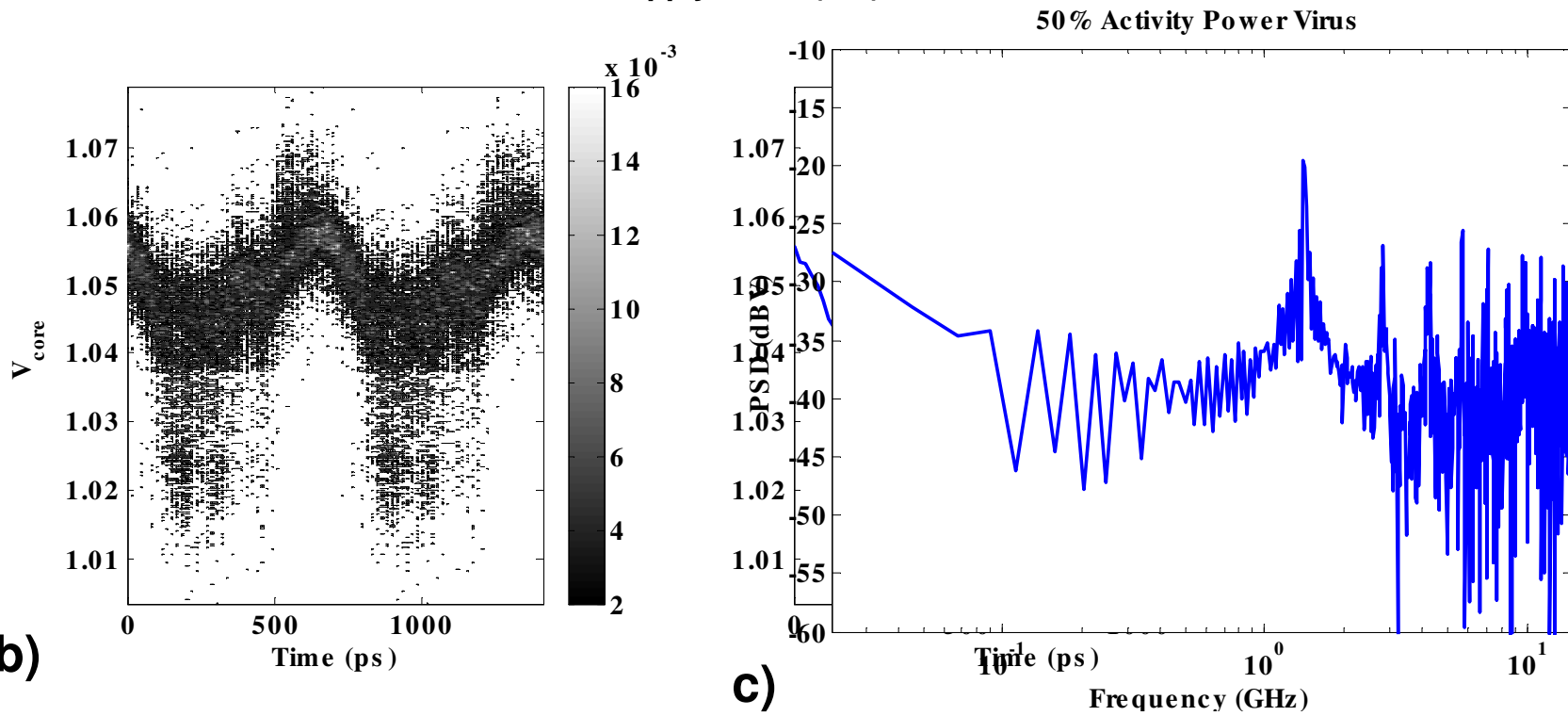


RVD Phase Comparator



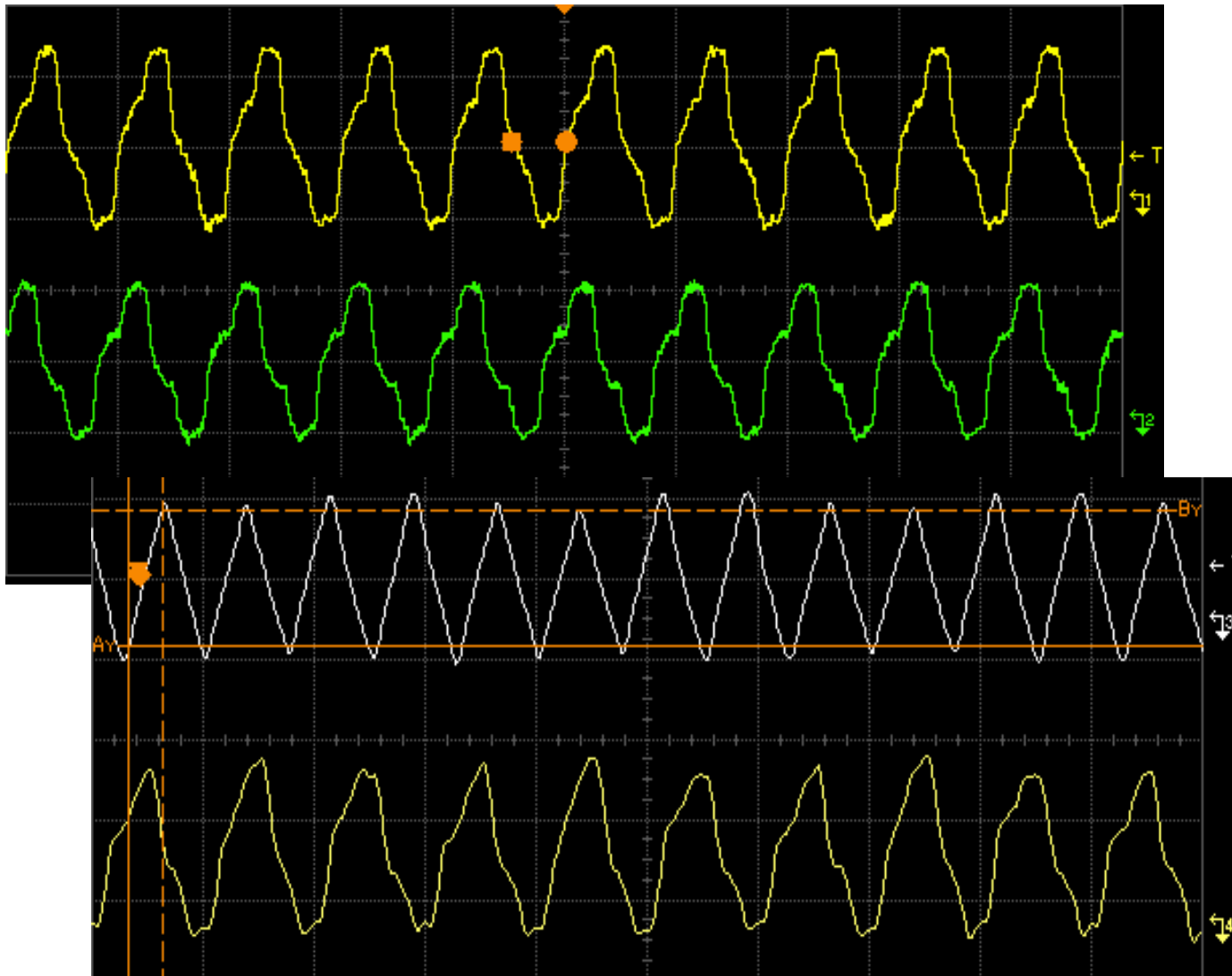


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VFM Performance vs. Supply Noise

FFM/VFM Core/Bus Clock Oscilloscope Traces



FFM, 1.2V

Core clock
1.6GHz

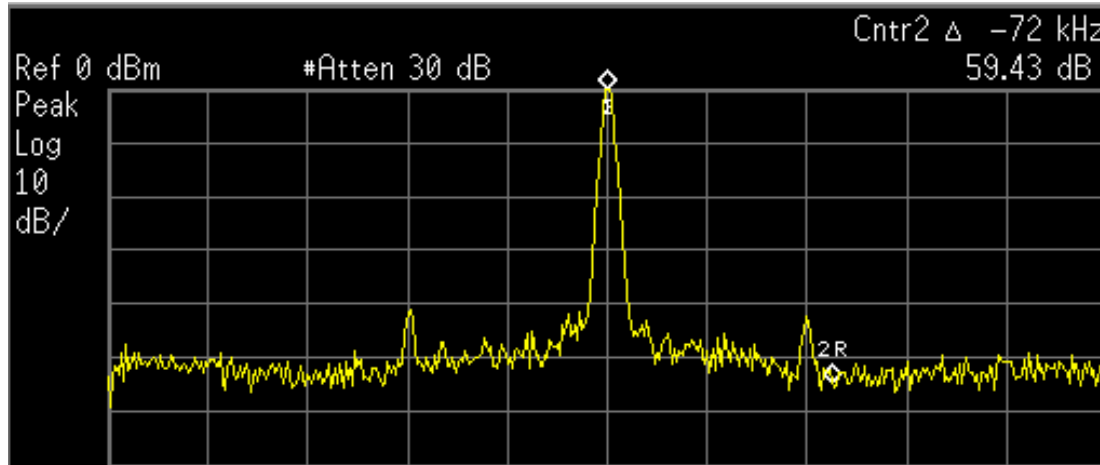
Bus Logic clock
1.6GHz

VFM, 1.2V

Core clock
2.14GHz

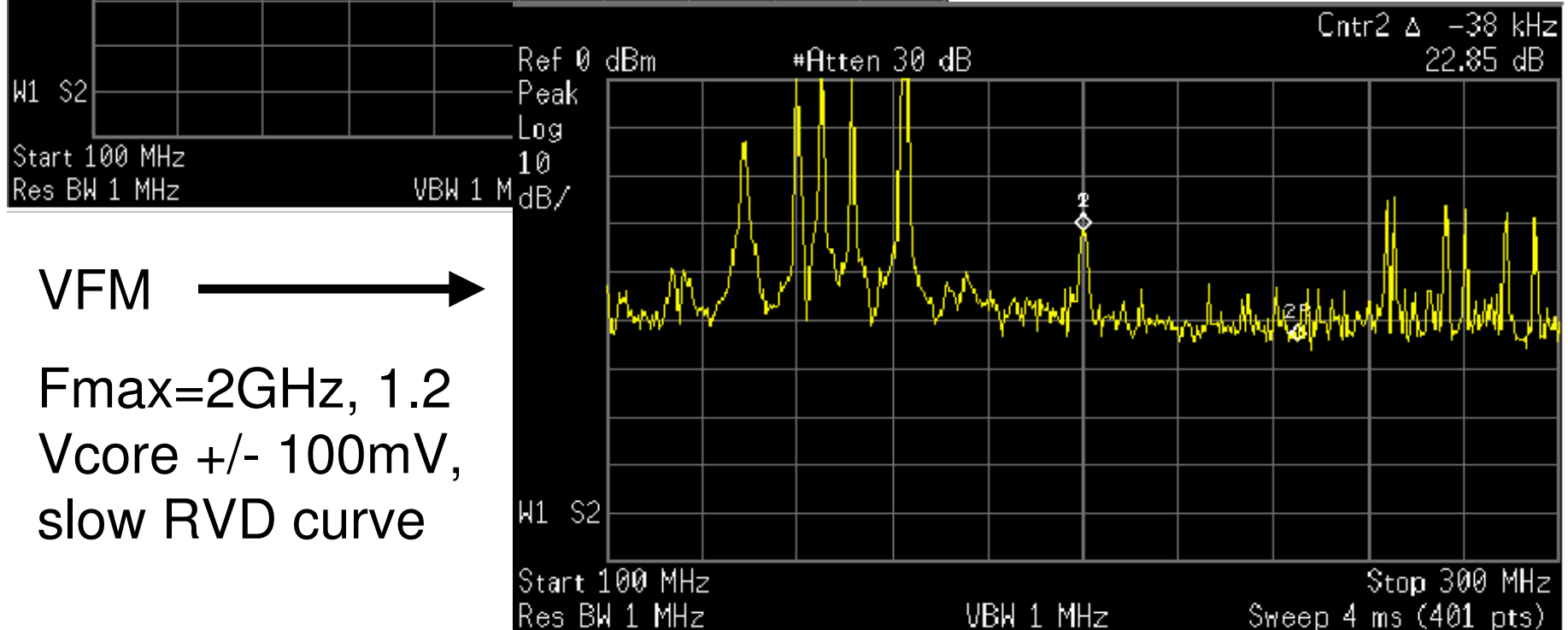
Bus Logic
clock 1.6GHz

Core Clock Spectral Content



← FFM

Fmax=2GHz,
Ffixed=1.6GHz,
1.2Vcore



VFM →

Fmax=2GHz, 1.2
Vcore +/- 100mV,
slow RVD curve

Summary

- Clock system enables a dynamic voltage-scaling power management system (Foxton)
 - Generates low-skew fixed- and variable- frequency clocks
- High-BW Voltage-to-Frequency conversion (VFC)
 - Regional Voltage Detectors
 - Synchronized Digital Frequency Dividers
 - VFC follows programmed V/F response
 - VFC lock onto and tracks local supply voltage
 - Tracks high-BW switching transients: 1 cycle VFC loop response
 - Tracks low-BW Foxton-based supply modulation
- Performance benefits through reduced guardband:
 - Fast response to switching transients (3-8%, path dependent)
 - Tracks process, temperature (3%)
- VFM operation demonstrated above 2GHz

Acknowledgements

E. Fetzer, S. Ghahremani, B. Doyle, A. Barton, M. Peters, S. Hall, J. Desai, E. Lee, F. Verdico, C. Pie, C. Bendele, A. Allen, R. Alley, P. Wyatt, B. Johnson, S. Undy, G. Benjamin, R. McGowen, R. Sandoval, C. Zhu, C. Young, A. Shoning, J. McBride, K. Kerr, D. Newsome, D. Sherlock, B. Haskin, J. Platenak, A. Gouldey, V. Freytag, R. Sims, G. Kumar, J. Pettsinger, R. Weidner, P. Liu, S. Wells, D. Clifford, S. Liepe, J. Ignowski, G. Ranson, P. Kummrow, C. Keen, W. Kever