Loopback Architecture for Wafer-Level At-Speed Testing of Embedded HyperTransport™ Processor Links

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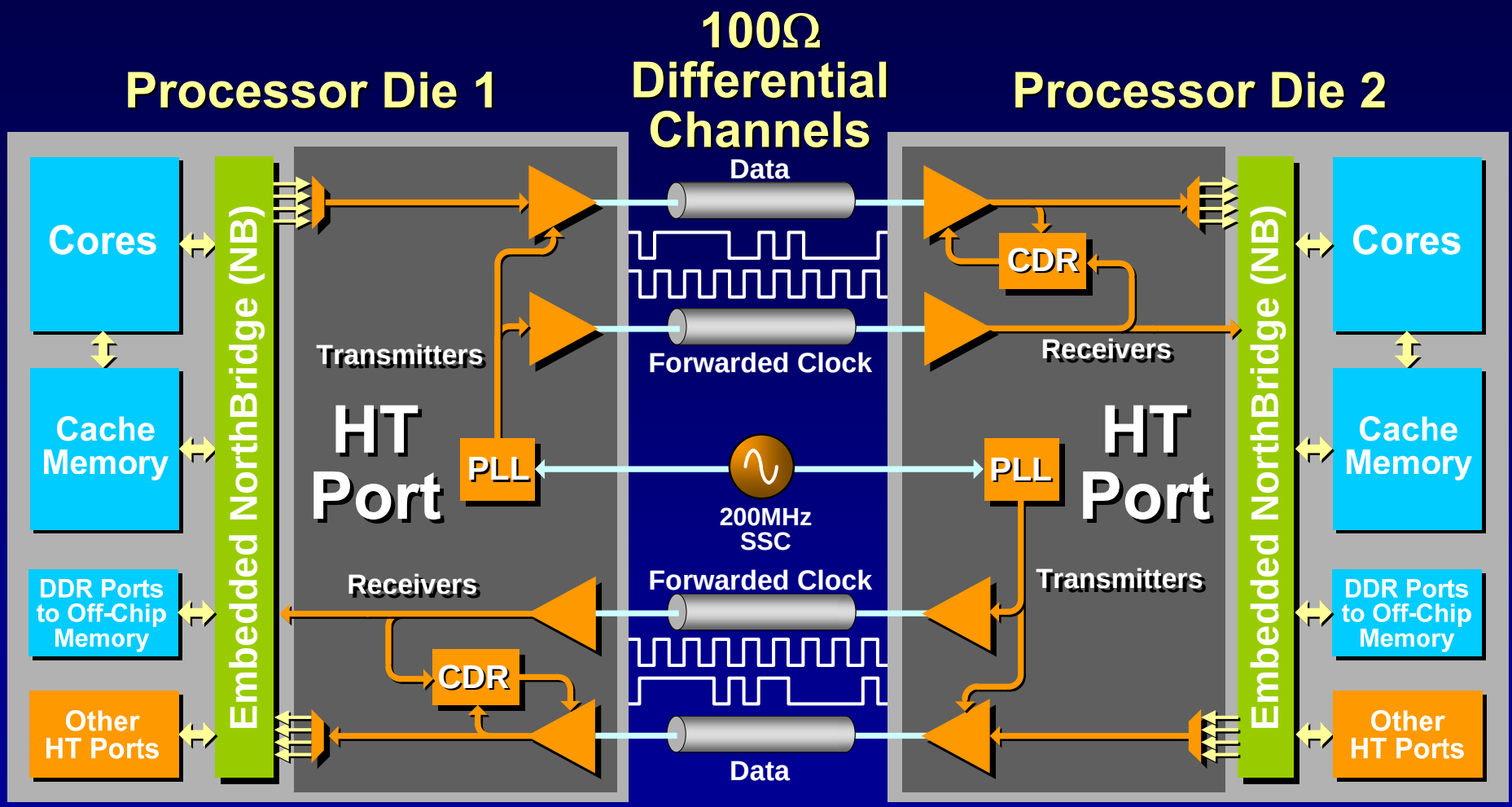
Outline

- Motivation
- HyperTransport™ Overview
- Loopback Implementation
  - Architecture
  - Loopback Channel
  - Transmitter
  - Receiver
- Silicon Results
- Conclusion

Motivation

- Processor dies now talk with each other using full-duplex, bidirectional point-to-point links
  - High-bandwidth, low-latency communication
  - Scalable vs. common FSB architecture
  - e.g., HyperTransport™ (HT) in AMD products
- I/O ports per die is increasing
  - Higher socket counts → more board connectivity
  - MCM embedded links → more package connectivity
- Cost benefit is increasing to sort for functional I/O before packaging, especially for MCMs
- Implement on-chip I/O loopback for *low-cost* at-speed wafer-level testing

Die-to-Die Processor Communication

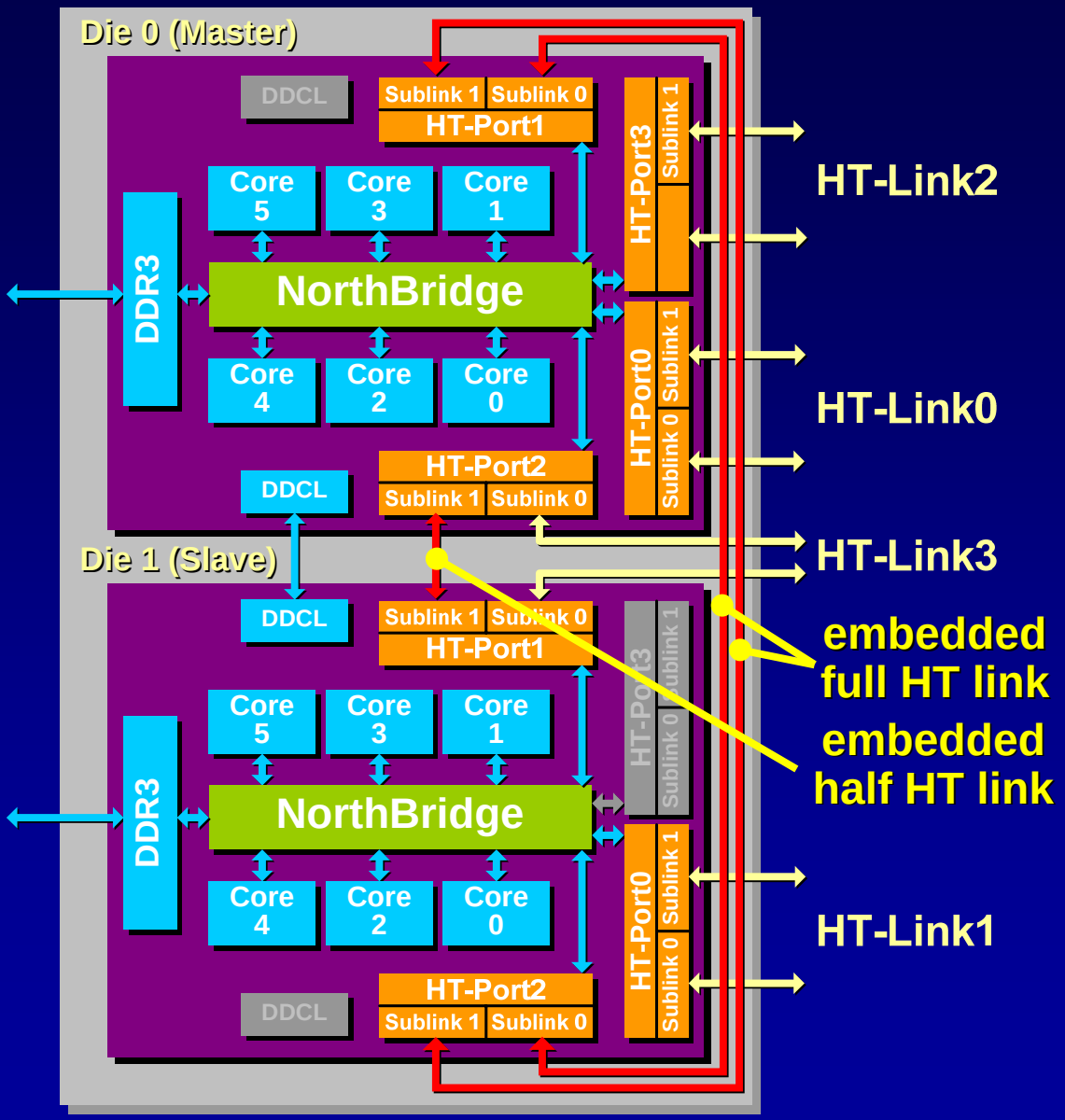


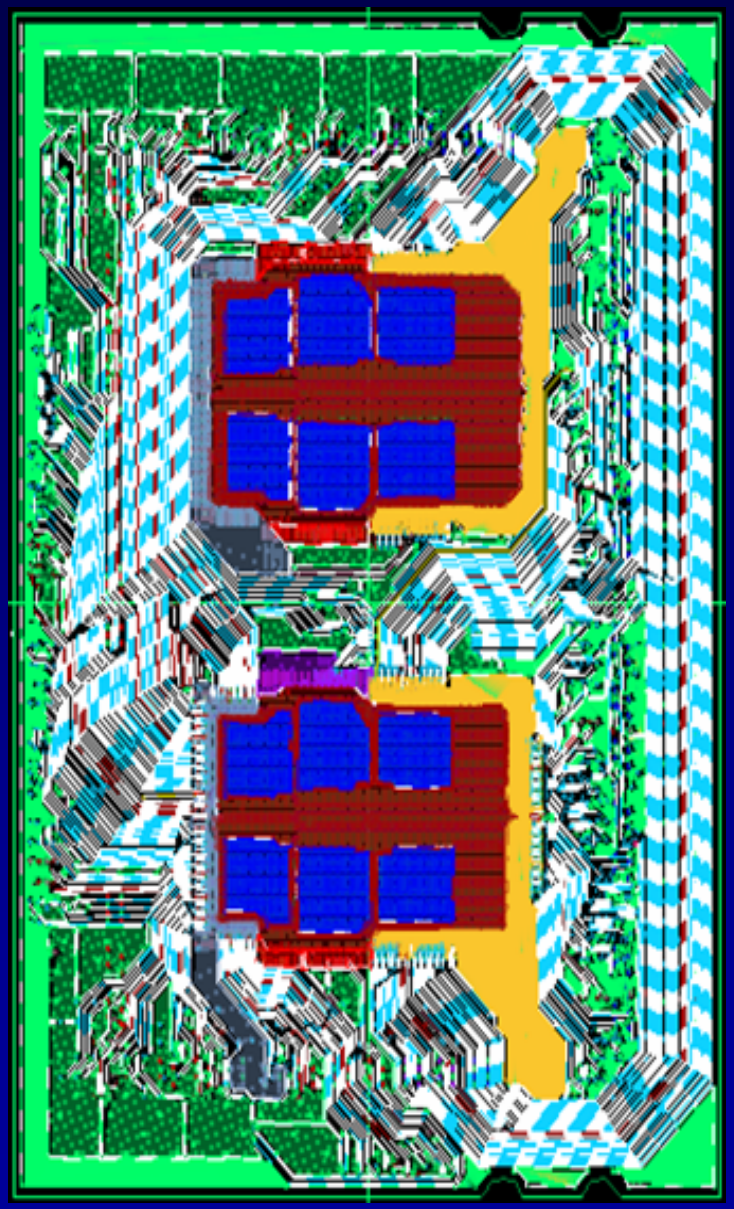
- PCB – max 30” trace + 2 connectors
- MCM substrate – 4” trace

HyperTransport™ (HT) Overview

- Source synchronous
  - Forward half-rate clock for RX data retiming
  - Common-mode jitter rejection, low latency
- 0.4 to 6.4Gb/s (0.4Gb/s steps) – NRZ PAM-2
- 20 lanes per direction (split into 2 sublinks)
  - 1 CLK & 9 data (CAD/CTL) lanes per sublink
- HT1 (0.4–2.0Gb/s)
  - CDR bypassed, data RX simply retimed by CLK RX
- HT3 (2.4–6.4Gb/s)
  - DLL-based CDR aligns received forwarded CLK to received data transitions for lower BER retiming

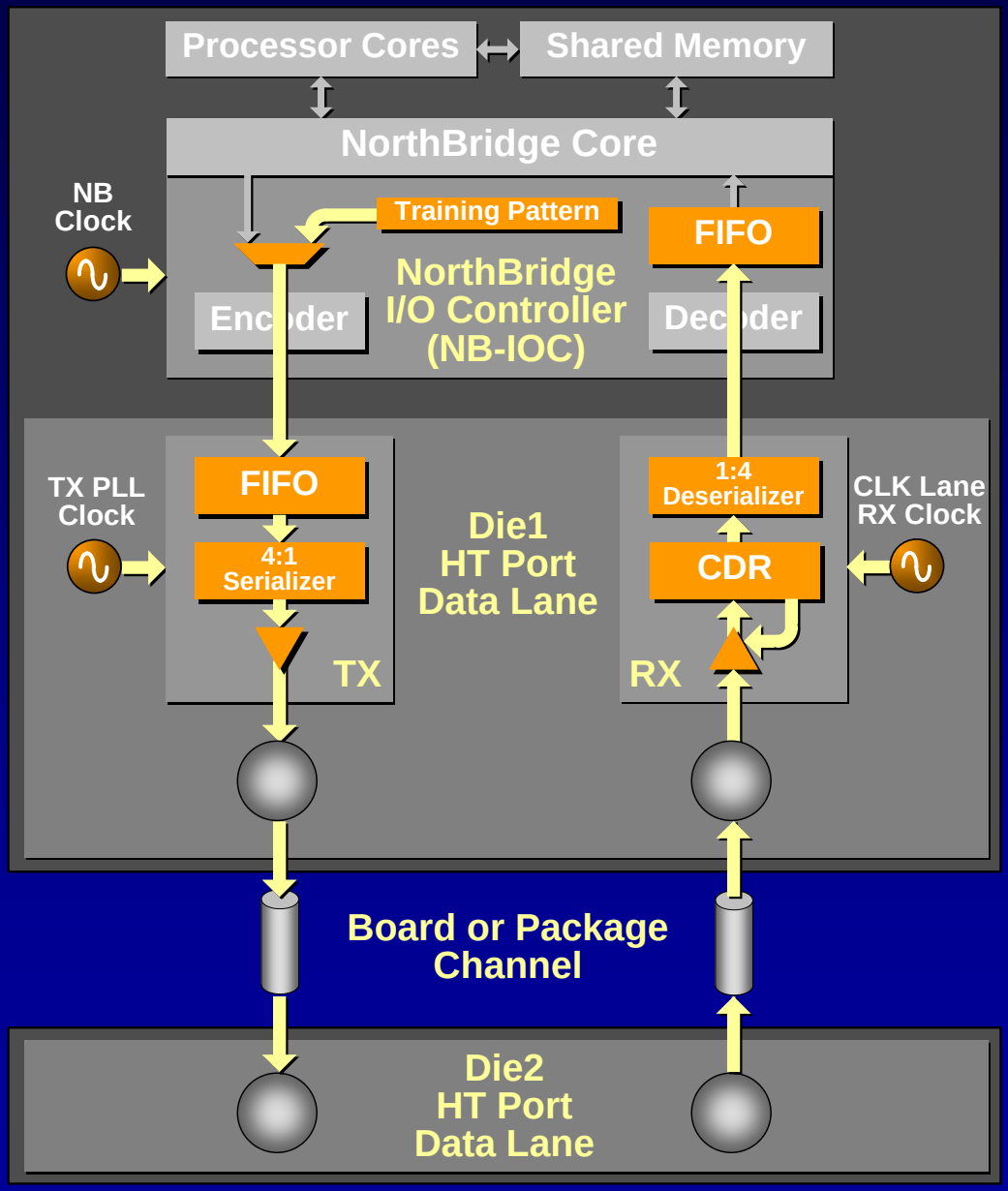
Opteron™ 6000 Processor (G34 MCM)





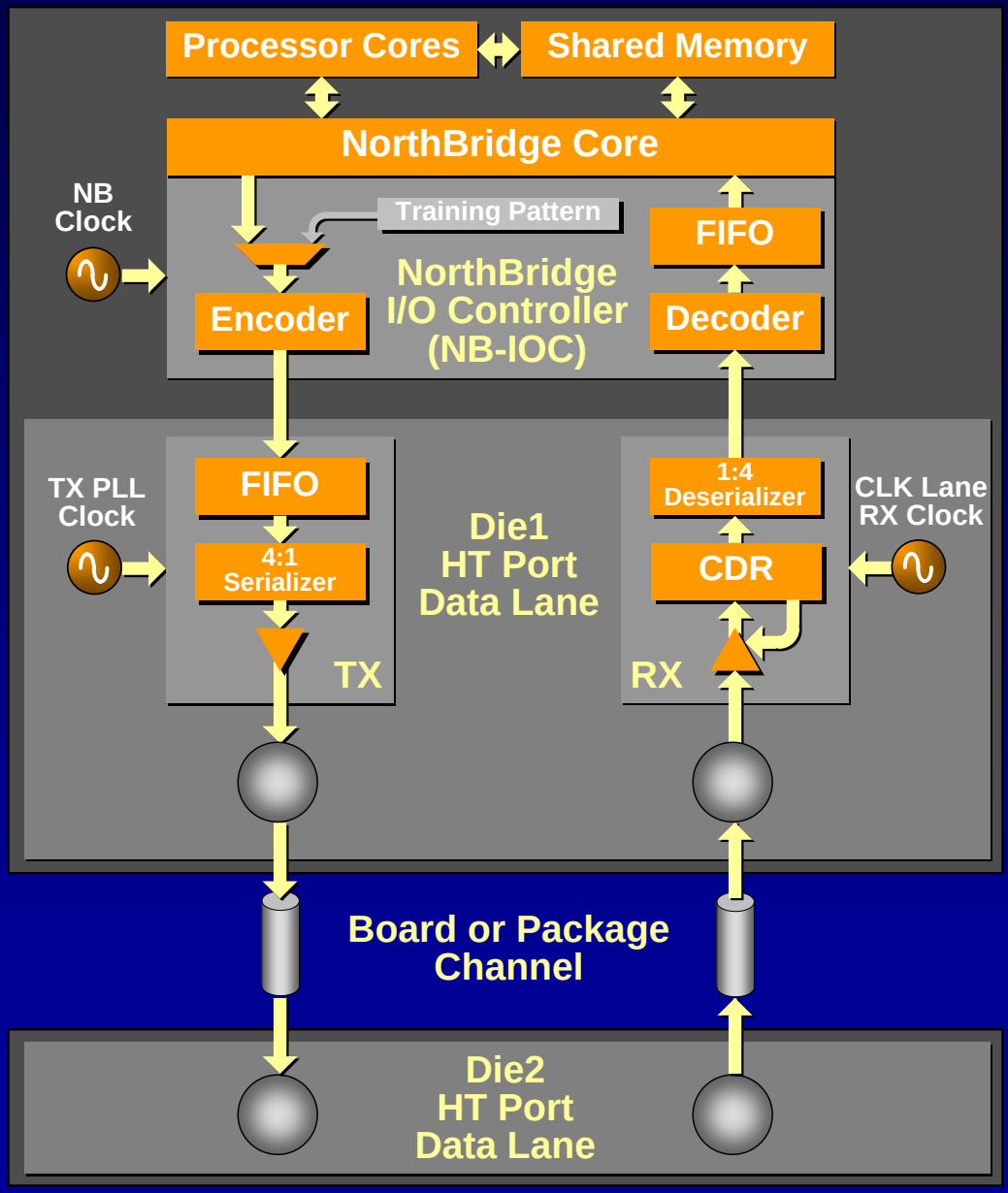
HT Link Training (Handshaking)

- Coordinated by NB-IOC in both dies
- Each NB-IOC sends predefined training pattern to the other die
- Training arms CDR to align clock to data & signals start of data transfer
- # data lanes enabled depends on link traffic



HT Data Transfer

- Data transfer starts immediately after last bit of training
- Once data transfer is completed, HT port is disabled into one of several possible sleep states for power saving
- Data is scrambled by XOR or by 8b/10b to reduce ISI



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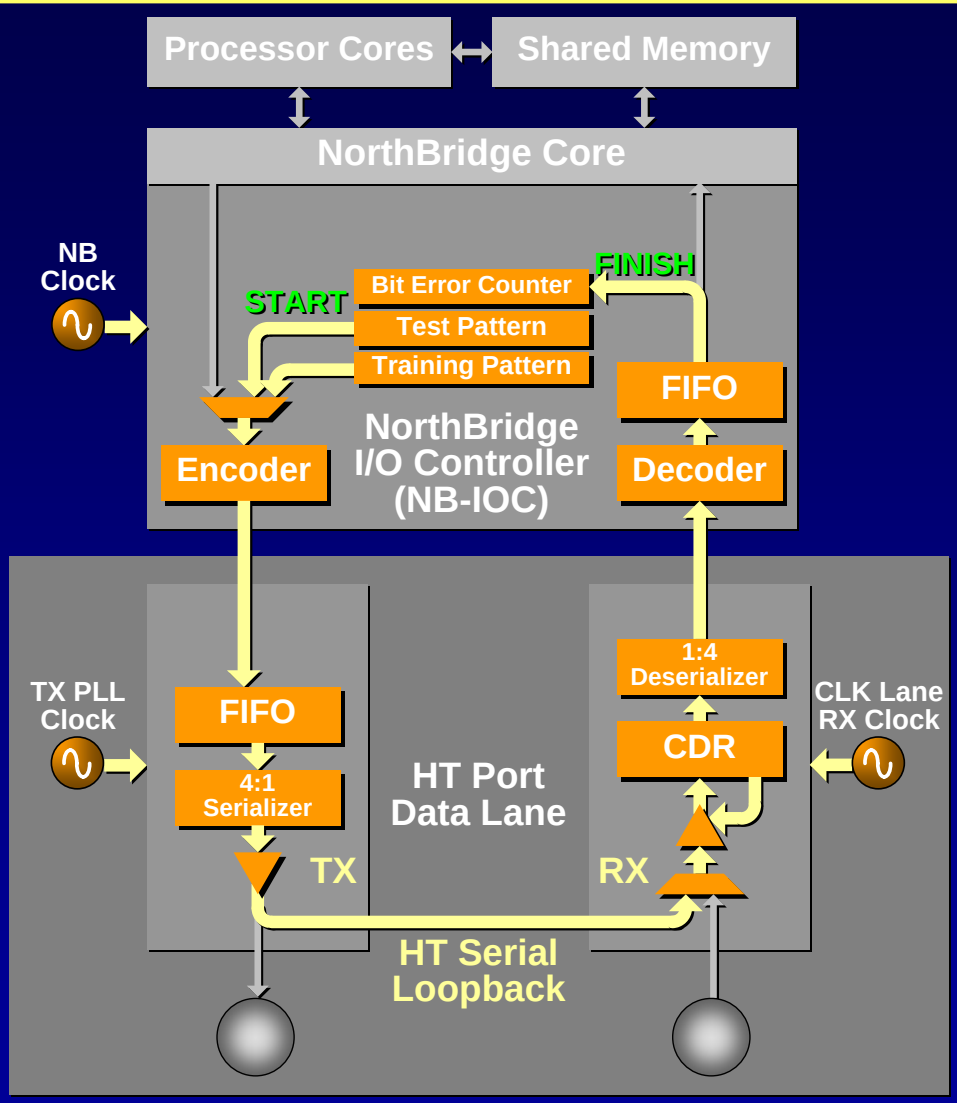
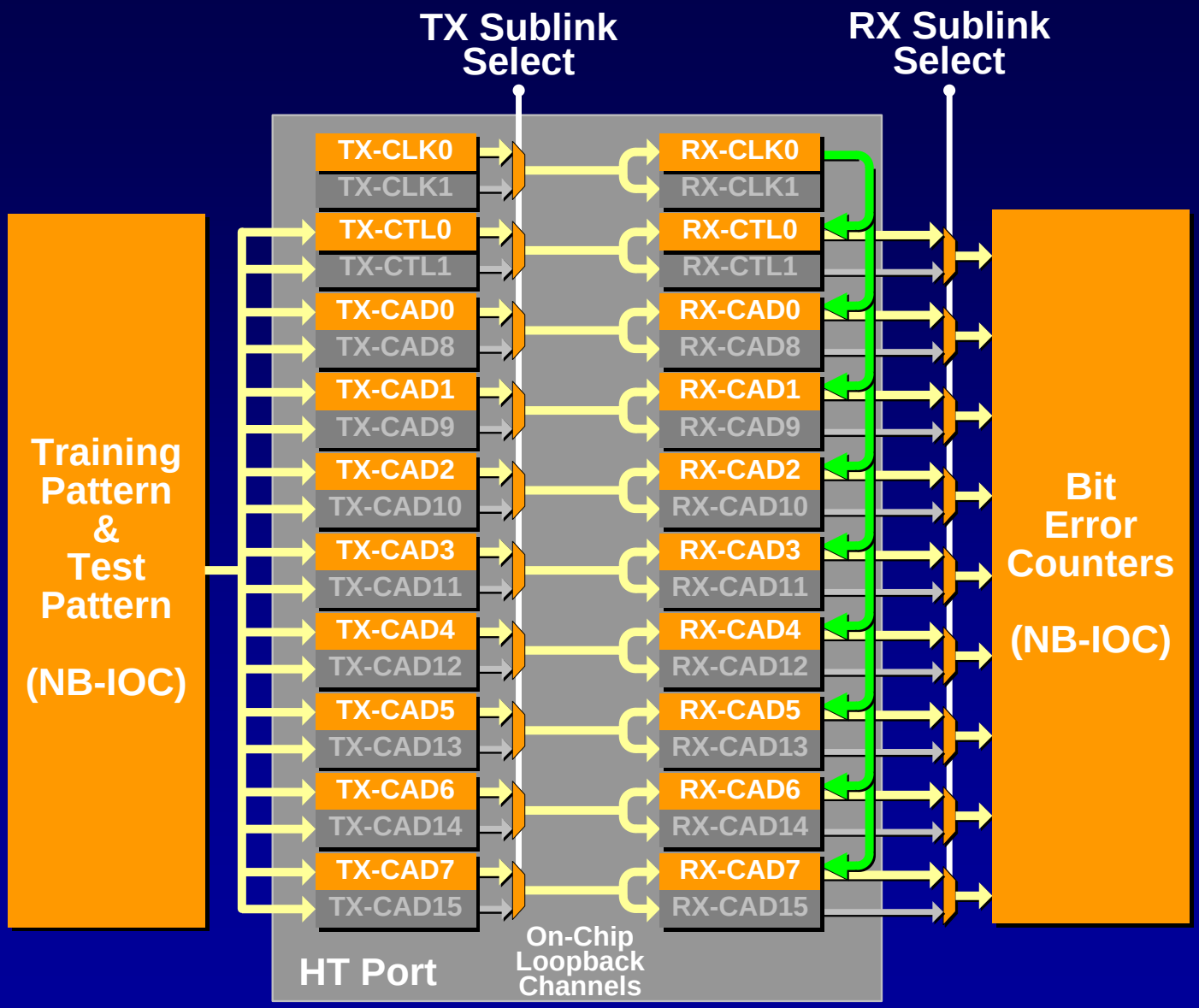
Enabling Internal Serial Loopback

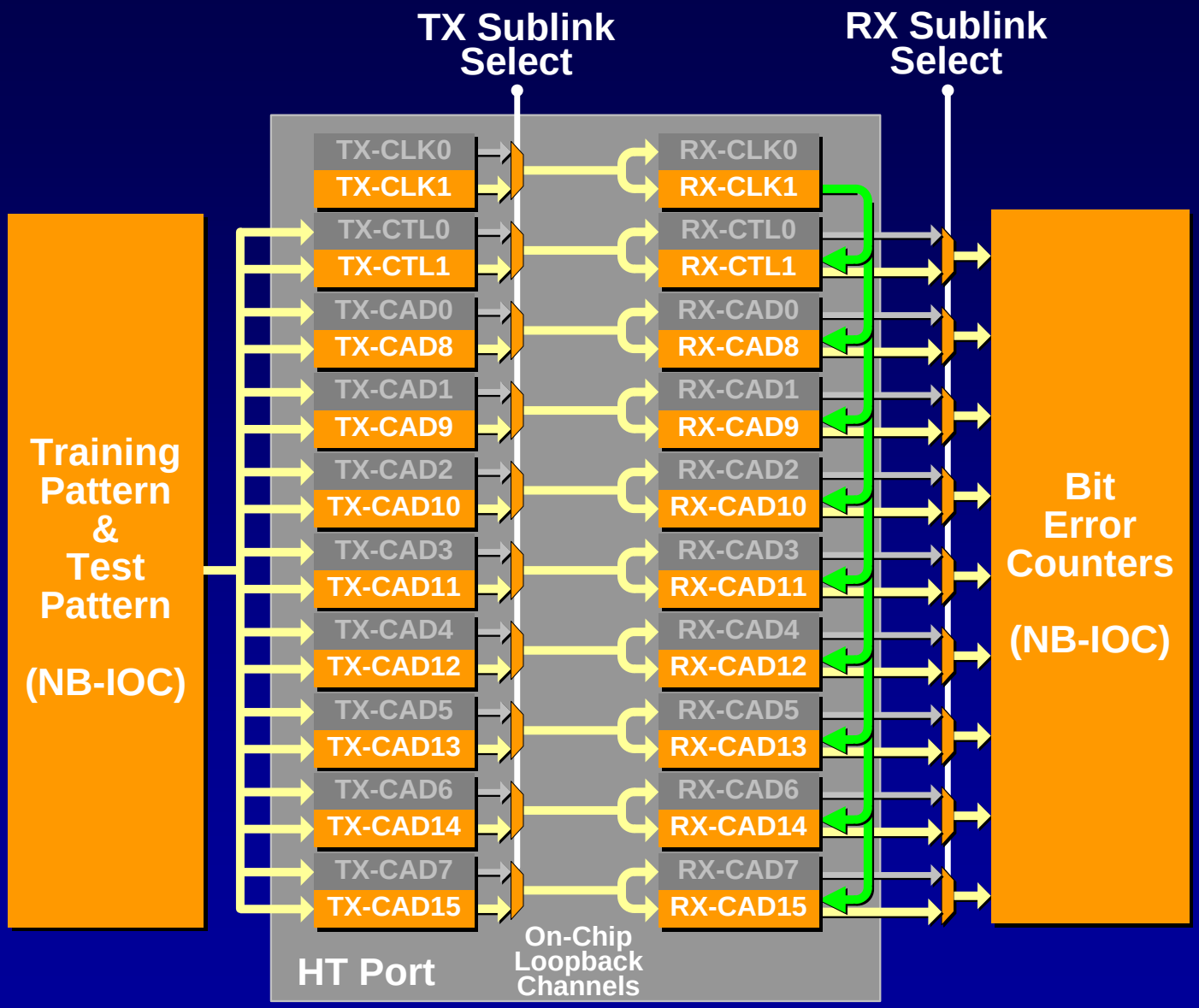
- TX→RX serial loopback via on-chip channel
- No external channel required, hence test can be performed at wafer-level sort
- NB-IOC initiates link by sending training bits, then user-specified test pattern
- RX is *self-trained* using bits sent by own TX
- Controlled by JTAG



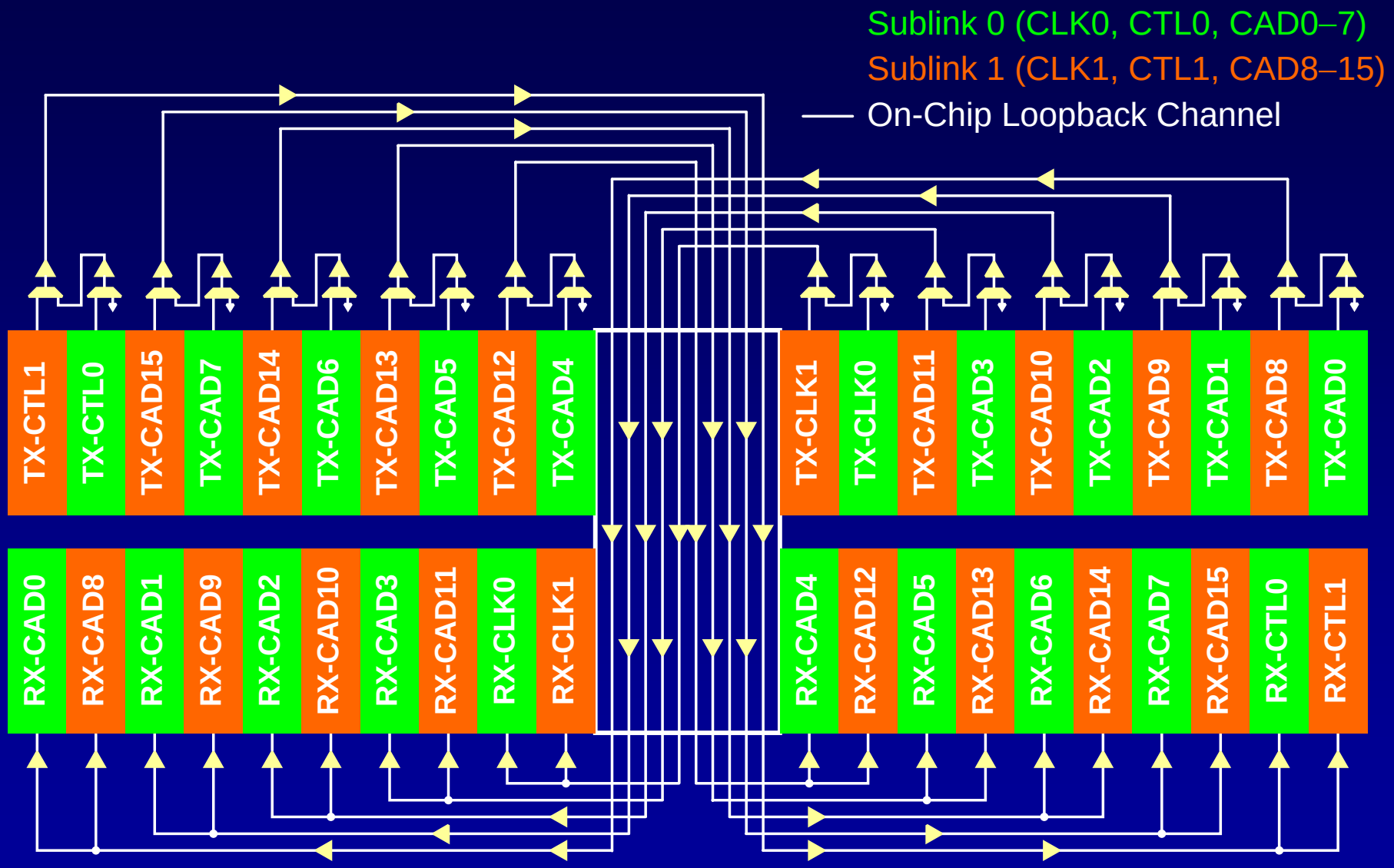
Sublink0 Loopback



Sublink1 Loopback



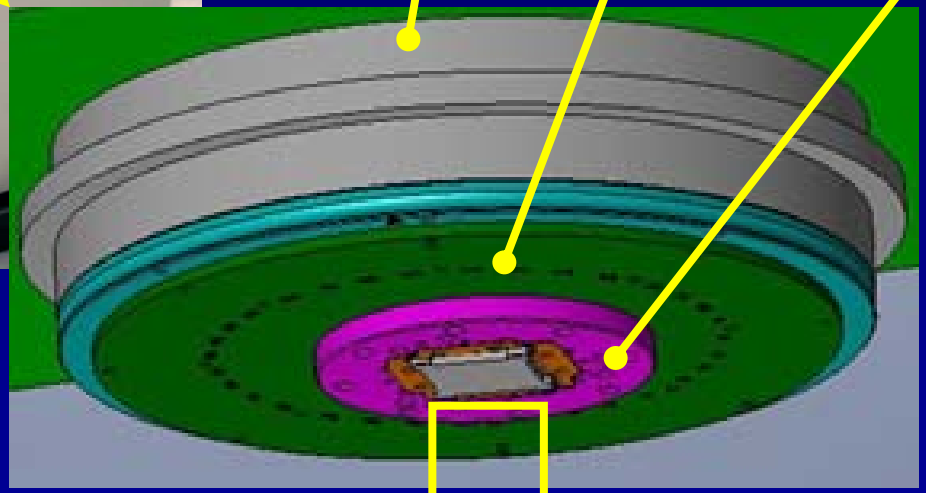
Transceiver Loopback Floorplan



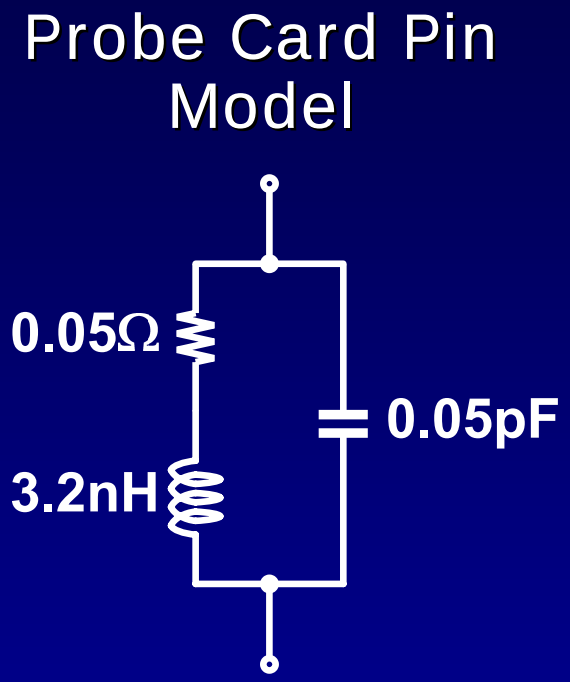
Horizontal HT Port shown

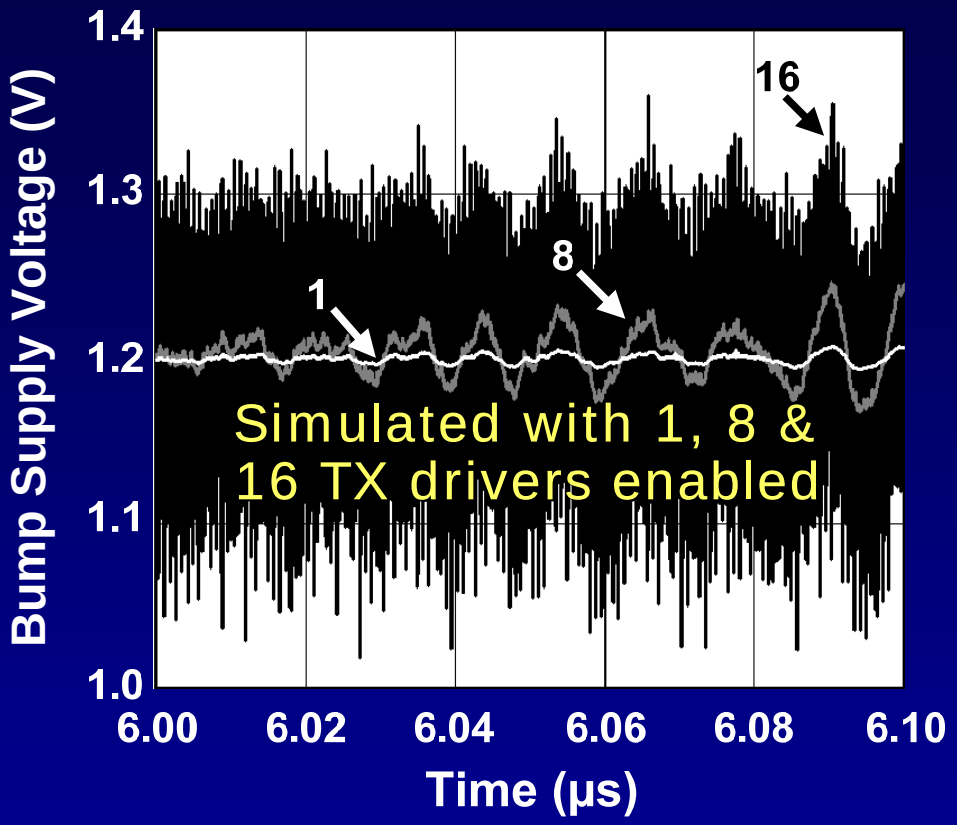
Wafer-Level Testing

LTX Sapphire platform



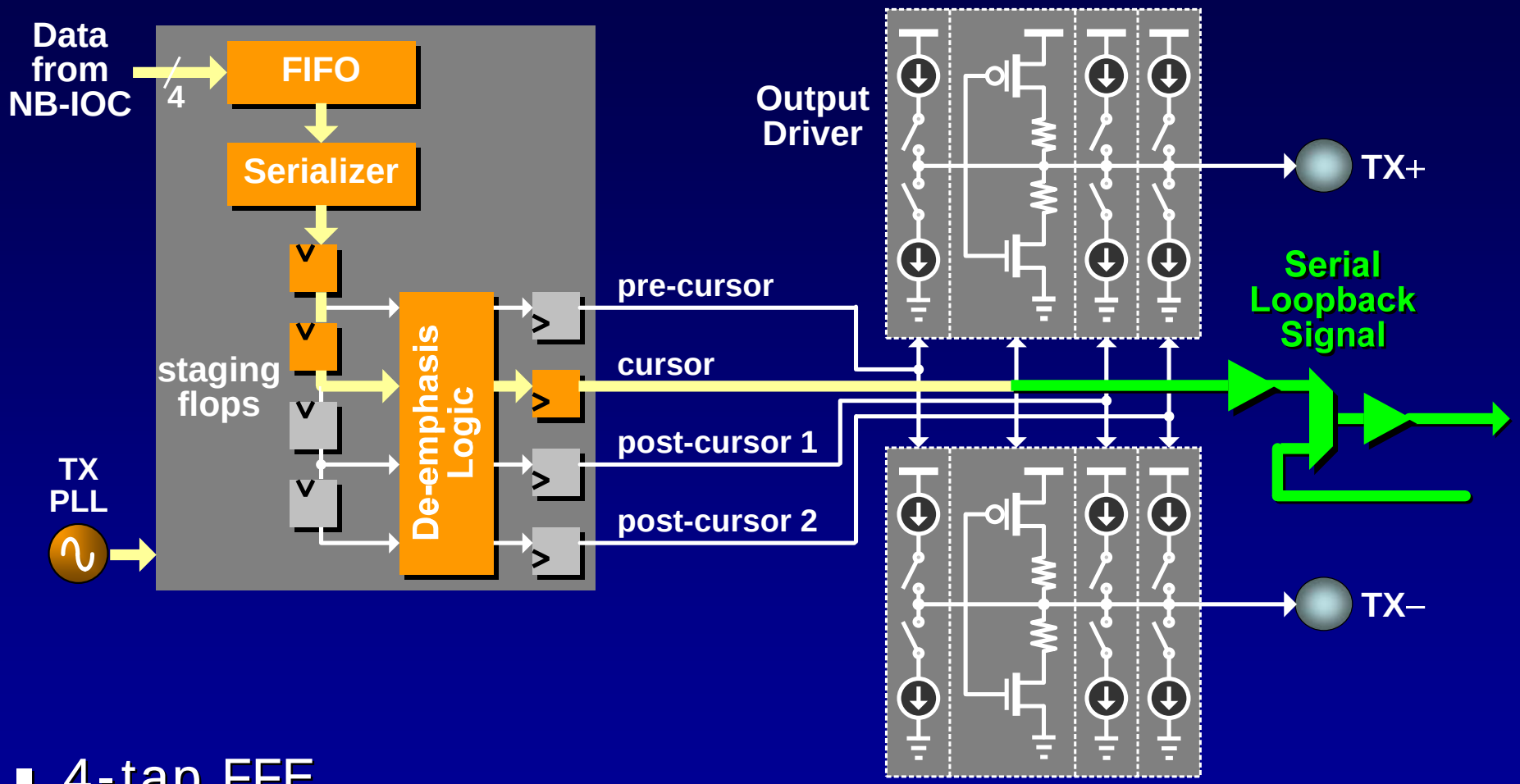
Wafer-Level Test Supply Noise





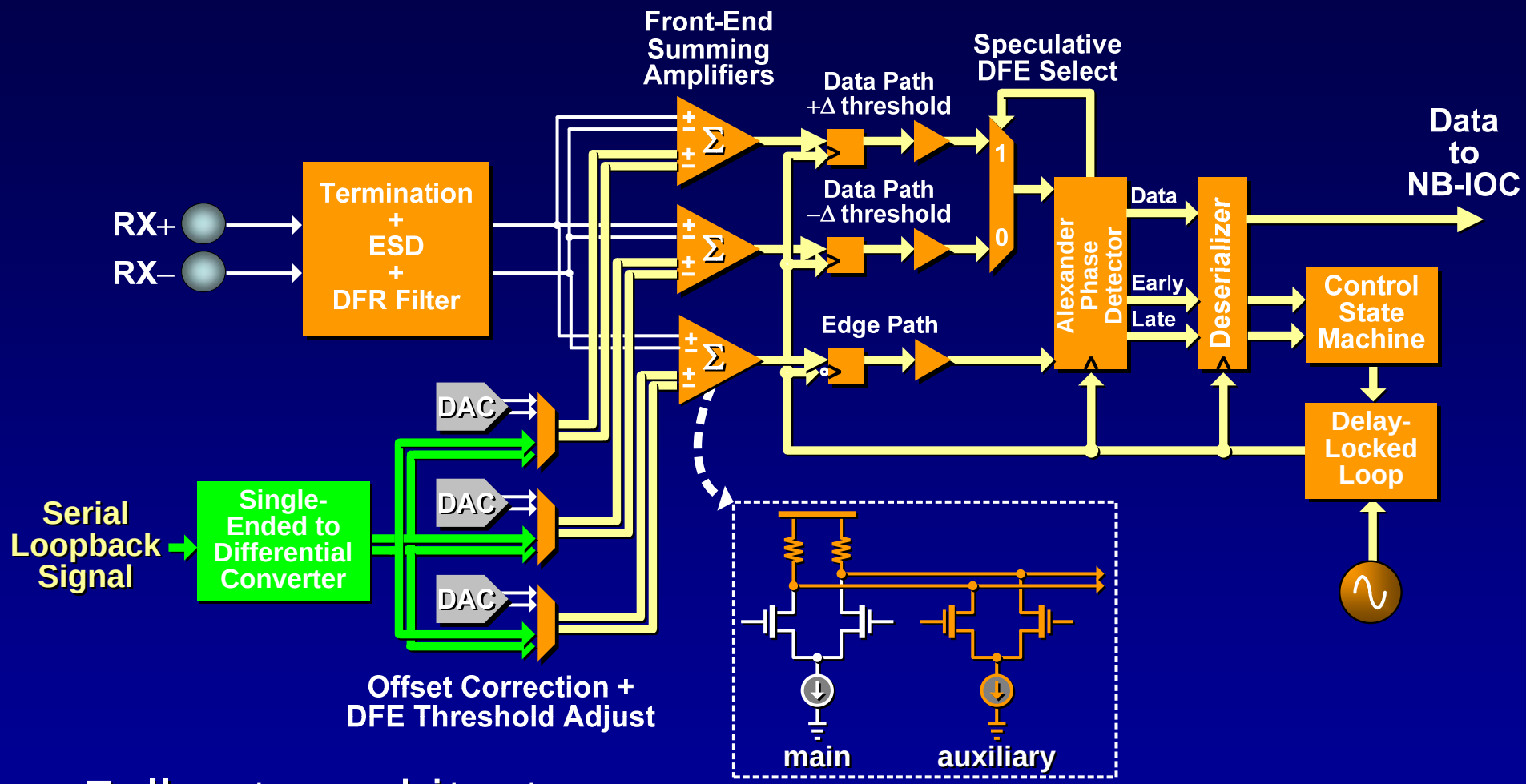
- Comes primarily from TX driver switching high currents through probe card pin inductance
- Can disable any TX driver per sublink during loopback

TX Loopback Implementation



- 4-tap FFE
- Hybrid V-/I-mode output driver

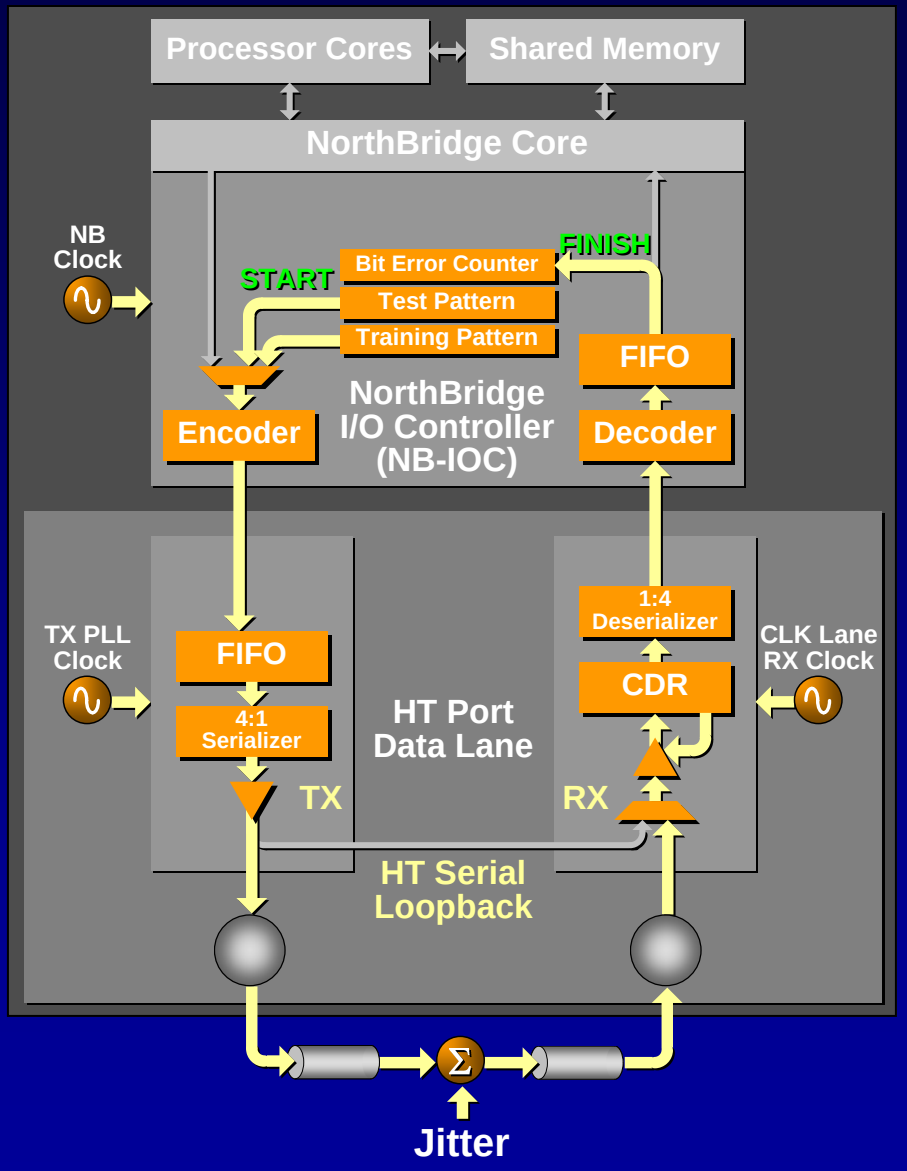
RX Loopback Implementation



- Full-rate architecture
- Equalization: 1-bit speculative DFE + analog DFR filter

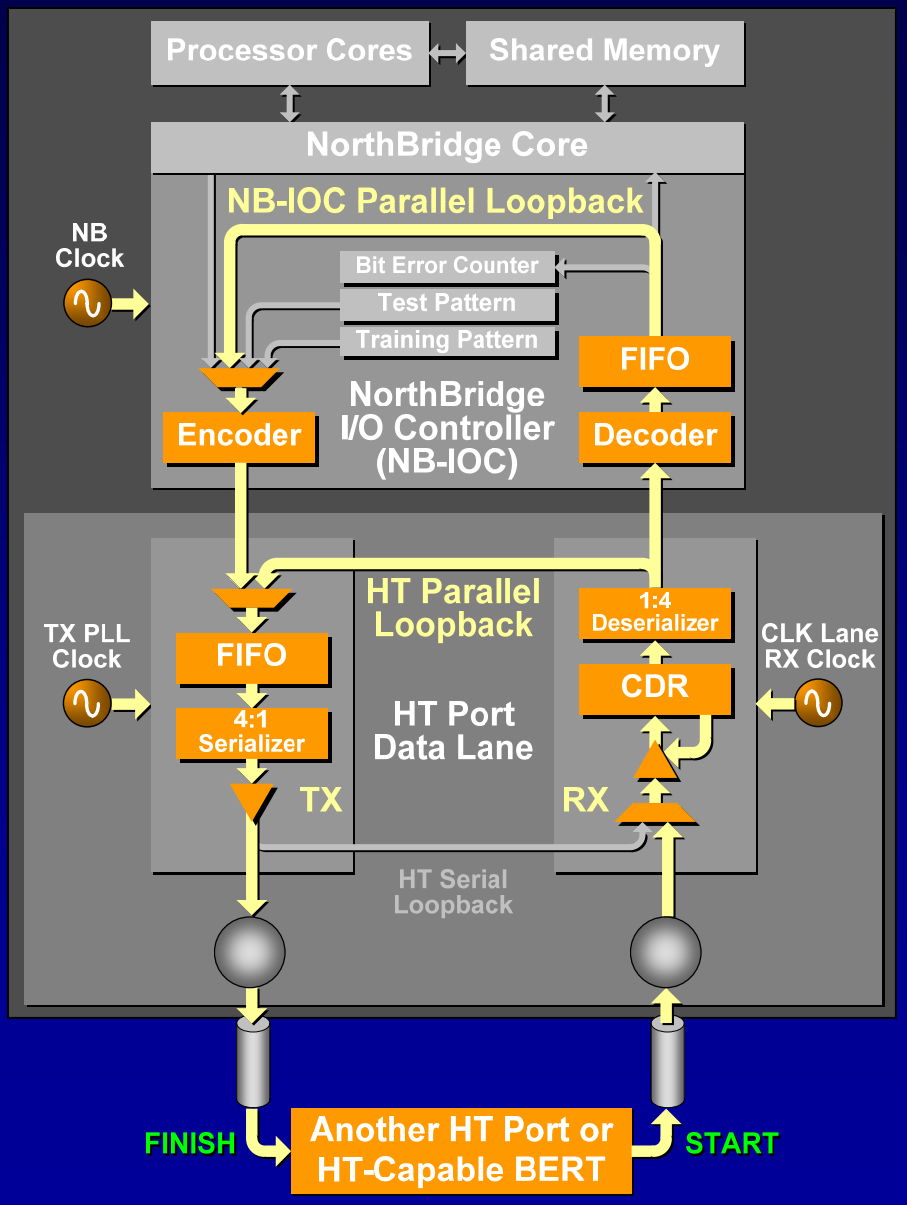
External Serial Loopback

- Package-level sort test
- Provides test coverage not exercised by internal serial loopback
  - TX output driver
  - RX analog front end
  - TX & RX equalization
- Can inject jitter into external channel for eye margining



Parallel Loopback Modes

- Package-level sort test
- RX→TX parallel loopback in HT or in NB-IOC
- Requires another HT port or BERT to initialize link & provide test pattern to RX
- Enables fault isolation



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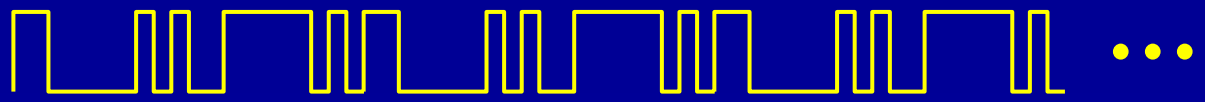
Loopback Test Description

- Wafers
  - 12” bumped AMD Opteron™ 6000 processors (45nm SOI-CMOS)

Conway *et al.*, *Hot Chips* 2009

- Test conditions
  - 1.1V, 1.3V
  - 5.2Gb/s, 6.4Gb/s
- Test pattern
  - 10^8 cycles of alternating +K28.5 & –K28.5
  - Passing test → BER < 5×10^{-10}



Early Example of Test Sort Results

Die No.	HT Loopback Fail Description
1	Port3 Sublink0 @ 6.4Gb/s – 1.1V CAD2 bit error count = 63 (saturated)
2	Port0 Sublink0 @ 6.4Gb/s – 1.1V CAD2 bit error count = 2
3	Port0 Sublink0/Sublink1 @ 5.2,6.4Gb/s – 1.1,1.3V Training failure in all CTL/CAD lanes
4	Port0 Sublink0 @ 6.4Gb/s – 1.1,1.3V CAD2 bit error count = 63 (saturated)
5	Port3 Sublink0 @ 6.4Gb/s – 1.1V CAD4 bit error count = 63 (saturated)
6	Port0 Sublink0 @ 6.4Gb/s – 1.1V CAD0 bit error count = 2
7	Port2 Sublink0 @ 6.4Gb/s – 1.1V CAD4 bit error count = 63 (saturated)

Conclusion

- Transceiver loopback enables wafer-level at-speed testing of HyperTransport I/O
- Demonstrated 6.4Gb/s test functionality
- Entirely digital architecture for simple implementation & verification
- Significantly improves package-level yield, especially for more expensive MCM packages
- Adds no extra sort infrastructure cost
- Established test for wafer-level screen of AMD 45nm products

Acknowledgments

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