SSCS DLP, Fort Collins

Wide band RF CMOS circuit design techniques

Domine Leenaerts

Semiconductors, The Netherlands

Content

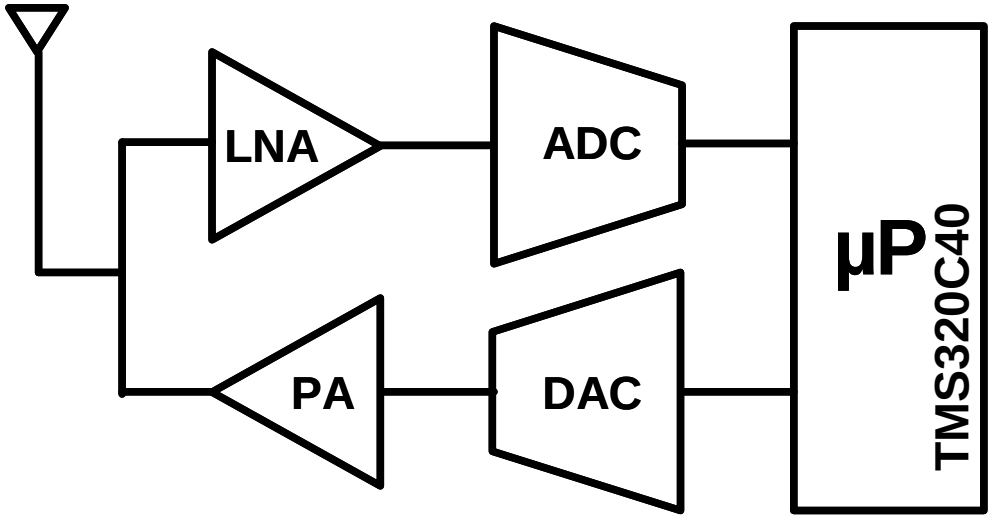
- **Why wide band RF design?**
- **How to make a wide band LNA?**
- **What about the wide band Rx architecture?**
- **What about the technology?**
- **Conclusions**

History: SpeakEasy project (1992)

- Large scale military software defined radio
  - motivated in large part by the communications interoperability problems that resulted from different branches of the military services having dissimilar (non-interoperable) radio systems
  - ten different radio waveforms in software on a single platform operating in frequency bands between 2 and 2000 MHz
  - Operated initially at the TMS320C40 processor

RJ Lackey and DW Upmal, "Speakeasy: The Military Software Radio," IEEE Communications Magazine, May 1995

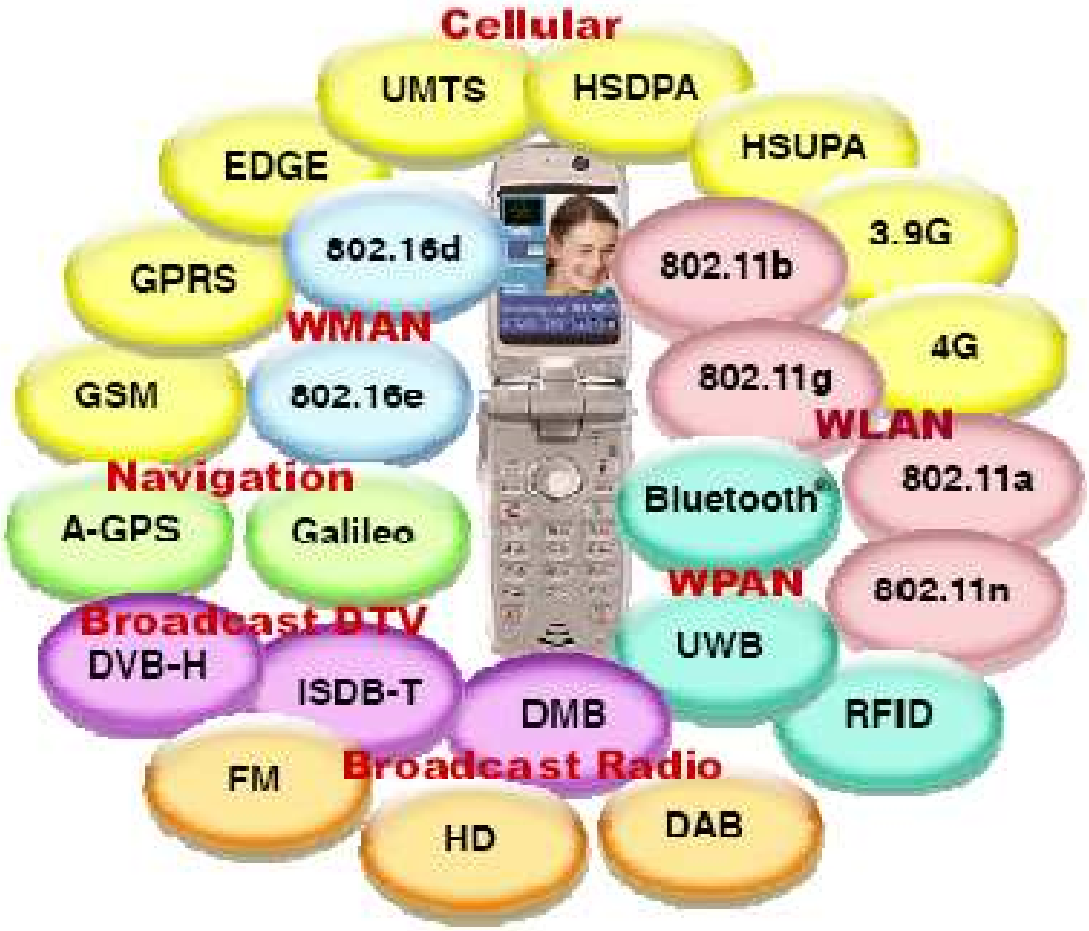
History: SpeakEasy project (1992)



Final result in 1994:

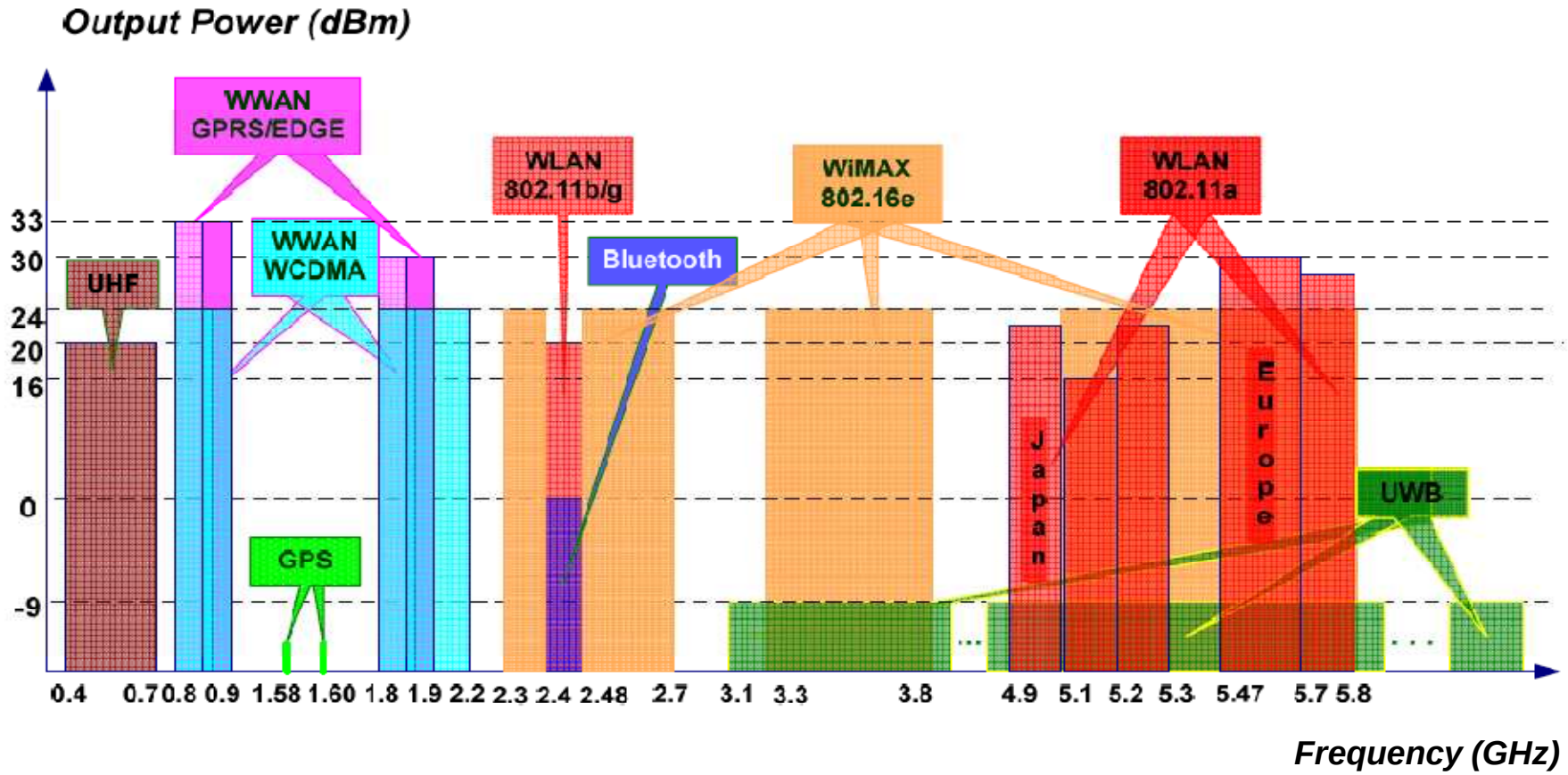
several hunderd processors and the ‘radio’ filled the back of a truck

Today: 10 different standards?

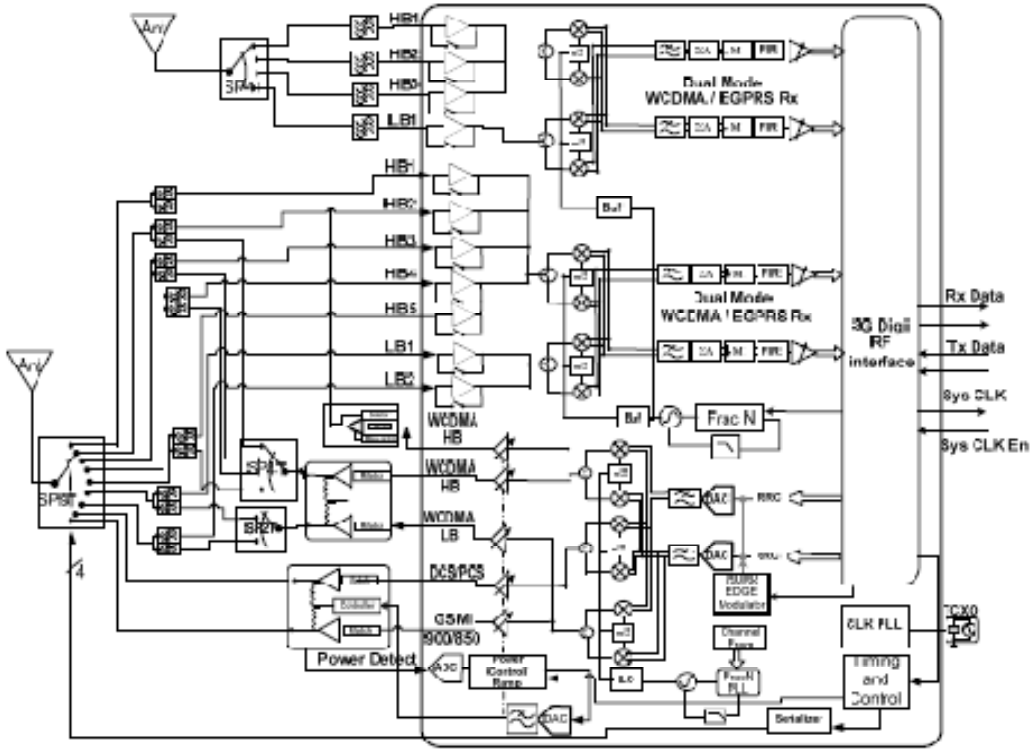


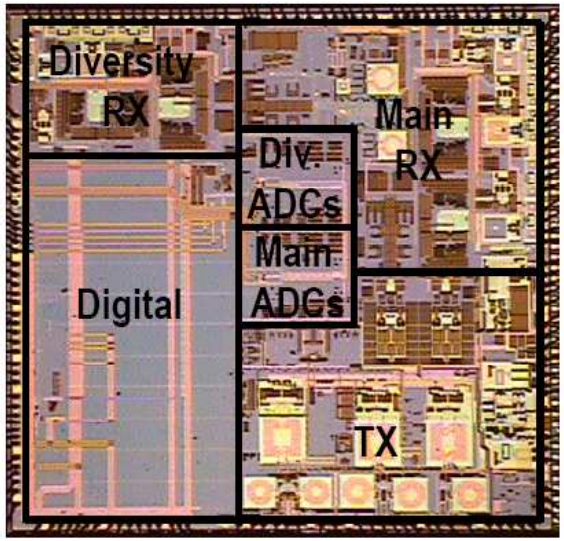
There is a convergence of standards ongoing, but still…

Today: 10 different standards?



Today in industry



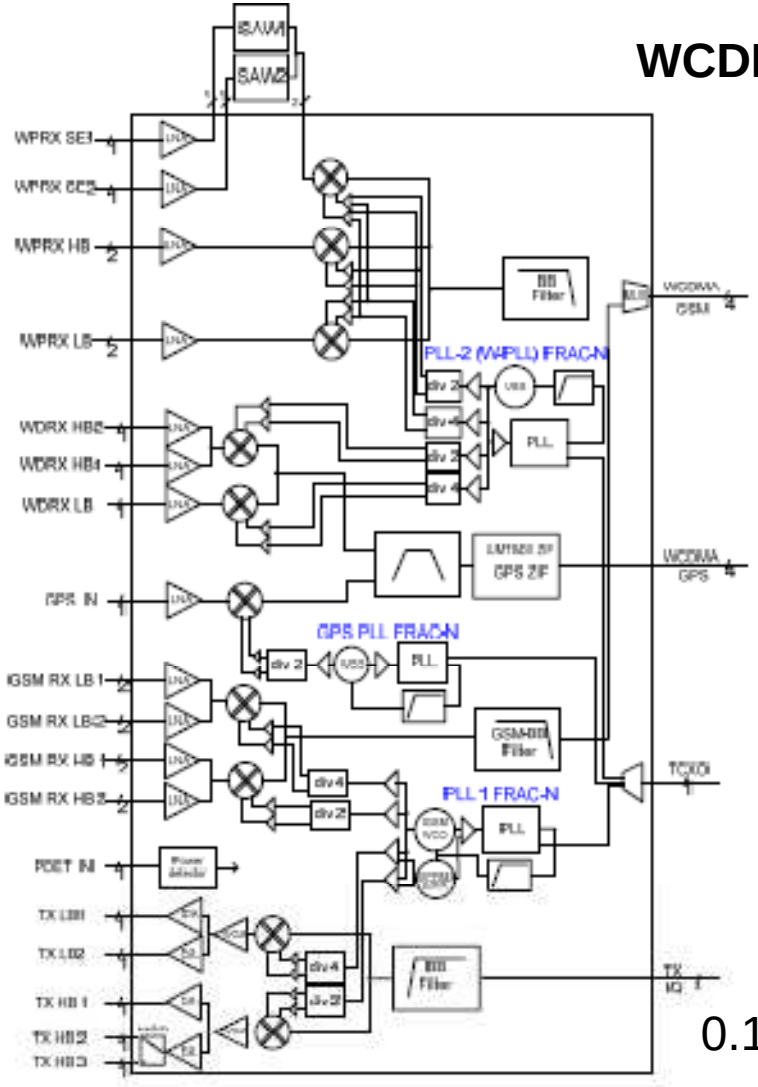


130nm cmos

WCDMA/HSDPA/HSUPA/EGPRS, Skyworks

ISSCC 2009

Today in industry



WCDMA/HSPA/EGPRS+ GPS and Rx diversity

WCDMA:4-LNA Primary Rx (2 SAW-less)

WCDMA:3-LNA diversity

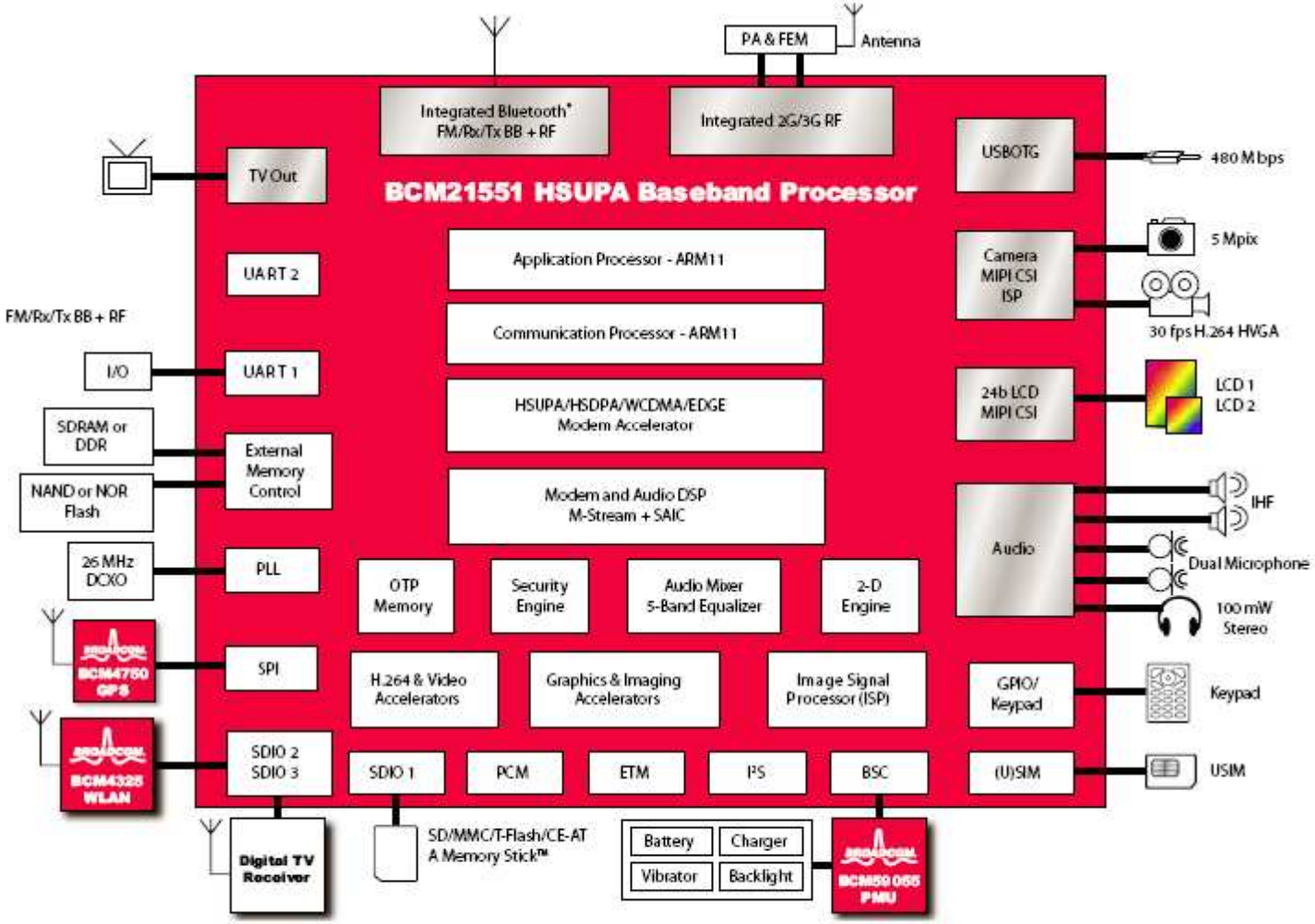
Quad-Band GSM/EDGE (800-900-1800-1900)

Qualcomm

0.18um CMOS

ISSCC 2009

Today in industry



Chip Block Diagram

Source: www.broadcom.com

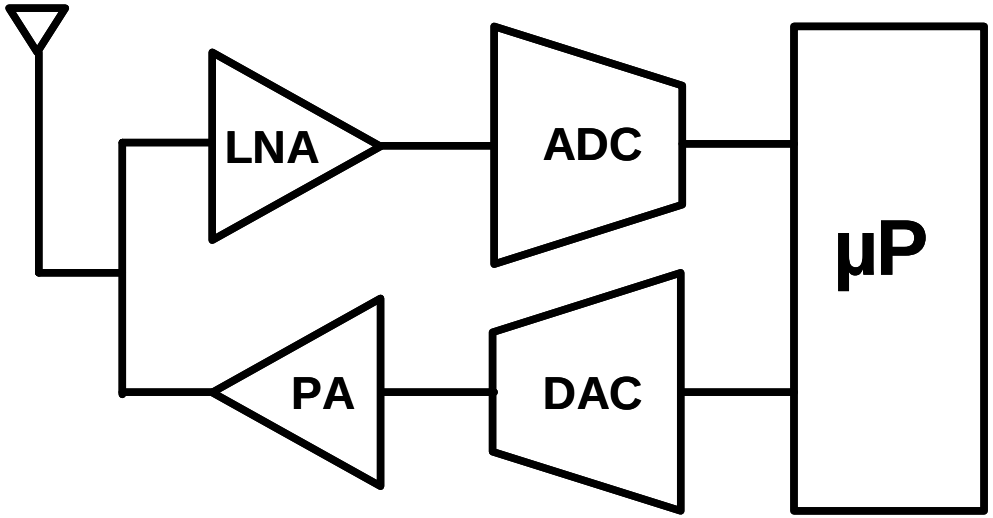
HSUPA+BT+FM in 65nm CMOS

Today in industry

- Industrial focus is on
  - Multi-band / multi-mode
  - Selectivity at RF
    - Front-end module by means of antenna filters
    - Selective LNA’s
    - LO generation per mode or band

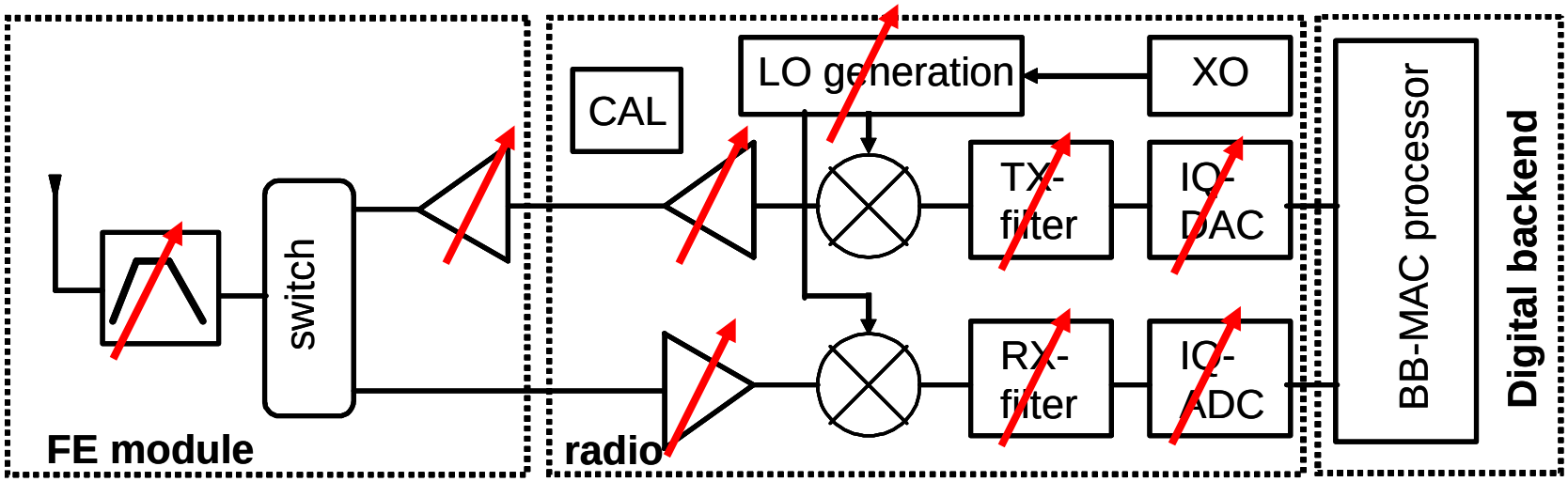
Software-defined radio (SDR)

- Based on signal processing
  - A/D requirements
  - Digital processing



Use Reconfigurable radio instead

- Analog selectivity
  - A/D requirements more relaxed
  - Wide-band RF front-end
  - Digitally assisted radio / FE module



Need of Wide-band RF front-ends

- First attempts were made by the development of UWB chipsets
  - 3 – 10 GHz
  - Started in 2003 with LNA design (see ISSCC 2004)
- Now focus on reconfigurable front-ends for 0 – 5 GHz operation
  - Started around 2005 (see ISSCC 2006)

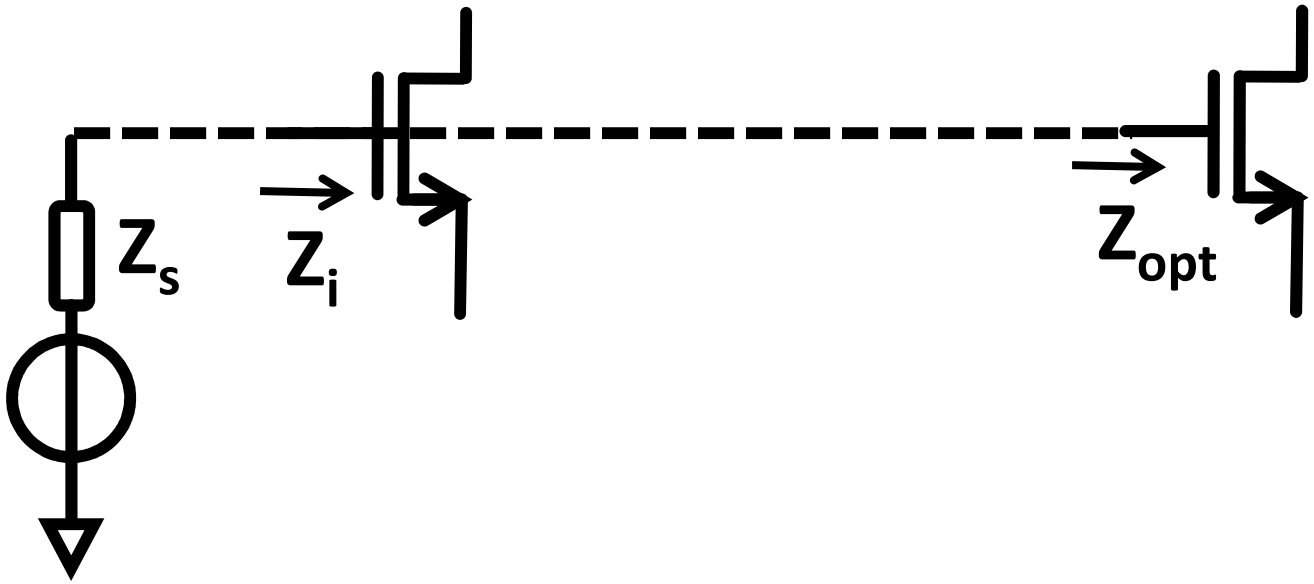
Wide band LNA: What's the problem?

Impedance match

$$Z_s = Z_i^* \Rightarrow P_{s,av} = P_{i,del}$$

Noise match

$$Z_s = Z_{opt}$$



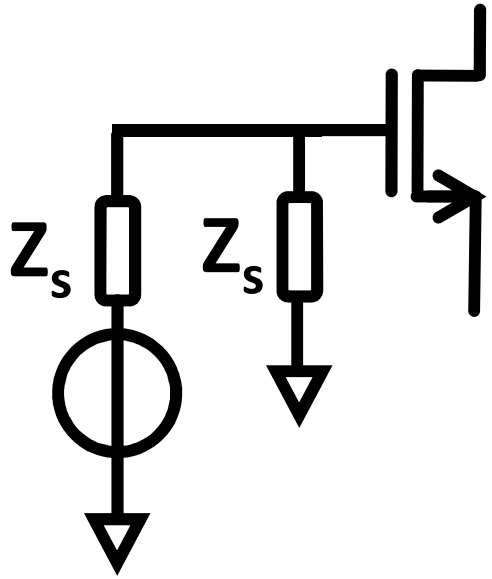
Z_i is mainly capacitive

Im(Z_{opt}) is inductive in nature

How to obtain power match and noise match over wide bandwidth?

What is the problem?

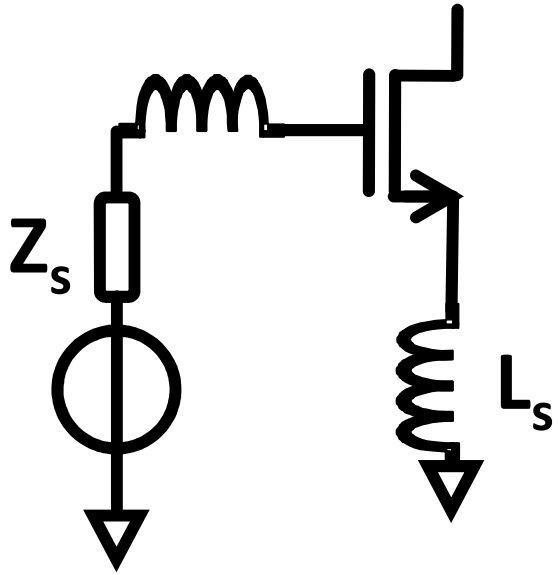
Wide band impedance match



$$F \geq 2 + \frac{4\gamma}{\alpha}\frac{1}{g_m R_s}$$

NF >> 3dB

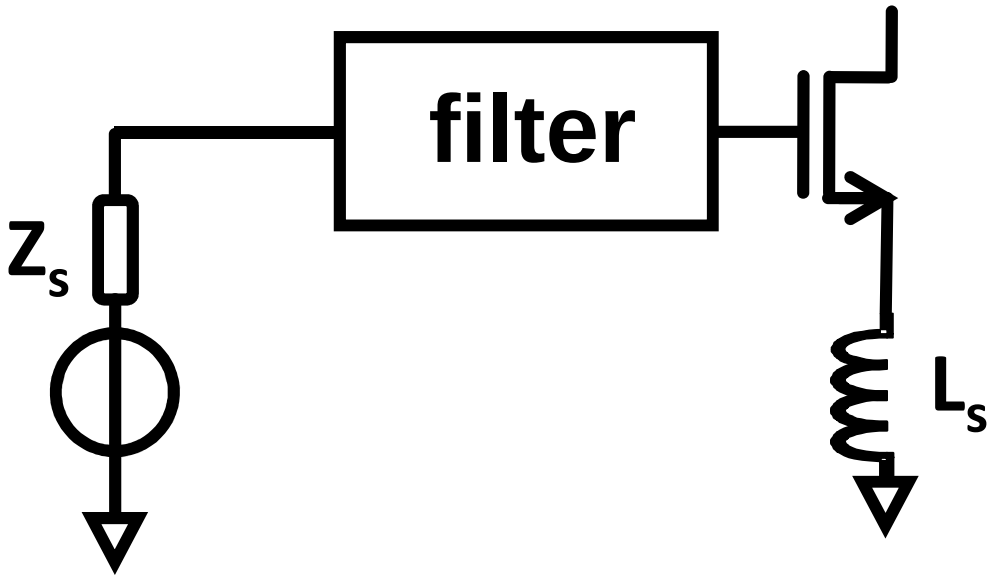
Narrow band impedance match



$$F \geq 1 + \frac{2}{3}\frac{\omega L_s}{Q R_s}$$

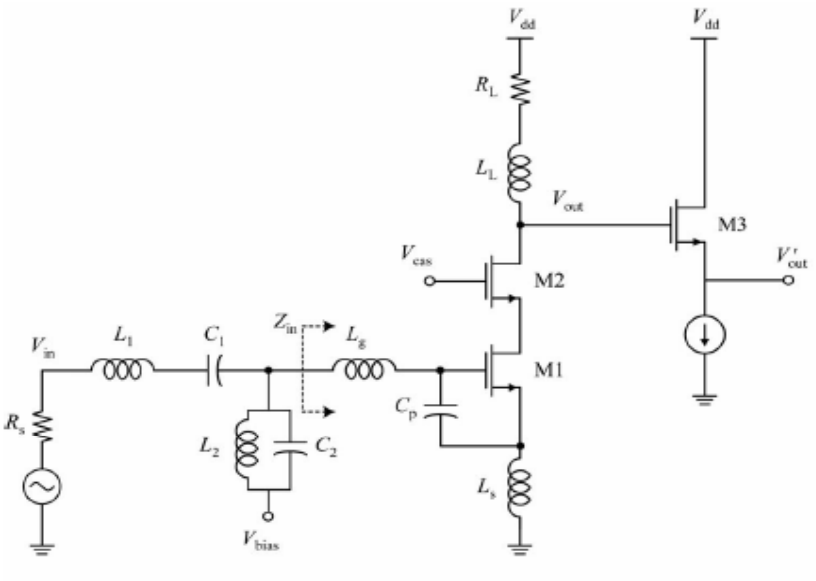
$$Z_{in} \approx \frac{g_m L_s}{C_{gs}} + sL_s + \frac{1}{sC_{gs}}$$

Possible solution



Wide band impedance match using filter as impedance converter

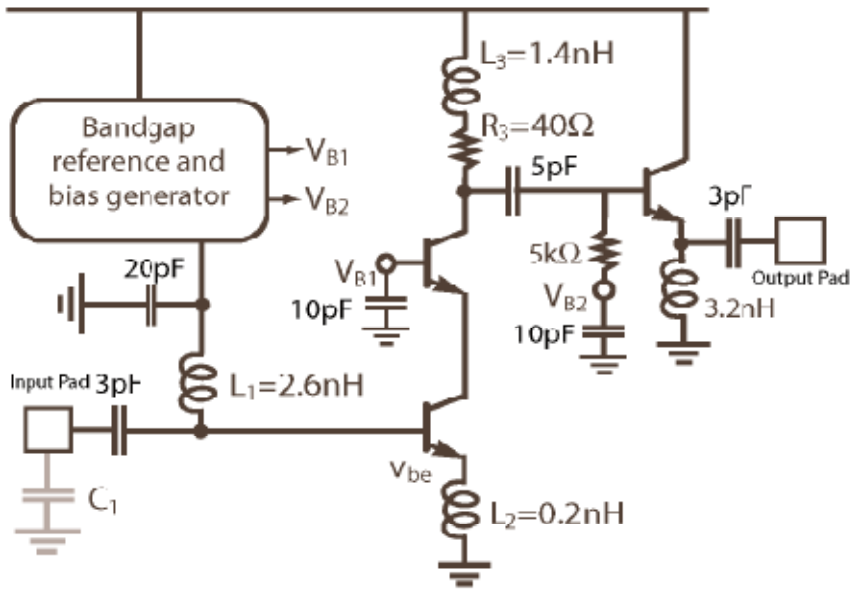
The first attempts



ISSCC2004: Bevilacqua

Band-pass LC matching network

NF: 5.5dB (3-8GHz)



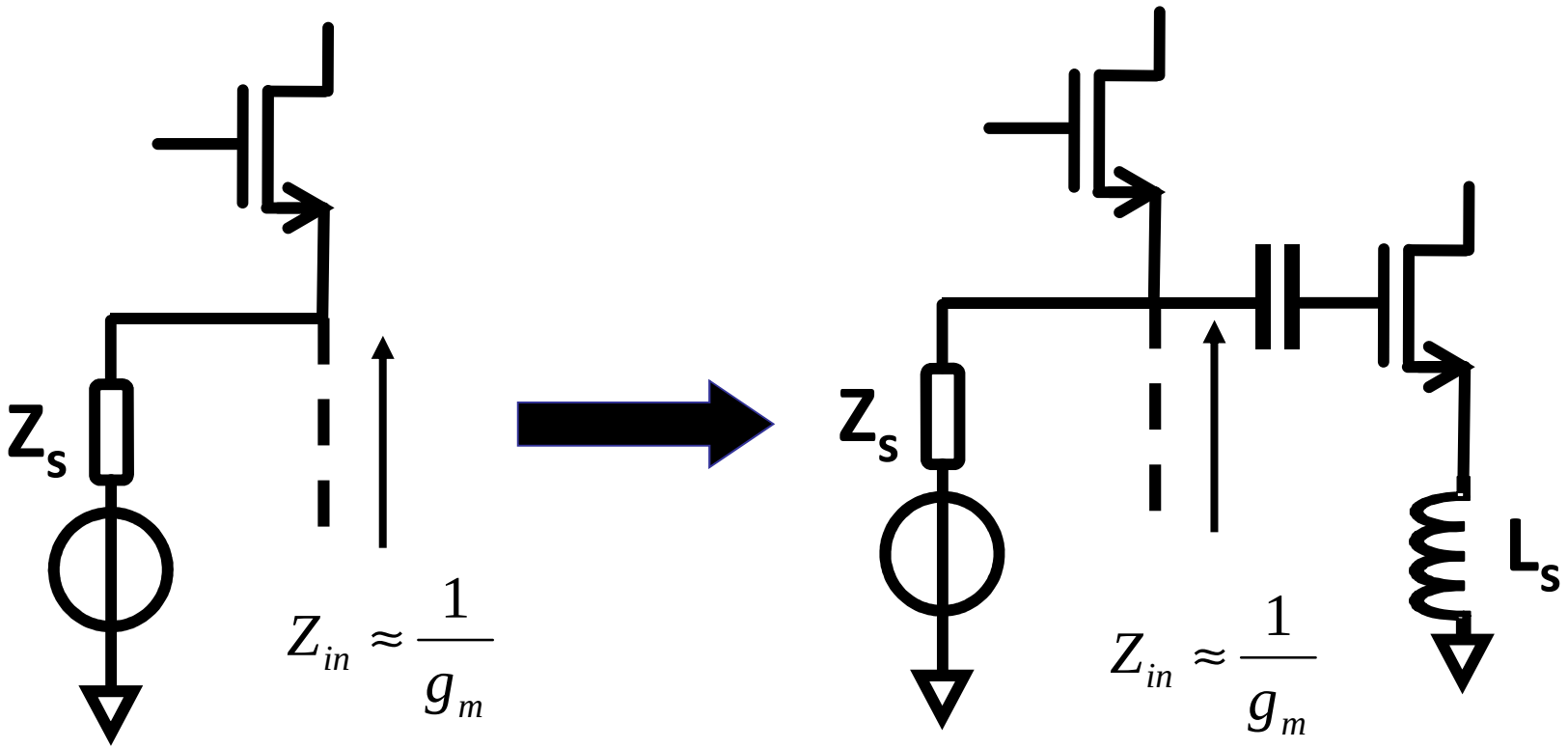
ISSCC2004: Ismail

Band-pass LC matching network

NF: 4.5dB (2-10GHz)

Both are bulky due to # integrated inductors and single-ended input/output

Other possible solution

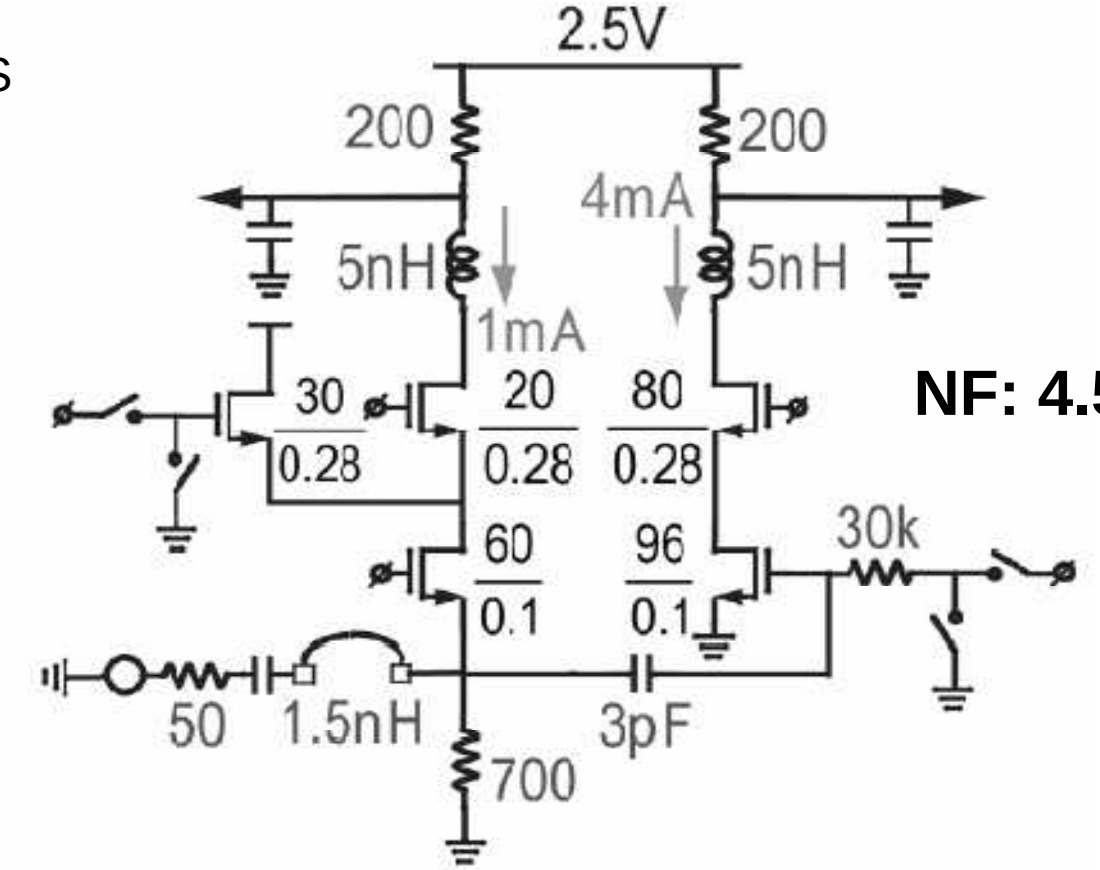


$$F \geq 1 + \frac{2}{3}\frac{\omega L_s}{QR_s} + O(CG)$$

Note: inherent single-to-differential conversion

‘Second’ Generation

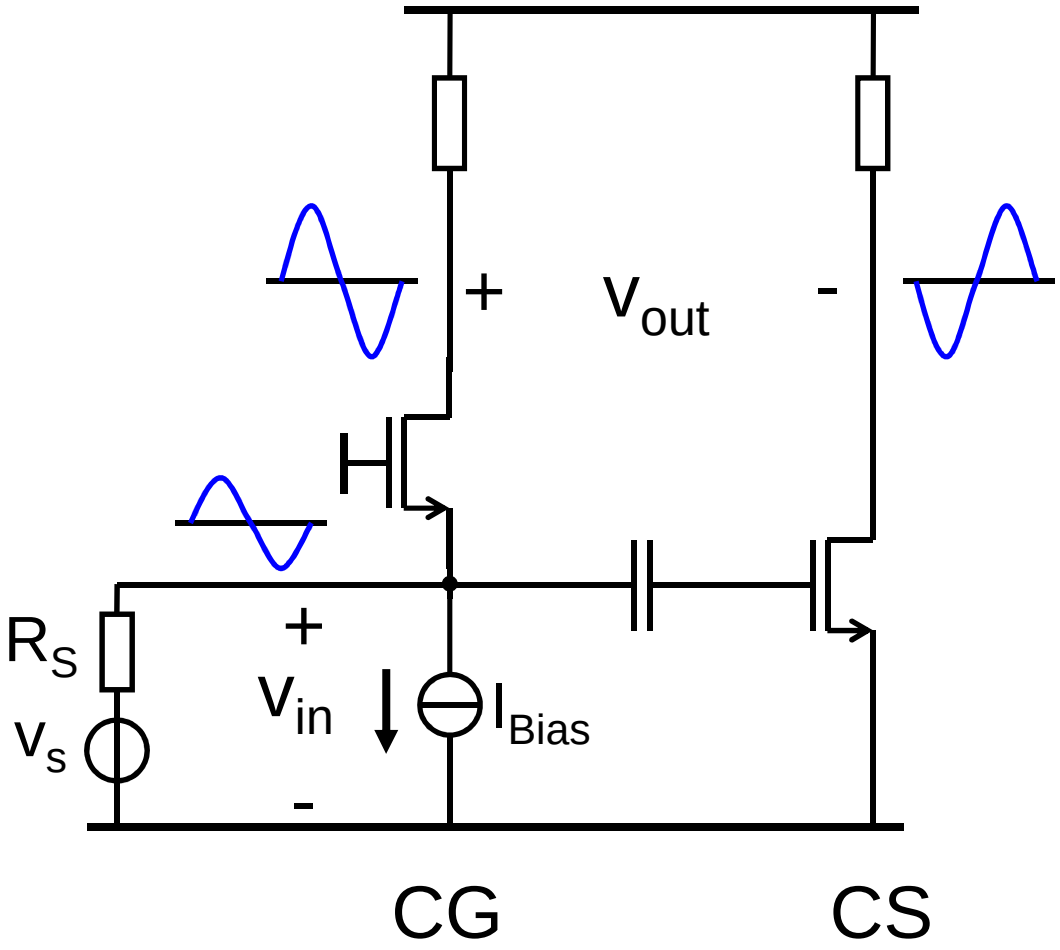
90nm CMOS



NF: 4.5dB (0.8-5GHz)

decouple the noise and input impedance match
but still bulky

Next generation: starting point

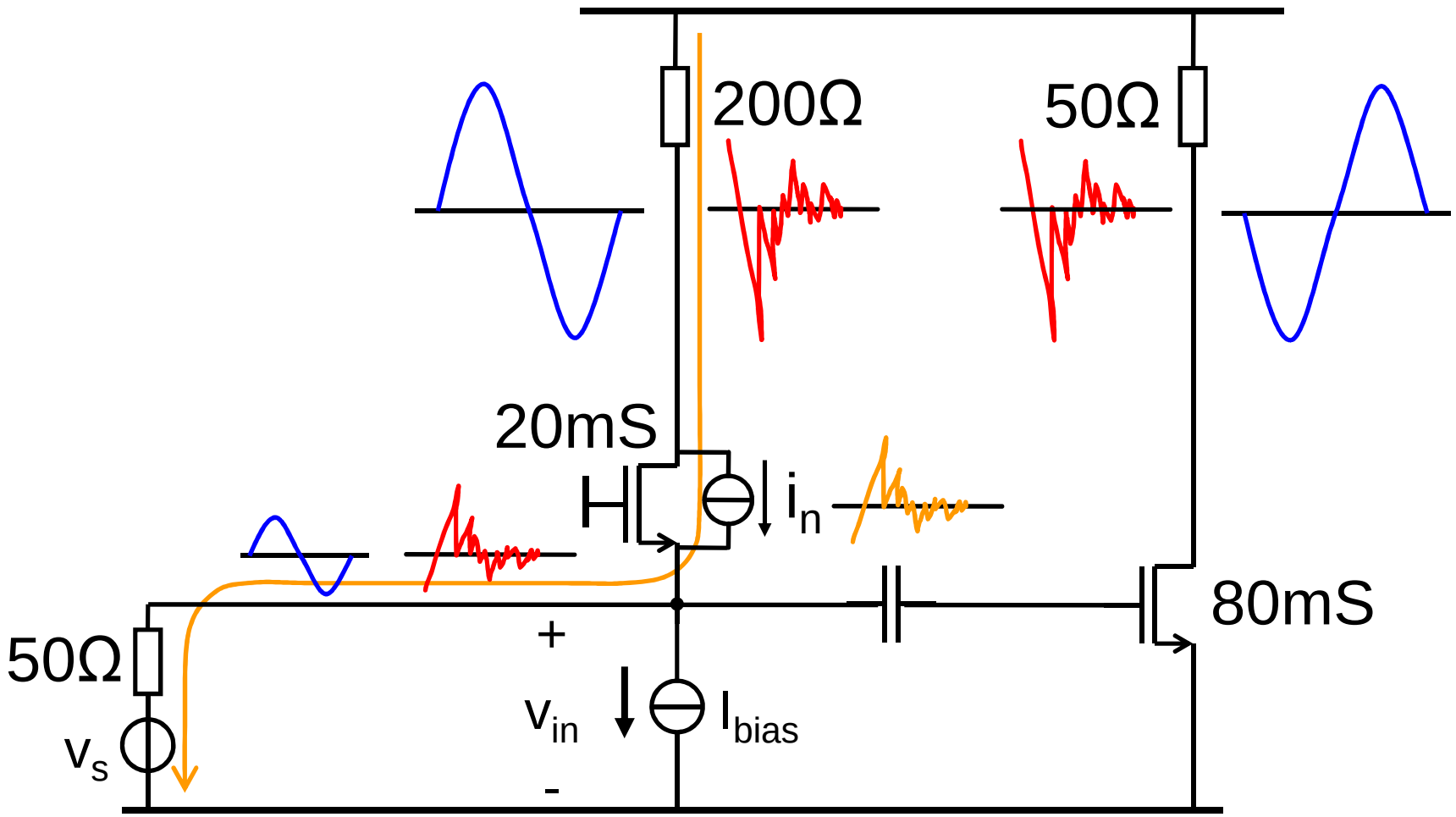


Simultaneous:

- Single-to-Differential
- Balanced Gain
- Broadband input match (~$1/g_{mCG}$)
- Noise Canceling
- Distortion Canceling

[Blaakmeer et al. ESSCIRC `07]

LNA: noise canceling



Noise canceled, signal amplified at differential output

LNA: limited bandwidth

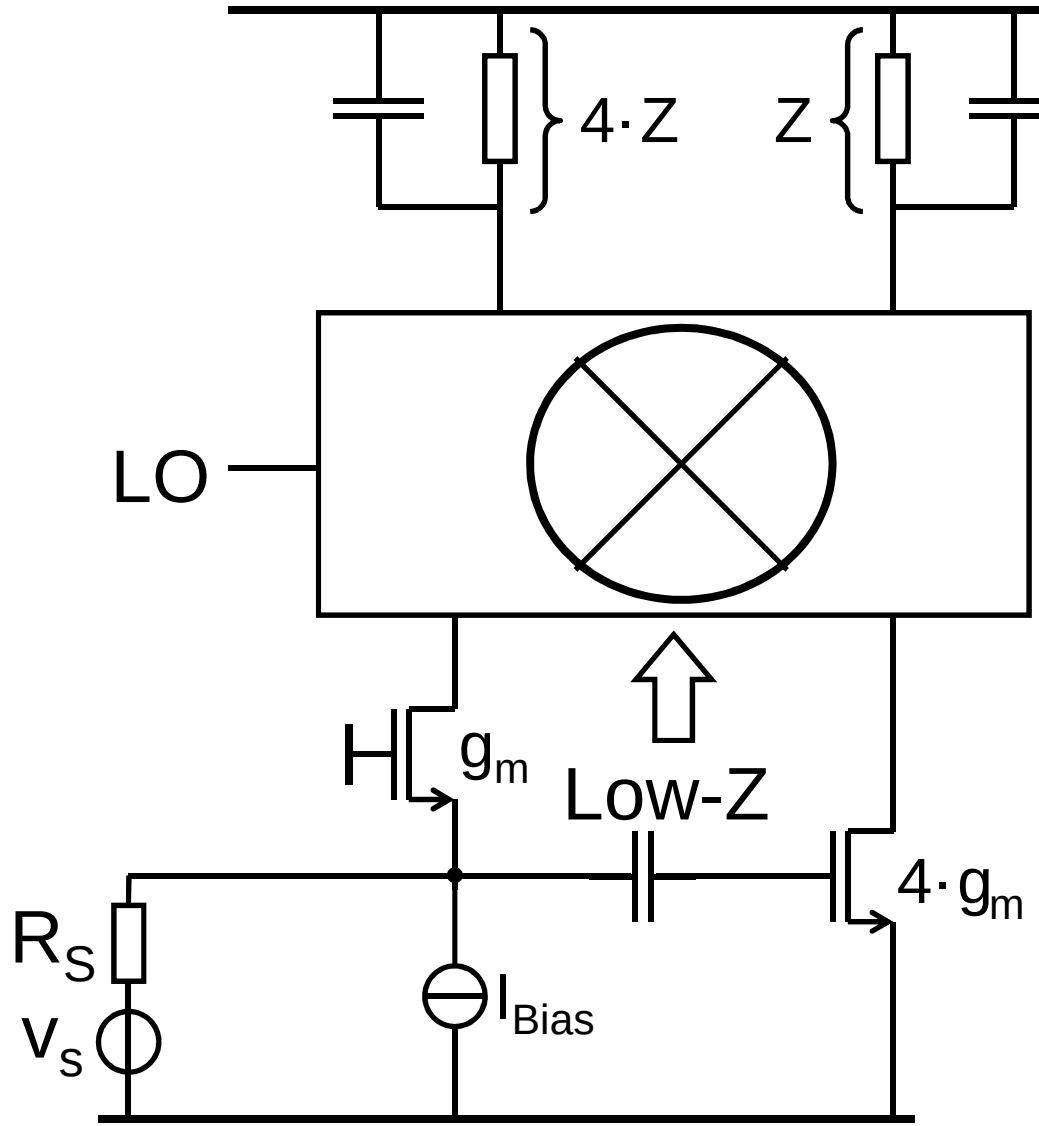
- Limited bandwidth at output CG-stage:

$$\left.\begin{aligned} R_{CG} &= A_{V,CG} \cdot R_S \\ &= 200\,\Omega \qquad @\ \ A_{V,CG} = 4 \\ f_{-3dB} &= \frac{1}{2 \cdot \pi \cdot R_{CG} \cdot C_{Load}} = 10\,\text{GHz} \end{aligned}\right\} \rightarrow \boldsymbol{C_{Load} < 80\ \text{fF}}$$

- Inductive peaking required
  - Contrasts aim: no on-chip inductors

<u>Solution: don't make voltage gain @ RF!</u>

Solution: insert mixer

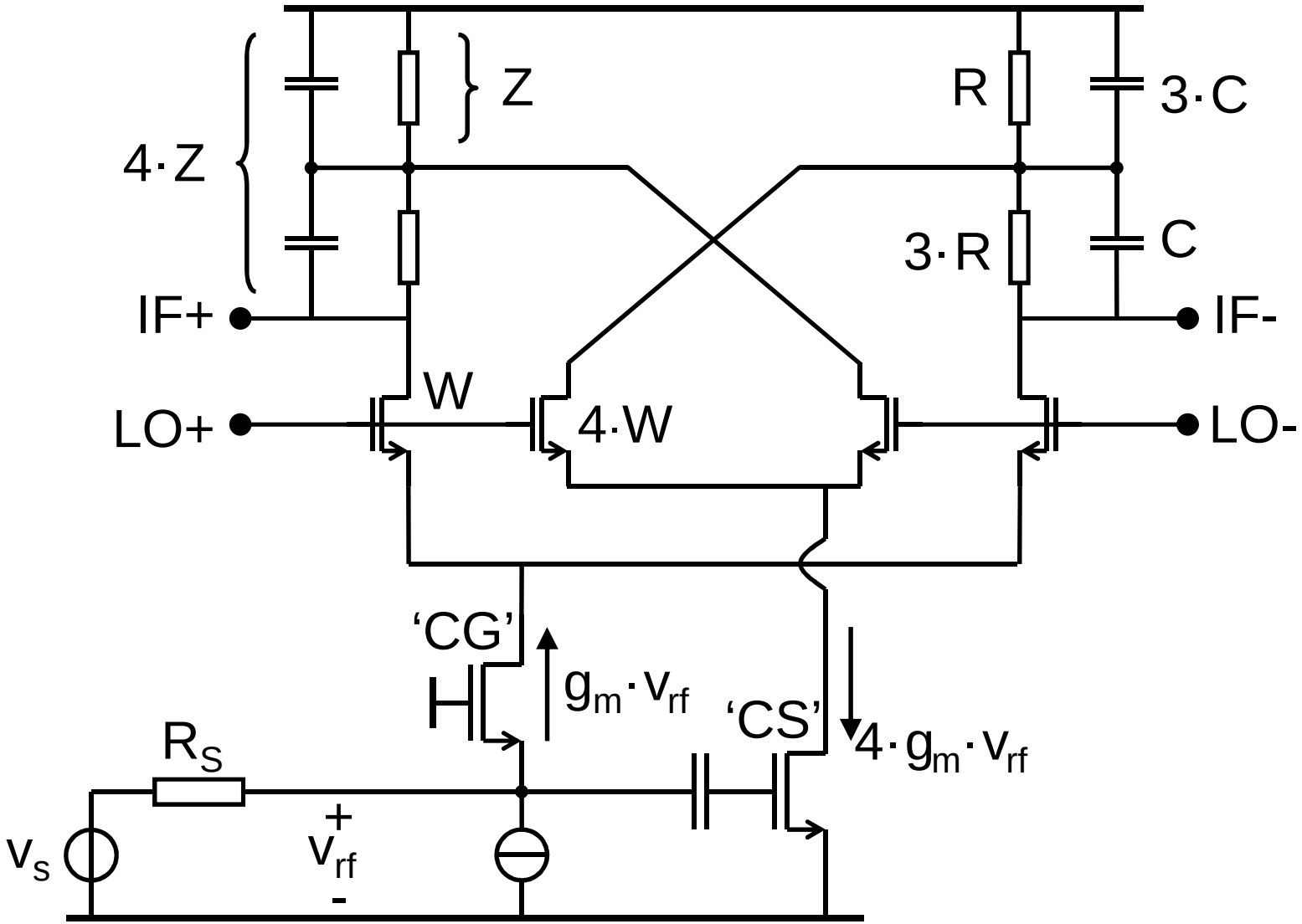


IF: Capacitance
no problem

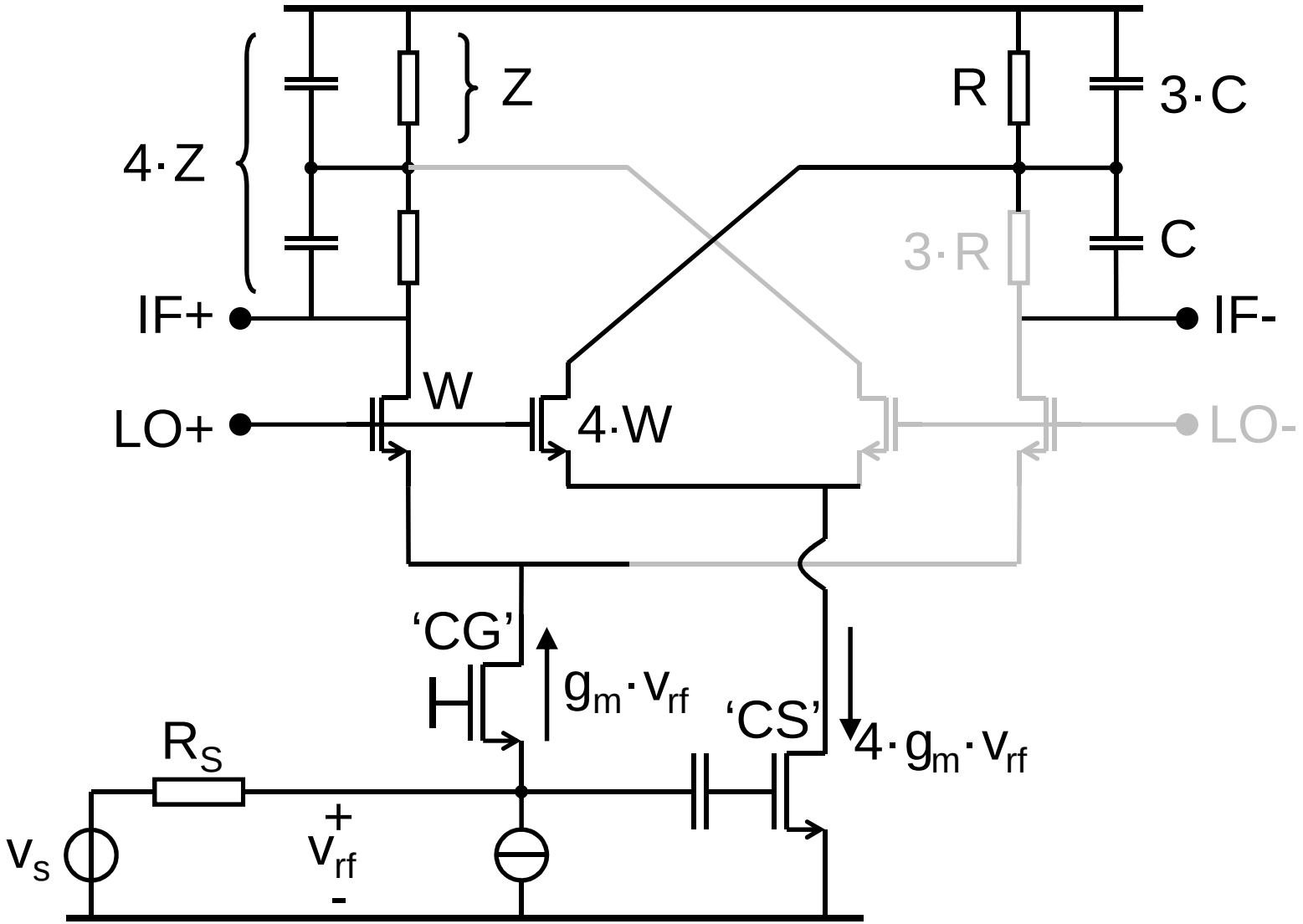
Mixer: Low-Z input

RF: no high-Z nodes

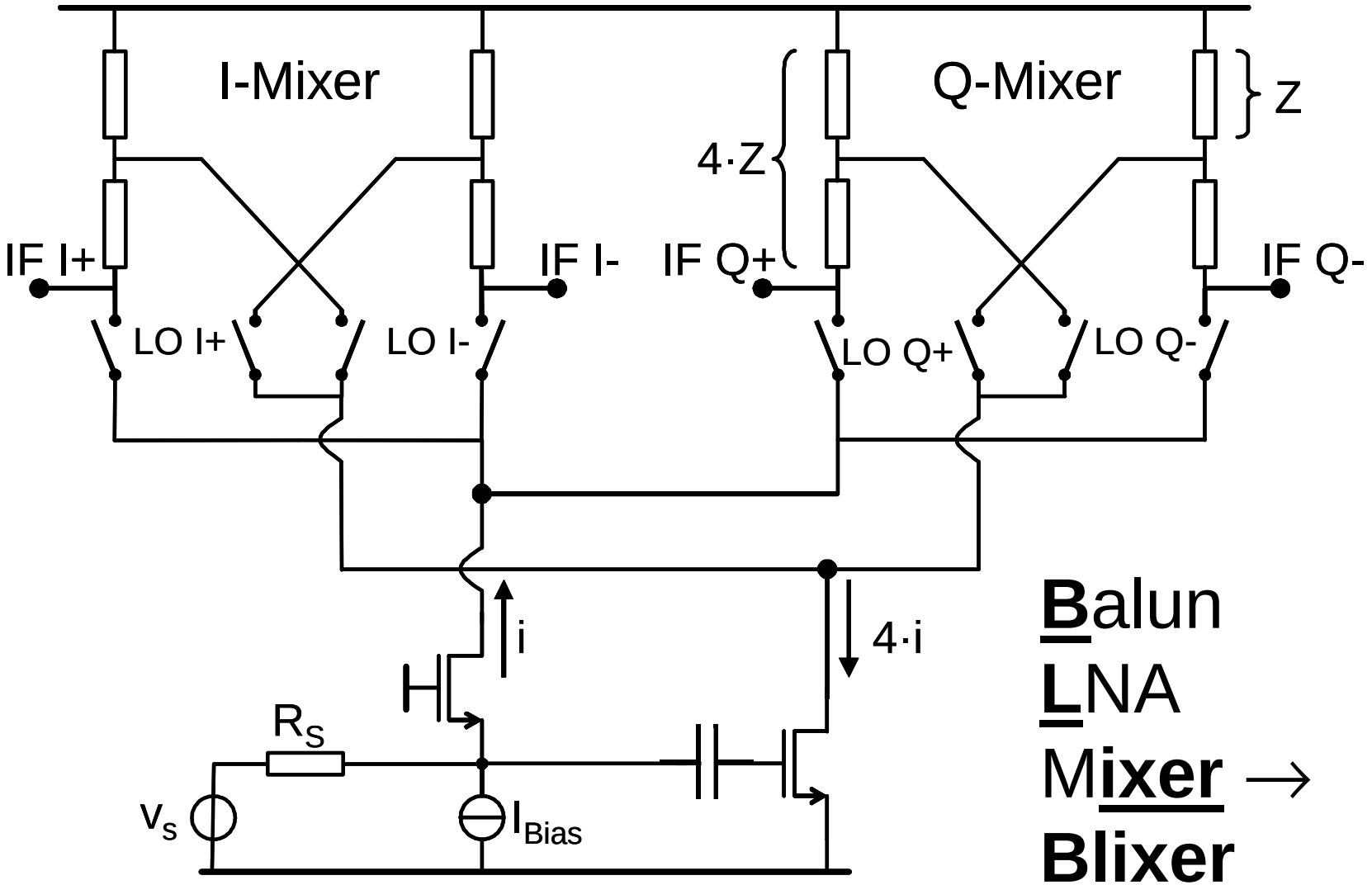
Solution: insert mixer



Solution: noise cancellation @ IF

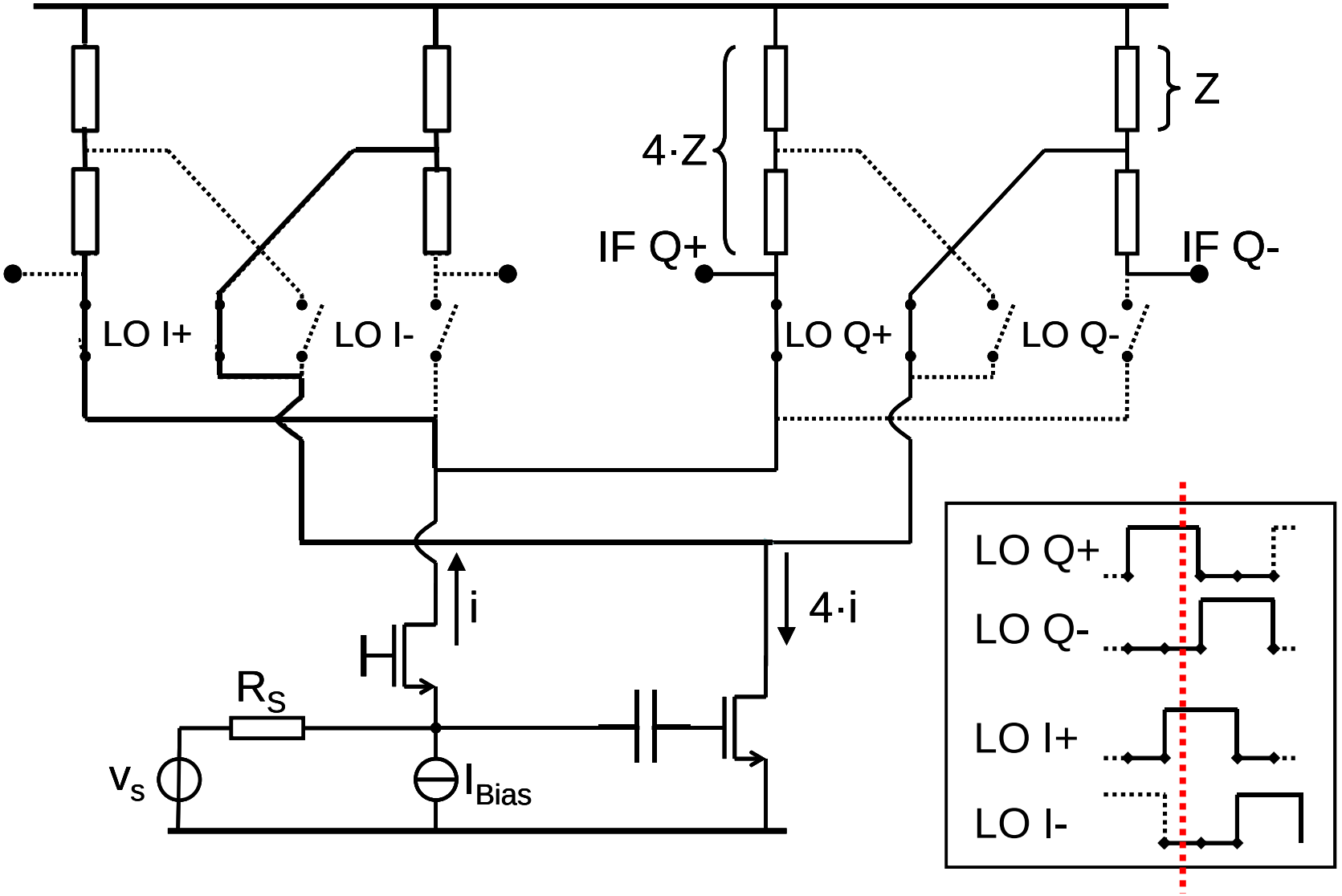


BLixer: IQ balanced

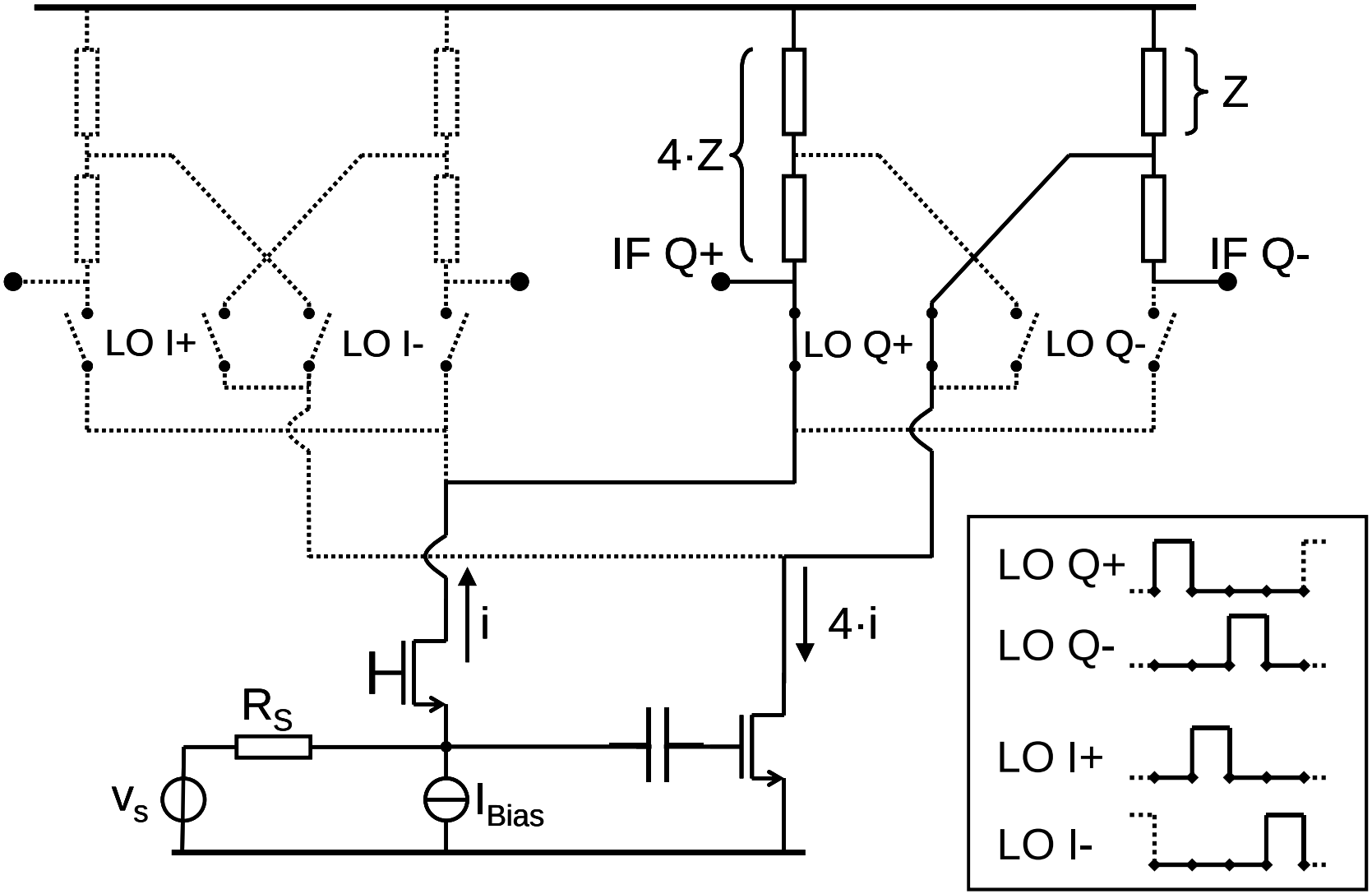


Balun
LNA
M**ixer** →
Blixer

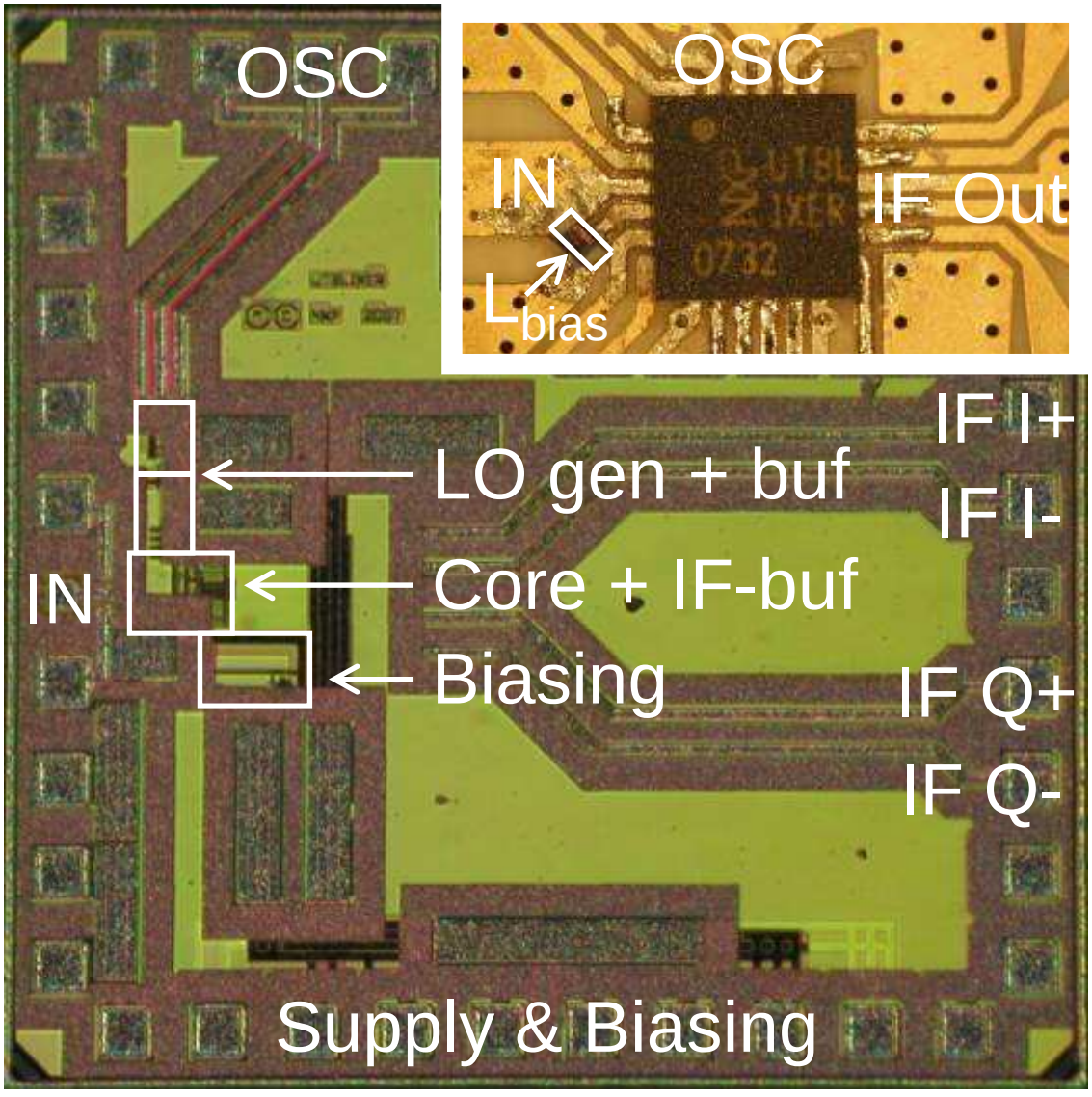
BLixer: 50% duty cycle



BLixer: 25% duty cycle



BLixer: silicon

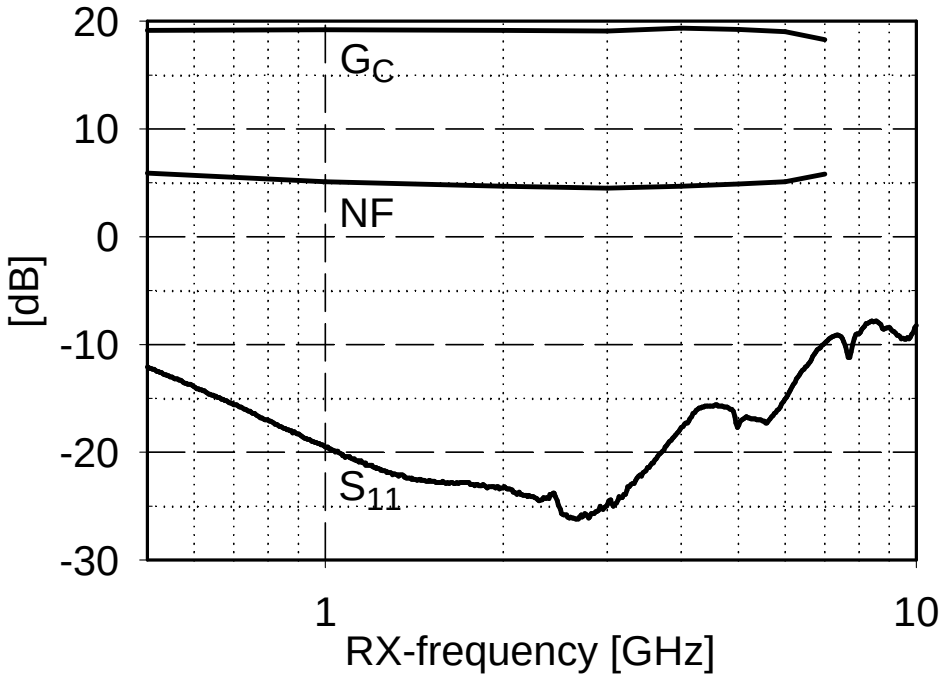


Baseline
65nm CMOS
1.2V supply

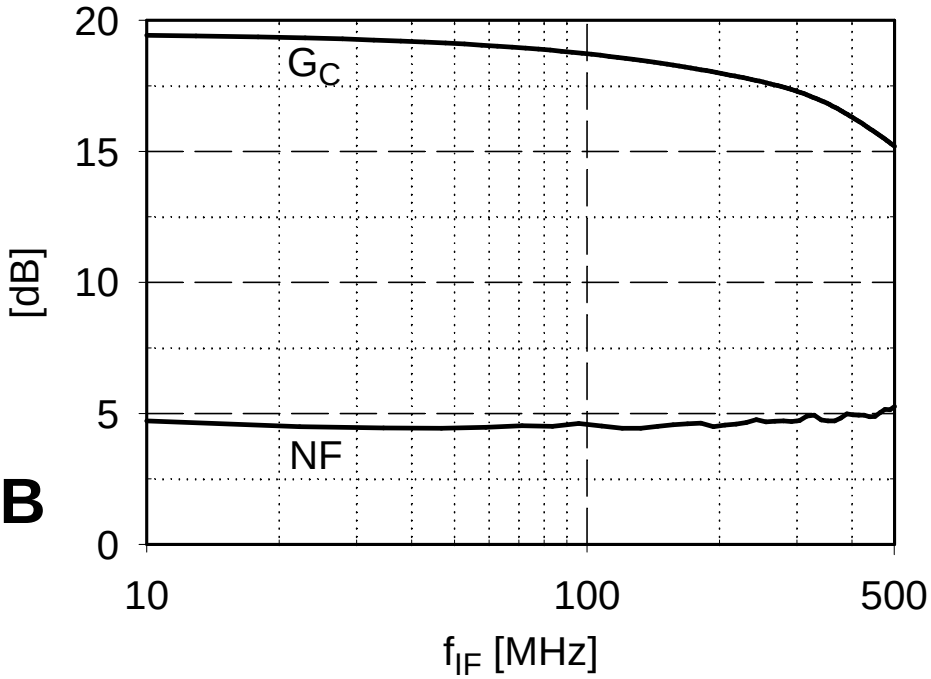
Active area
< 0.02 mm^2

[Blaakmeer et al. ISSCC '08]

BLixer: measured results



Wide band behavior at RF

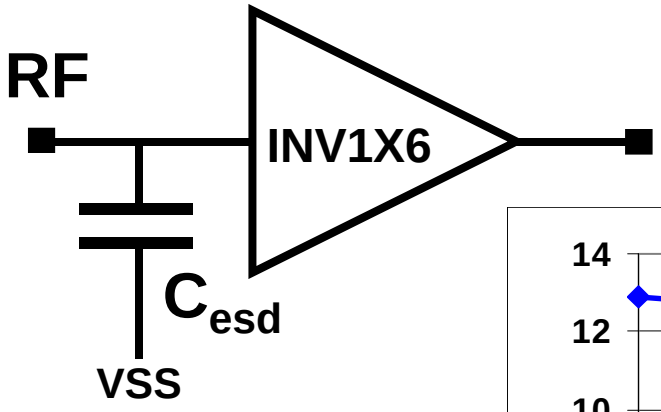


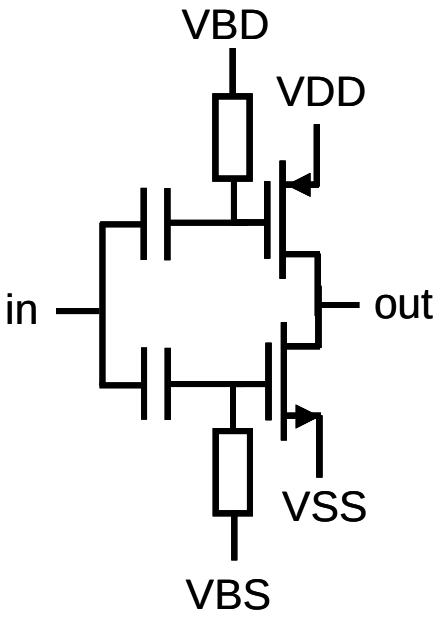
… and at IF/BB

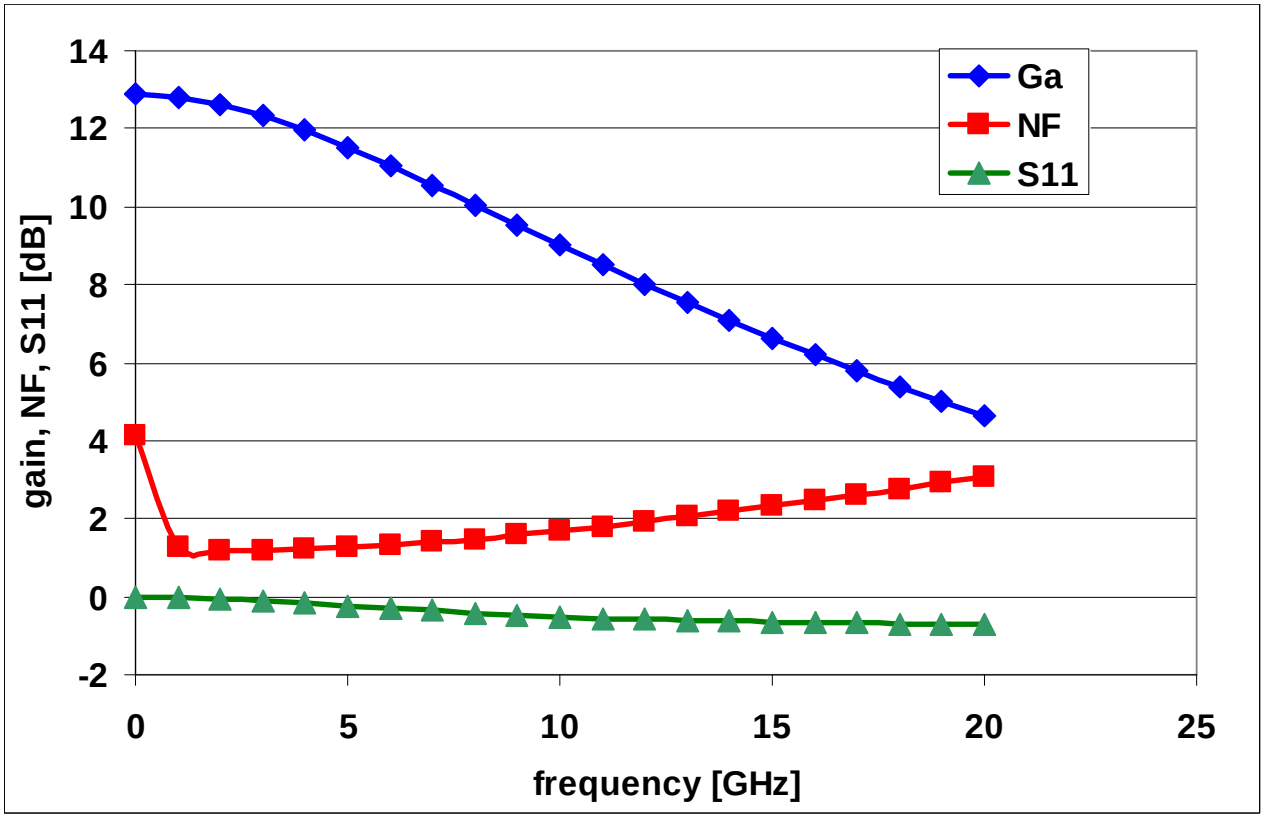
BLixer: measured results

- Linearity:
  - IIP3 @ RF: -3 dBm (5.2 & 5.7GHz, f_{LO} = 4.6 GHz)
  - IIP2 @ RF: +20 dBm (2.4 & 5.7GHz, f_{LO} = 3.2 GHz)
  - IIP2 (Mix-leak.) >+40 dBm (5.7 & 5.8GHz, f_{LO}:0.5 - 7 GHz)
- Quadrature accuracy:
  - Phase error < 3°
  - Gain error < 1dB
- LO leakage < -50 dBm

What about inverters?



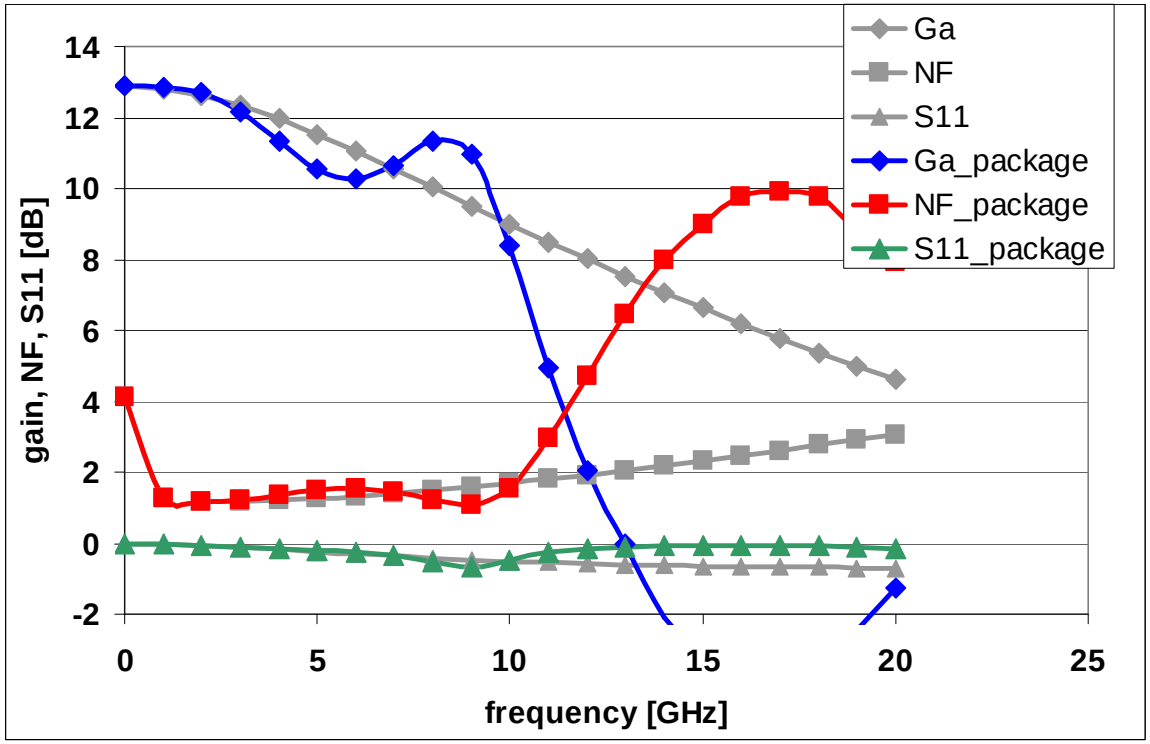


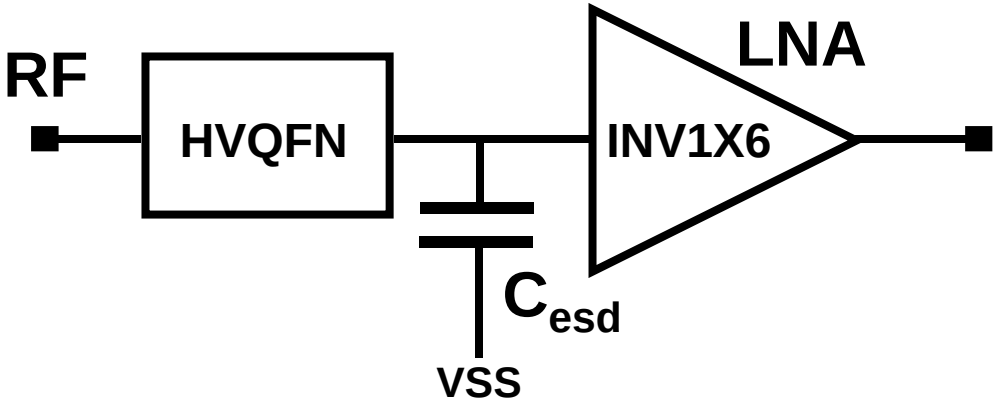


What about inverters?

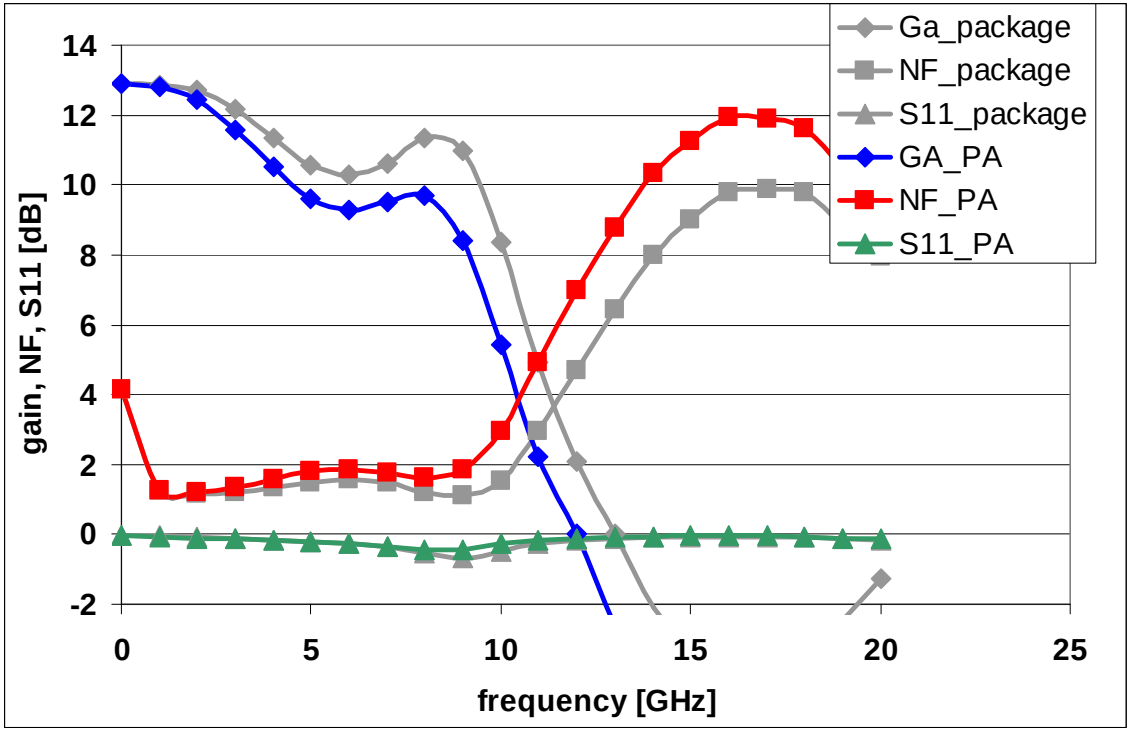
Add package:

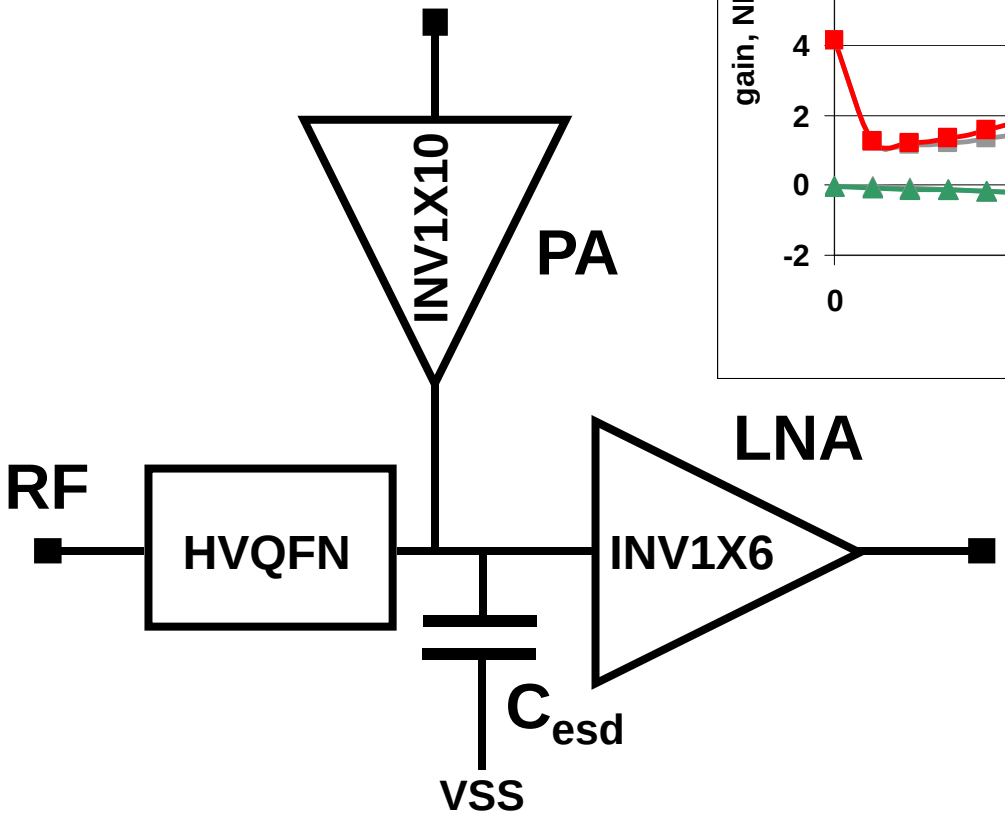
HVQFN



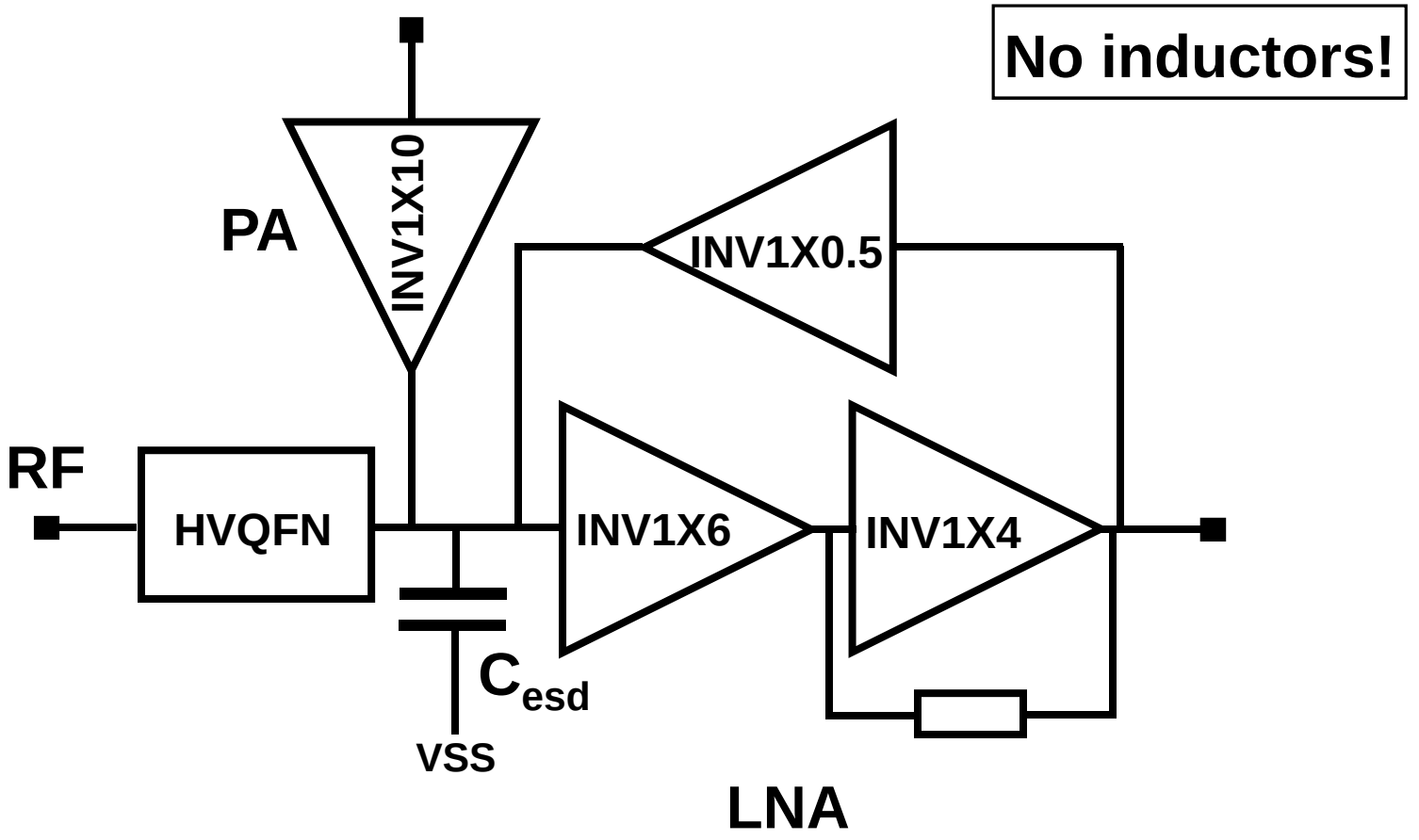


What about inverters?



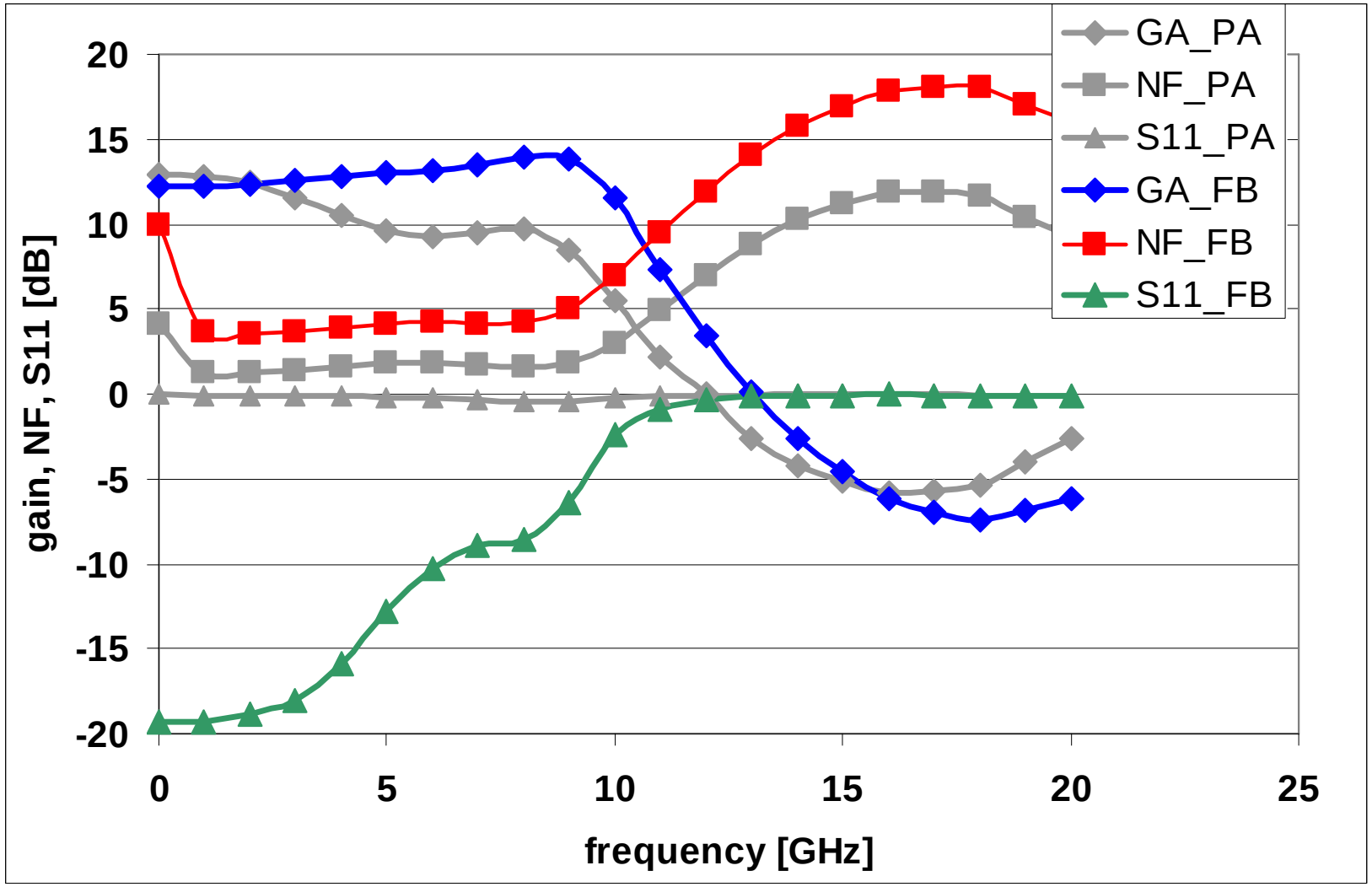


‘Inverter-only’ LNA

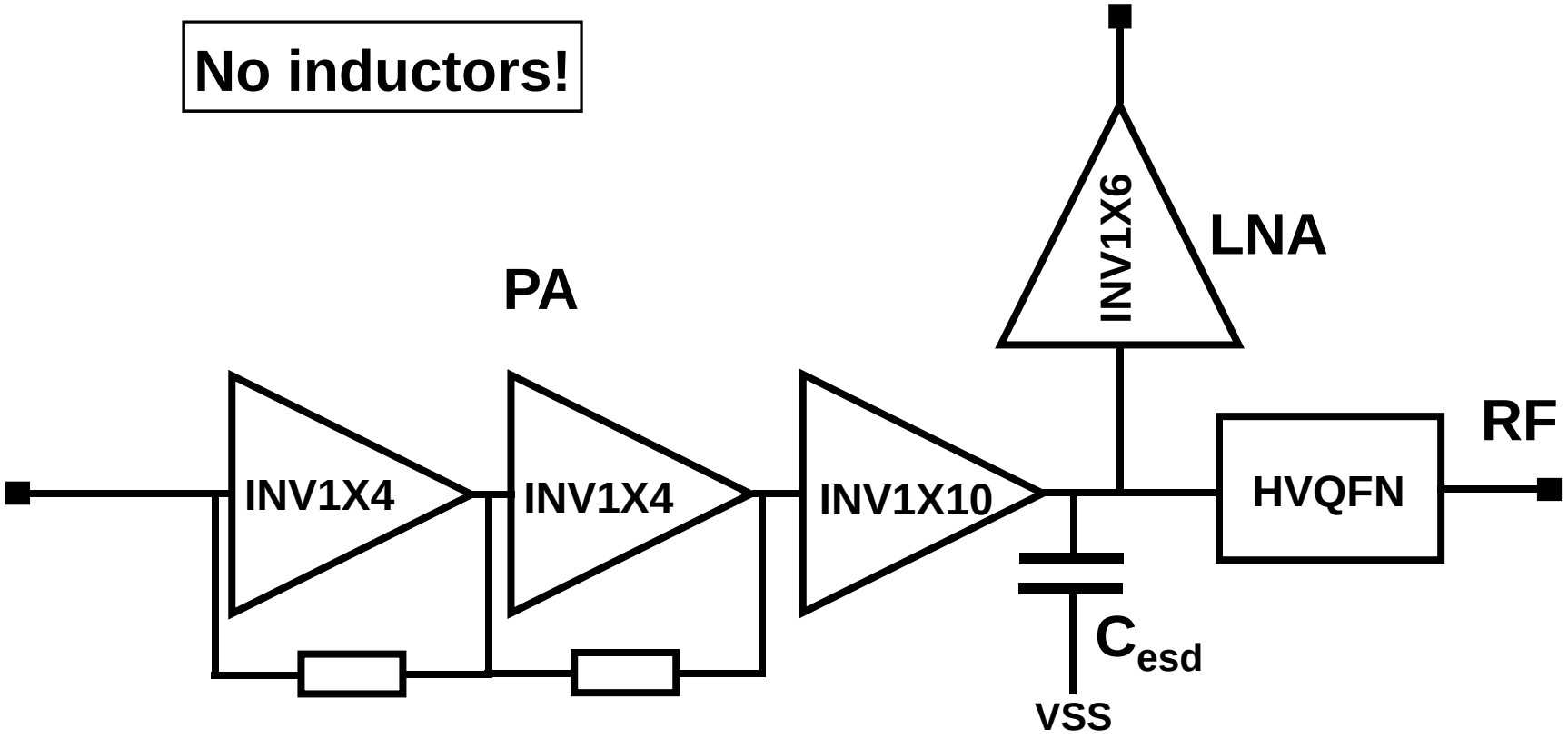


Add additional stage and feedback in LNA

‘Inverter-only’ LNA

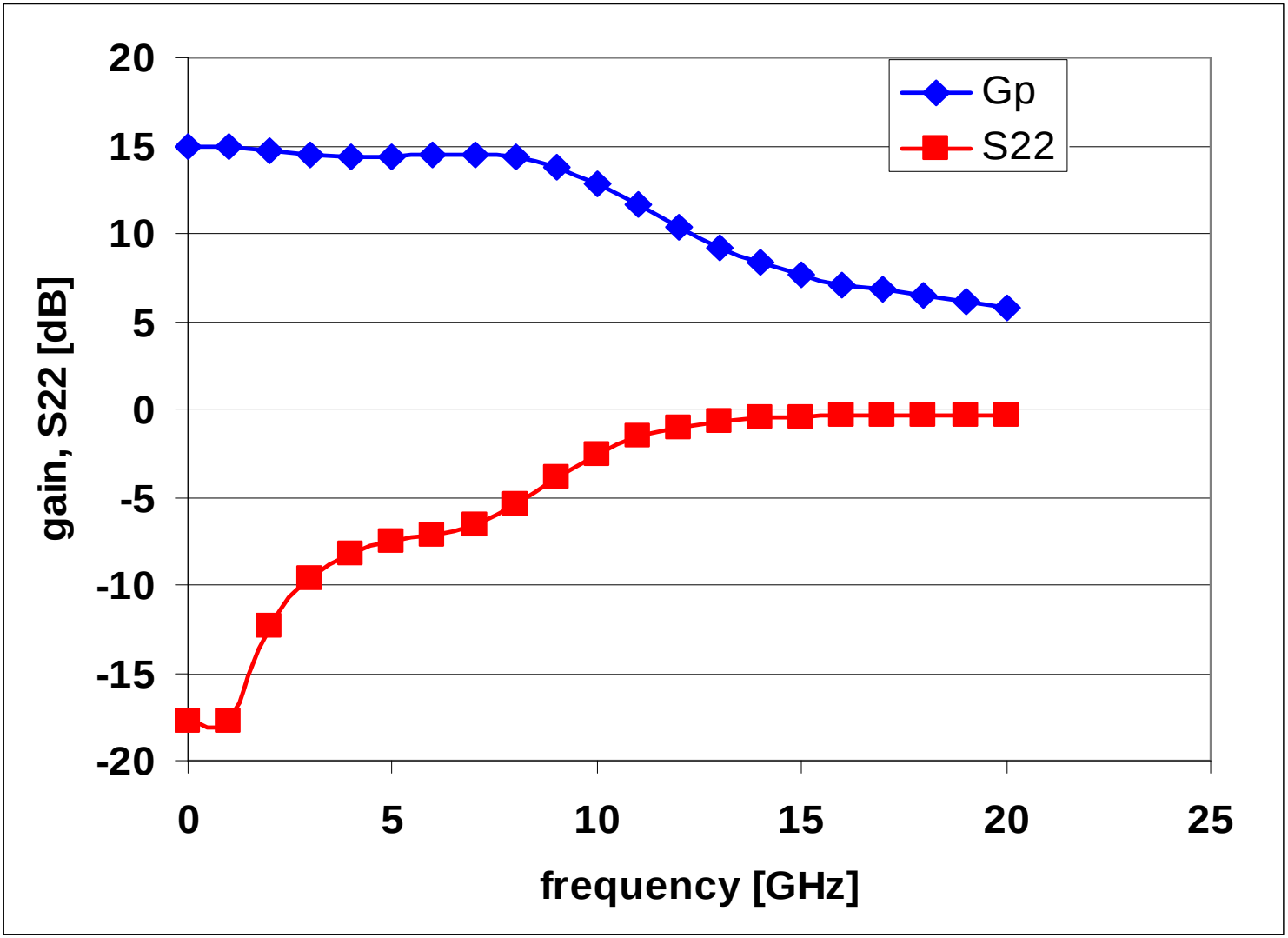


‘Inverter-only’ PA

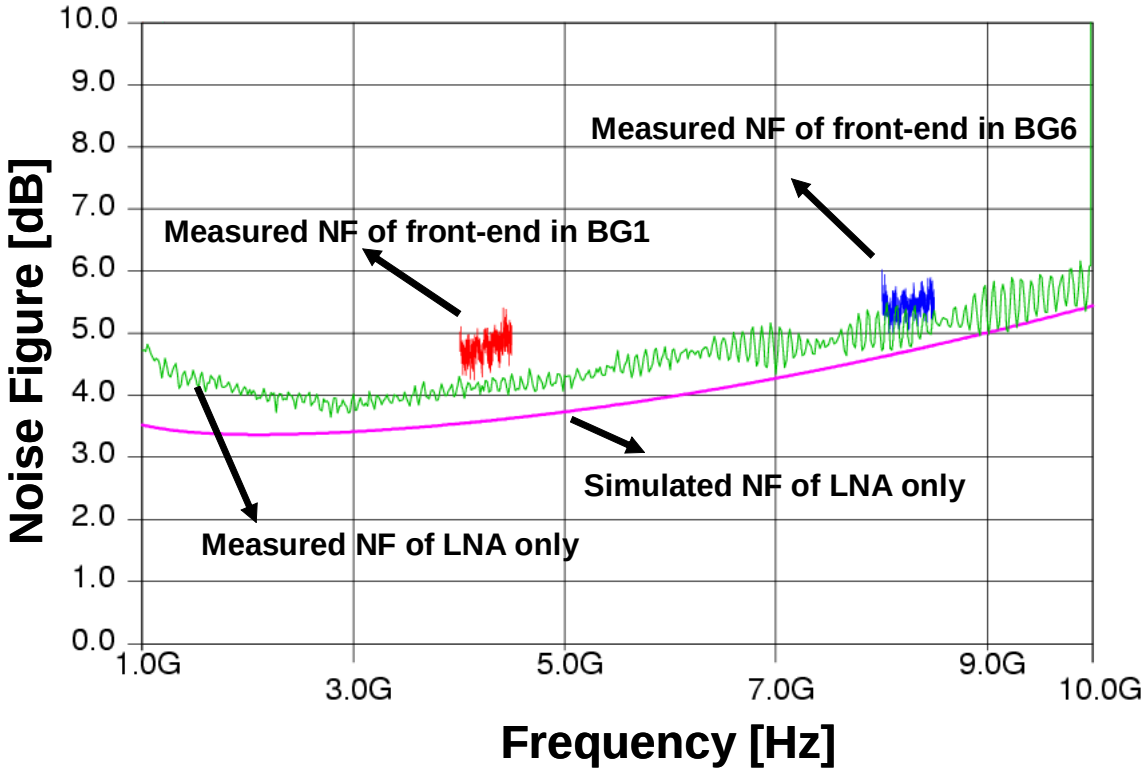


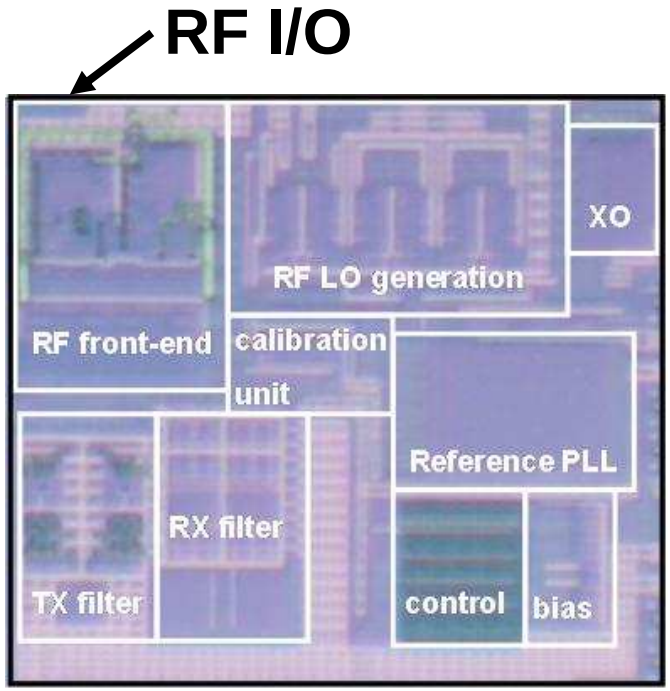
Add additional stages and feedback in PA

‘Inverter-only’ PA



RF front-end only with inverters!





radio

65nm (LP) CMOS

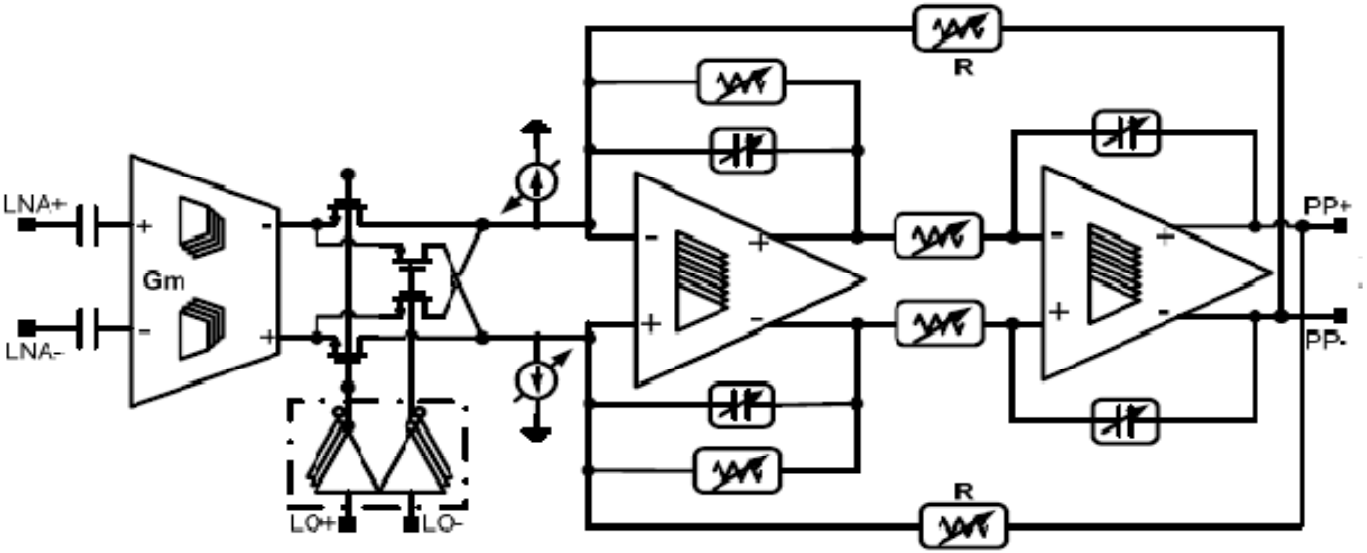
[Leenaerts et al. ISSCC '09]

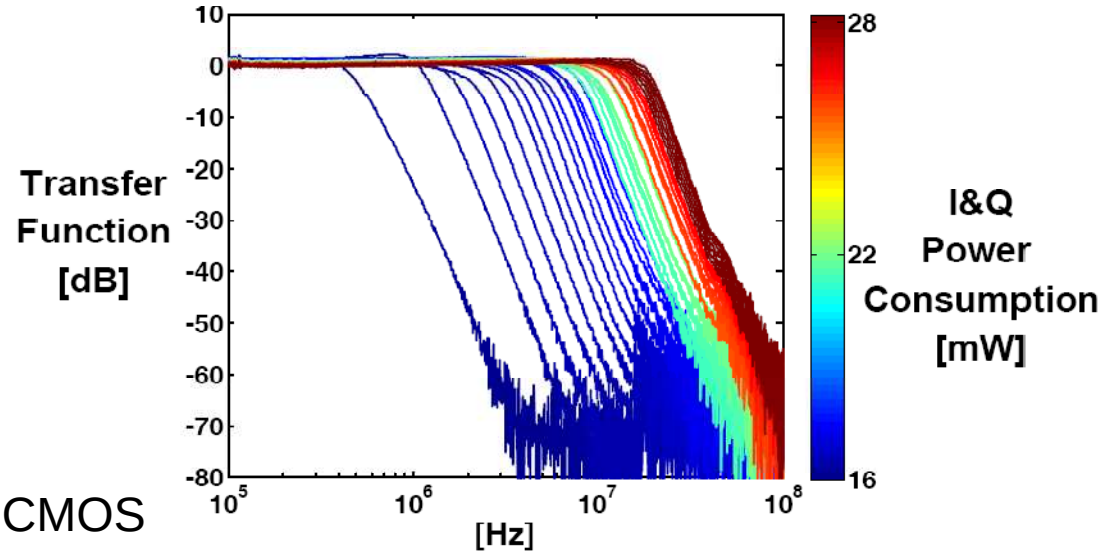
- We can make wide band LNA’s, but what about the receiver?

What about the RX architecture?

- Commodity is to use passive mixers
  - Inherently wide band nature as they act as switch only
  - Can be made very linear
- Followed by analogue wide band BB filters
  - Tunable in filter order, bandwidth

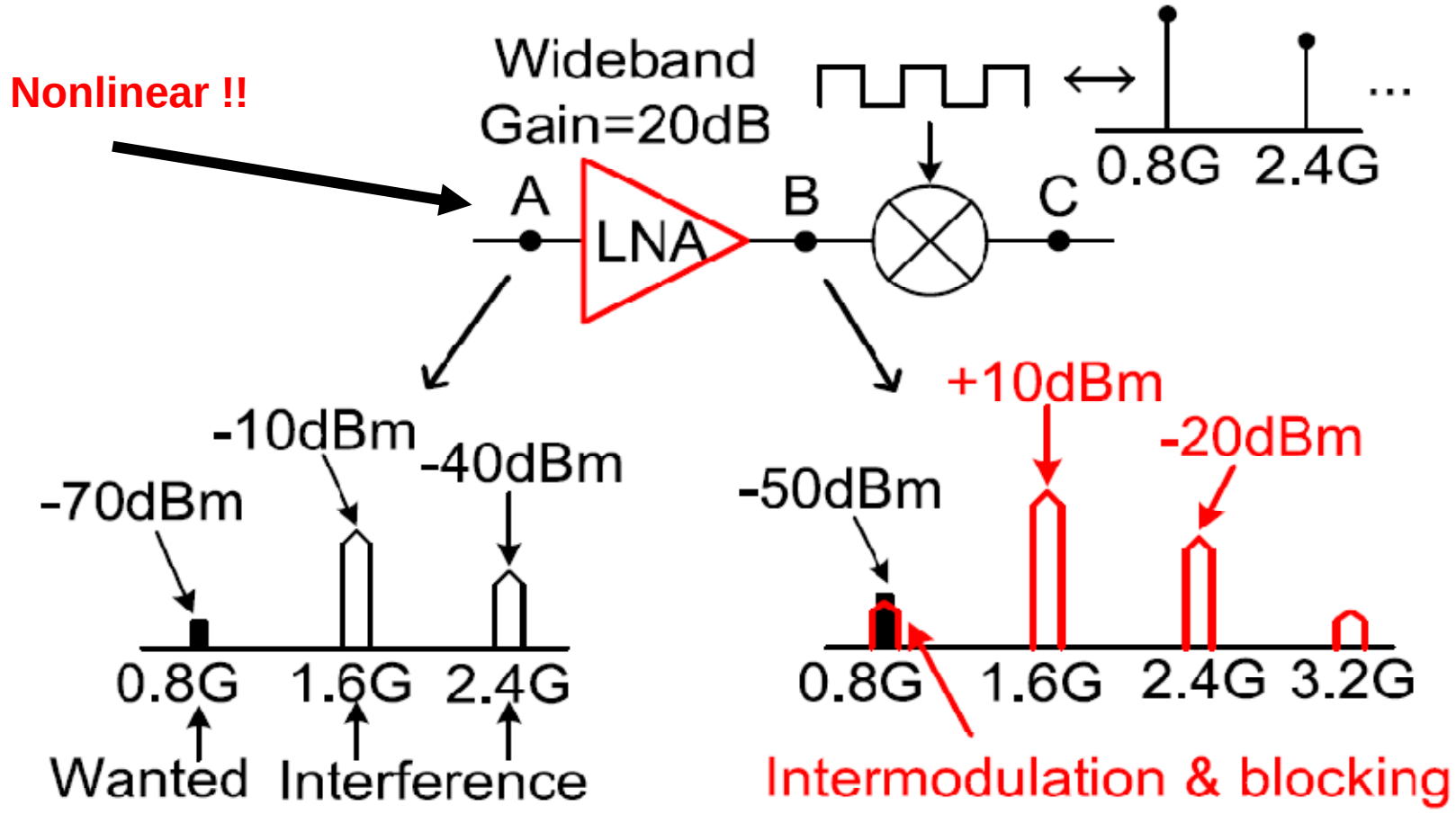
‘Classical’ ZIF architecture





ISSCC 2009: IMEC, SDR in 45nm CMOS

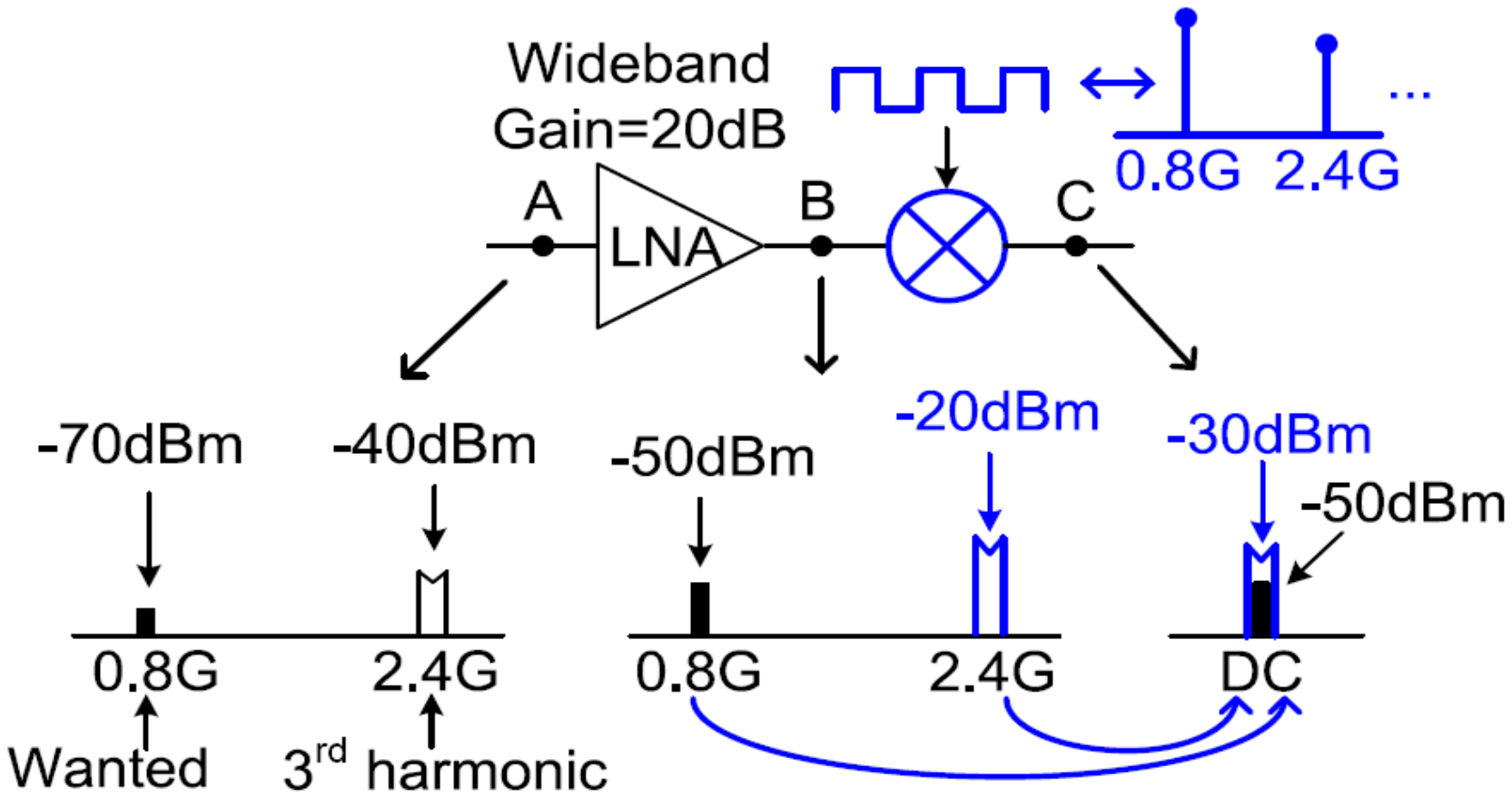
... but how to handle interferers?



Wide band at RF give rise to interference issues

ISSCC 2009: Ru, SDR in 65nm CMOS

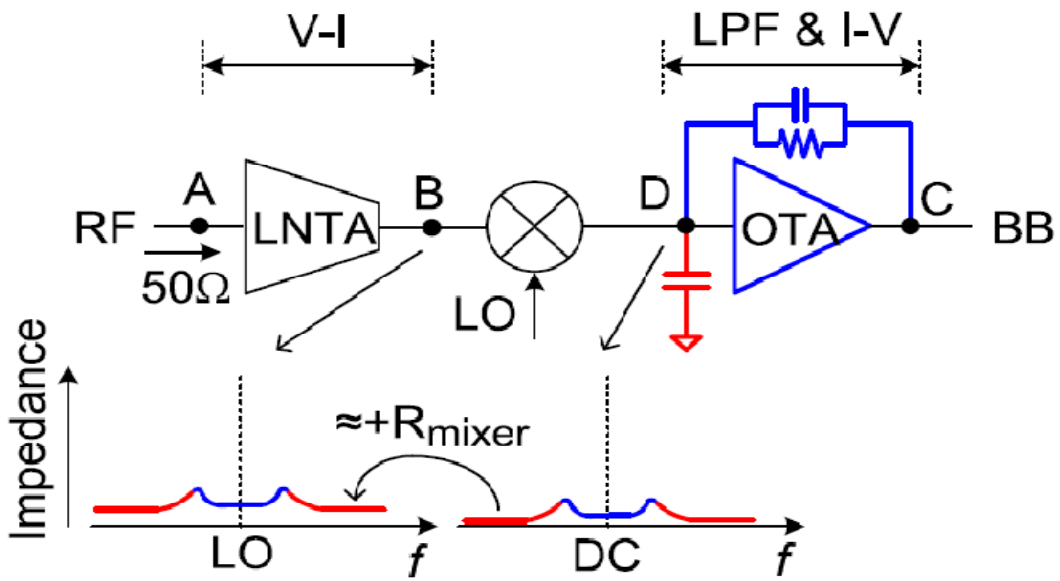
... but how to handle interferers?



and 'square-wave' LO results in harmonic mixing

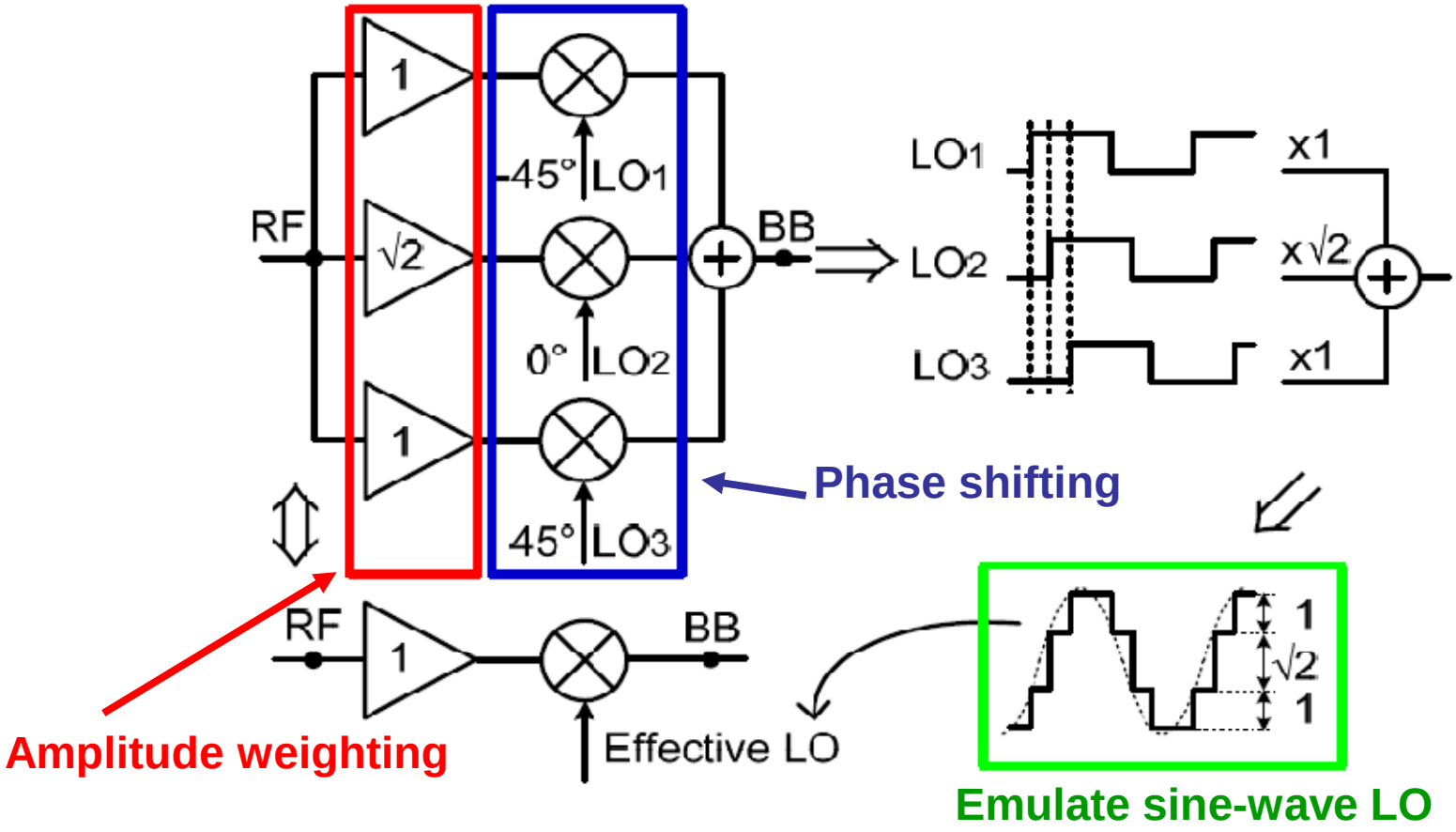
... but how to handle interferers?

- One solution is to use band-pass filters
  - Need tunable BP, difficult at RF
- Other solution is to NOT make (too much) gain at RF



ESSCIRC 2001: Leenaerts, 180nm CMOS

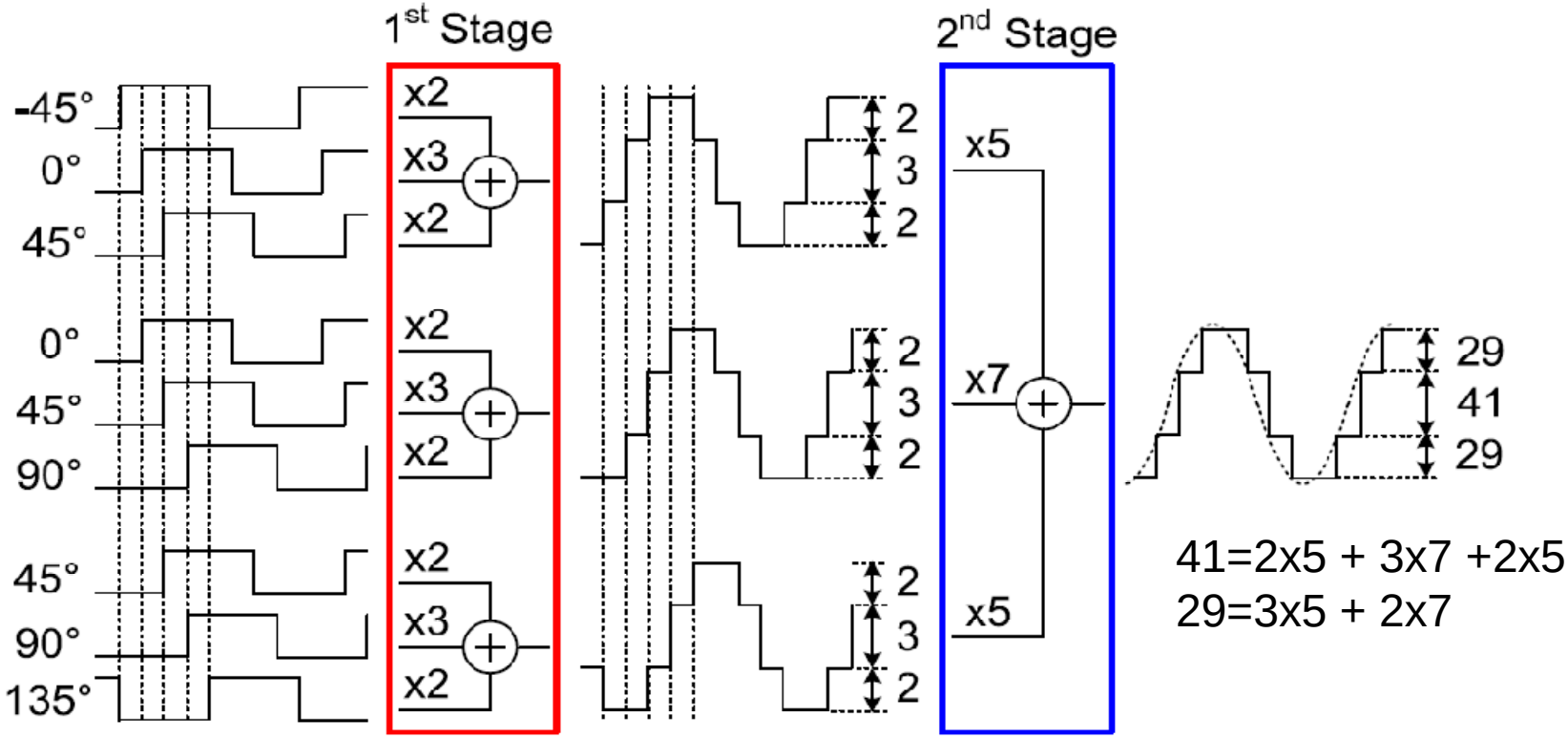
… but harmonic mixing remains



harmonic rejection mixer removes 3*LO and 5*LO

ISSCC 2001: Weldon

… but how to make $\sqrt{2}$ accurate?

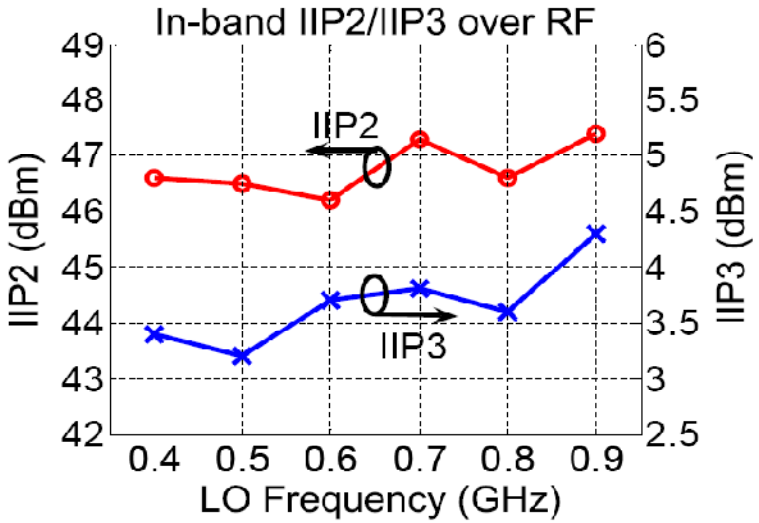


41/29 = 1.4138 and $\sqrt{2}$ = 1.4142, so error is 0.03%

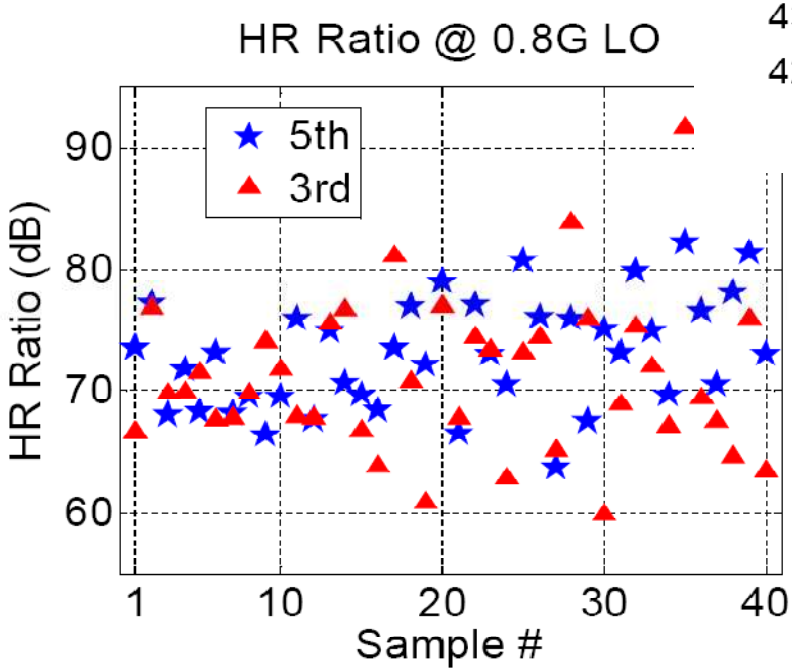
2-stage poly phase network

ISSCC 2009: Ru

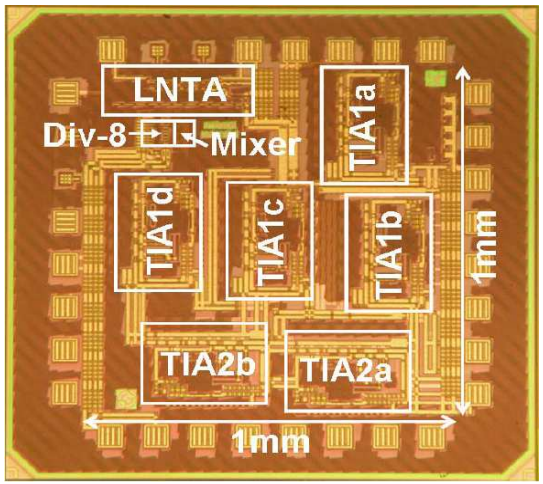
And the result …



LO Frequency	0.4~0.9GHz
Gain	34.4±0.2dB
DSB NF	4dB±0.5dB
S_{11} < -10dB	80M~5.5GHz
In/Out-of-band IIP3[1]	**+3dBm / +18dBm**
In/Out-of-band IIP2[2]	+46dBm / +51dBm
IF Bandwidth	12MHz
1/*f* noise	**30kHz** corner



Min. HR5=64dB
Min. HR3=60dB

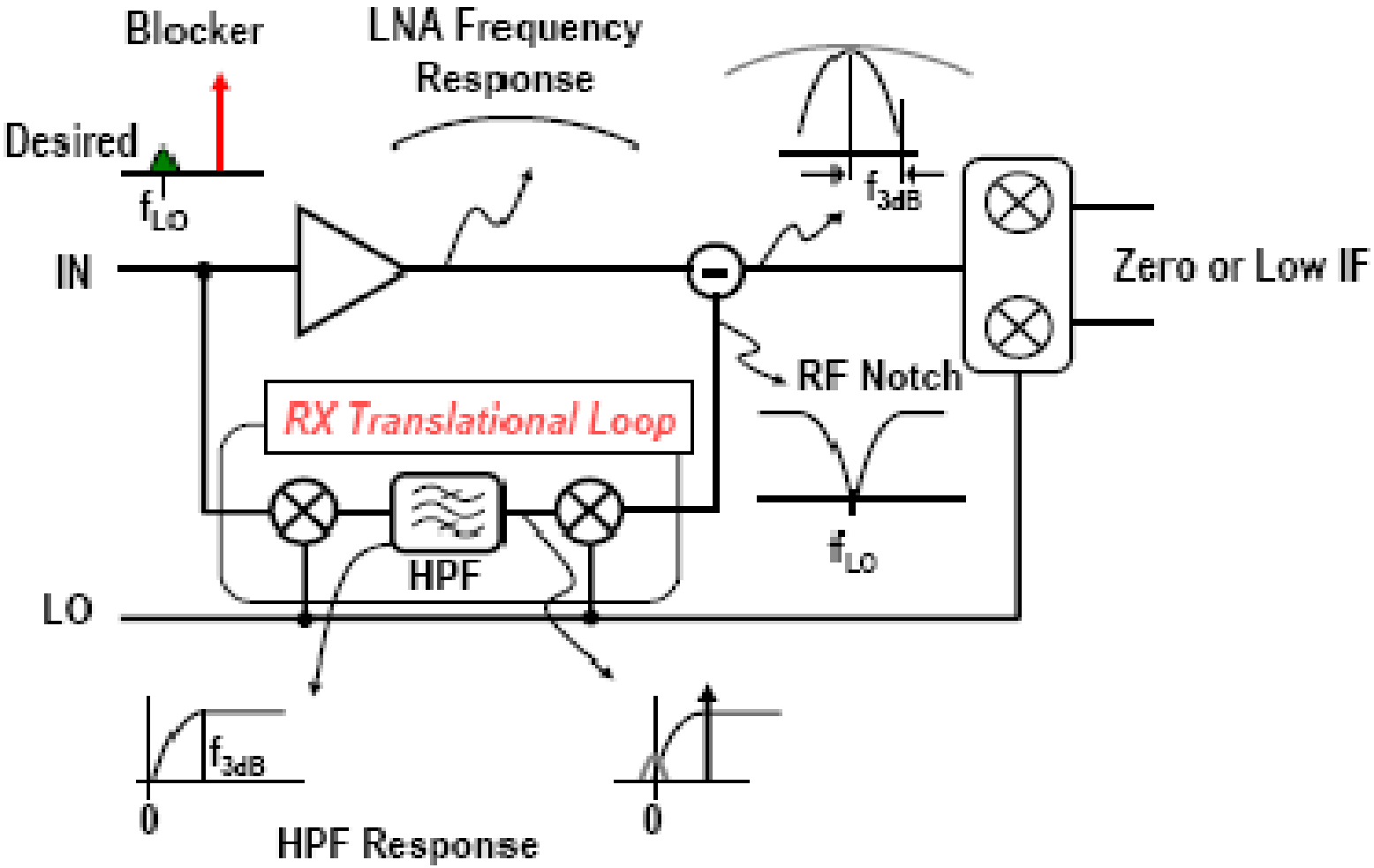


65nm CMOS

… but what about other interferers?

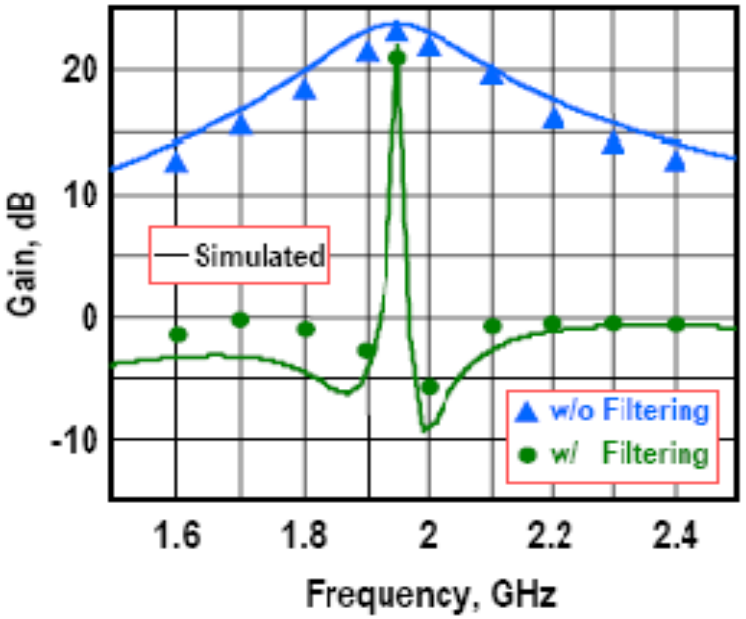
- Harmonic mixing helps only for interferers which are at harmonics of the used LO frequency
- How do we improve robustness against other interferers?
  - Make notch at RF

Notch at RF by translational loop



Darabi, ISSCC 2007

Notch at RF by translational loop



Parameter	Measured, w/ filtering	Simulated, w/ filtering	Measured, w/o filtering	Simulated, w/o filtering
Gain	20.9	21.3dB	23.4	23.5dB
NF	6.8dB	5.8dB	3.9dB	3.5dB
In-Band IIP3	N/A		2.6dBm	2.8dBm
3-dB Bandwidth	4.5MHz	6MHz	250MHz	220MHz
Stop-band Rejection	> 21dB	> 23dB	3dB	3dB
S_{11}	< -10dB	< -10dB	< -10dB	< -10dB
Current Drain	29mA	29mA	8mA	8mA
Power Supply	1.2/2.5V			
Operating Temperature	-20°C to 85°C			
Active Die Area	0.28mm²			
Technology	65nm CMOS			

Impact on NF of LNA is 3dB, so activate filter only in presence of interferer

Darabi, ISSCC 2007

Some conclusions

- Wide Band CMOS design is possible
  - Convergence towards a receiver comprising wide band LNA, passive mixers and BB filtering
  - Additional tricks added to cope with interference are still needed
- But which technology is favorable?

What about the technology?

Does CMOS scaling improves wide band behavior?

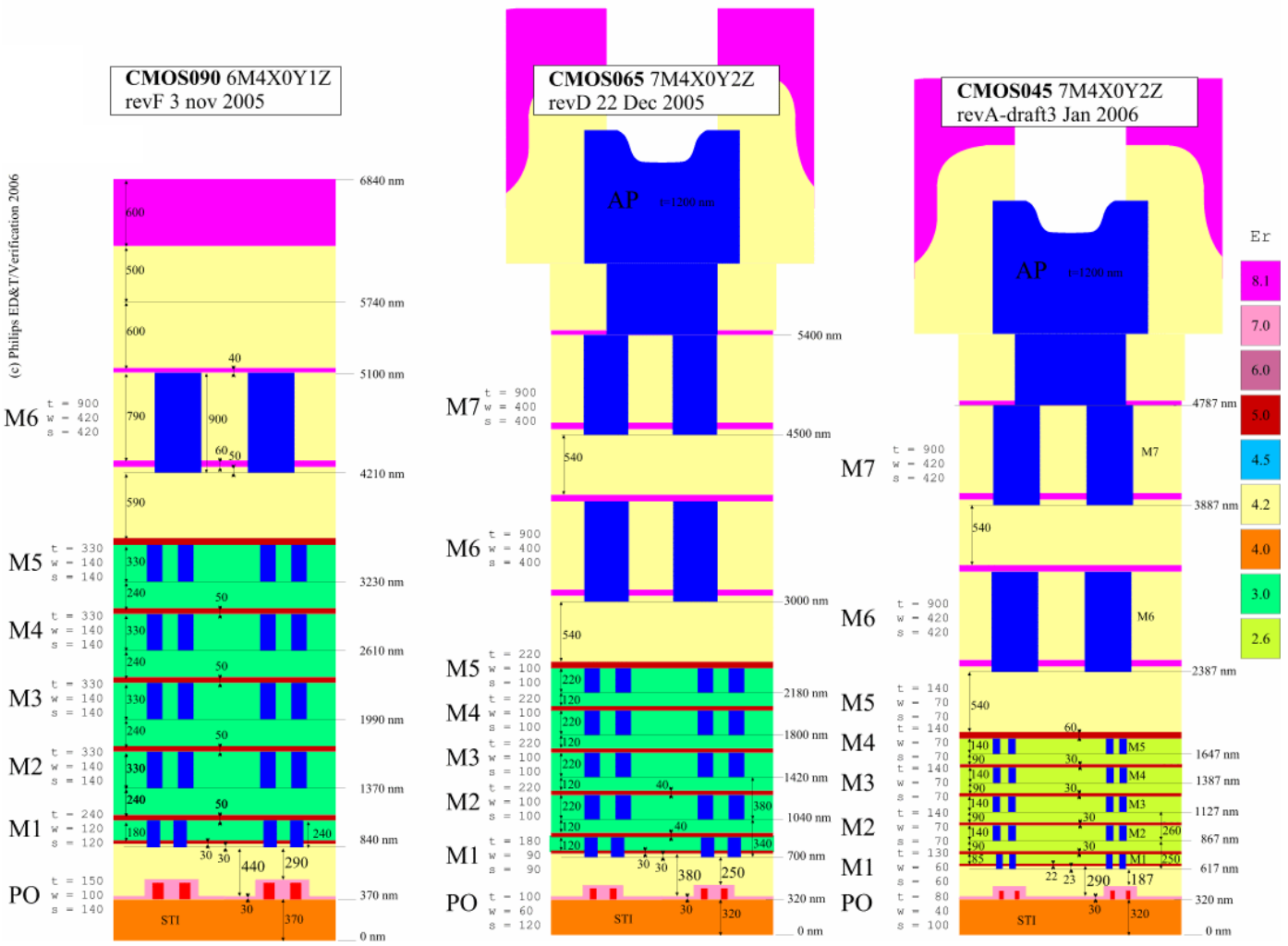
- Technology RF performance
  - 180nm, 90nm, 65nm, 45nm
- UWB CMOS circuits
  - 90nm, 65nm, 45nm (and SiGe BiCMOS)
- UWB receiver design
  - 65nm, 45nm

Used technology

- All experiments have been done in a *low standby power* process node, i.e. LP CMOS

CMOS	90nm	65nm	45nm
Lgate [um]	0.1	0.06	0.04
Vdd [V]	1.2	1.2	1.1
$I_{em,M1,minW}$ [mA@110°C]	0.21	0.11	0.07
#metal	6 + ALU	7 + ALU	7 + ALU

Technology



$$C = \varepsilon_o \varepsilon_r \frac{\text{Area}}{\text{distance}}$$

Some definitions

- Cut-off frequency ft
  - unity gain current frequency for short-circuited output

$$f_T \sim \frac{g_m}{2\pi C_{gg}}$$ → **input capacitance**

- Voltage gain bandwidth fa
  - Frequency for 3-dB DC voltage gain drop, calculated for a resistive load making the DC voltage gain 2x

$$f_A \sim \frac{g_m}{2\pi A_{dc} C_{dd}}$$ → **output capacitance**

Some definitions

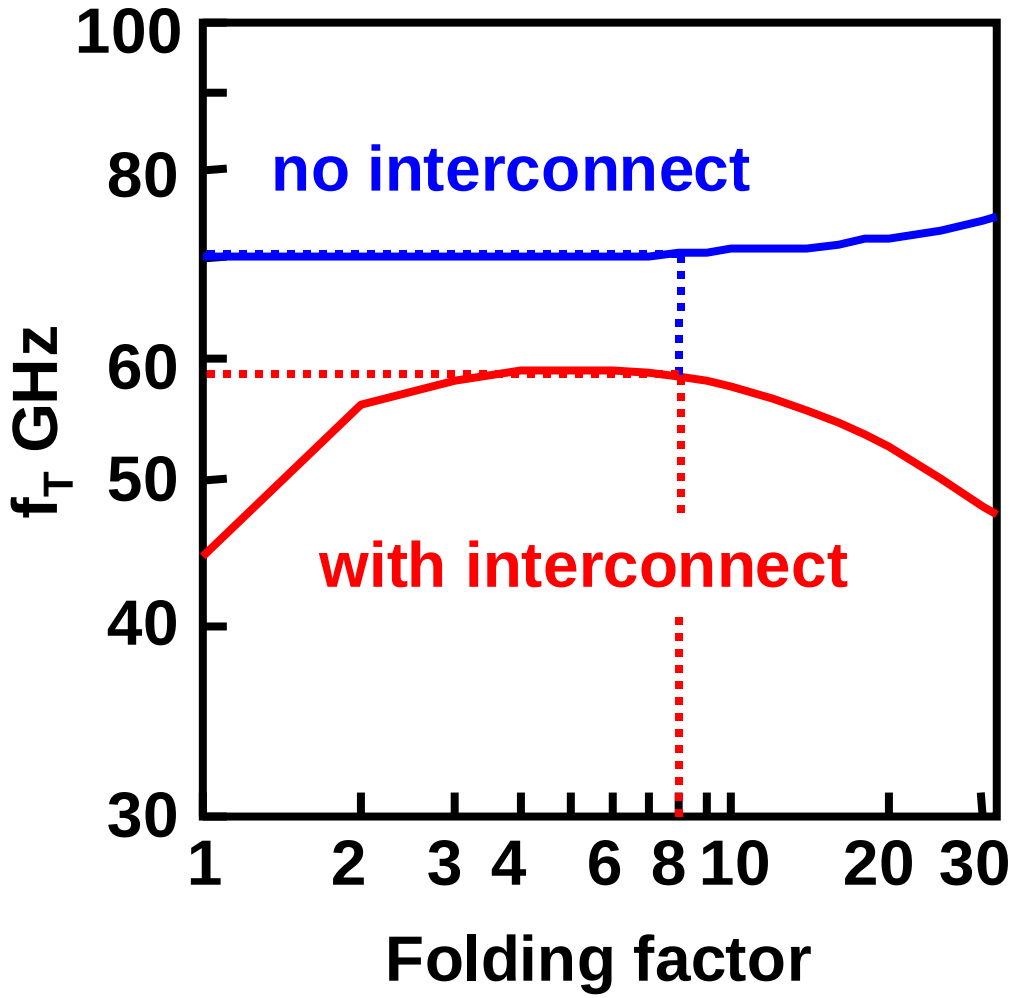
- 1-dB minimum Noise Figure frequency (fNF1dB)
  - frequency for which this NF is still reached assuming optimum NF matching
- Finger width Wf
  - Folded device finger width: Wf = W/FOLD

Difference schematic - layout

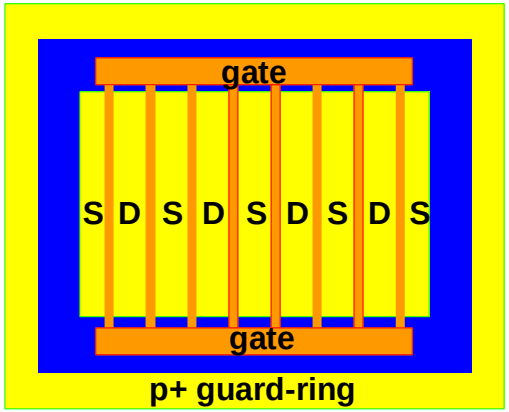
- Schematic
  - MOS model takes into account ***naked device*** behavior.
- Layout
  - parasitics due to metal connections, especially CO-M1
  - metal layers to fulfill current reliability

Layout has major impact in deep sub-micron

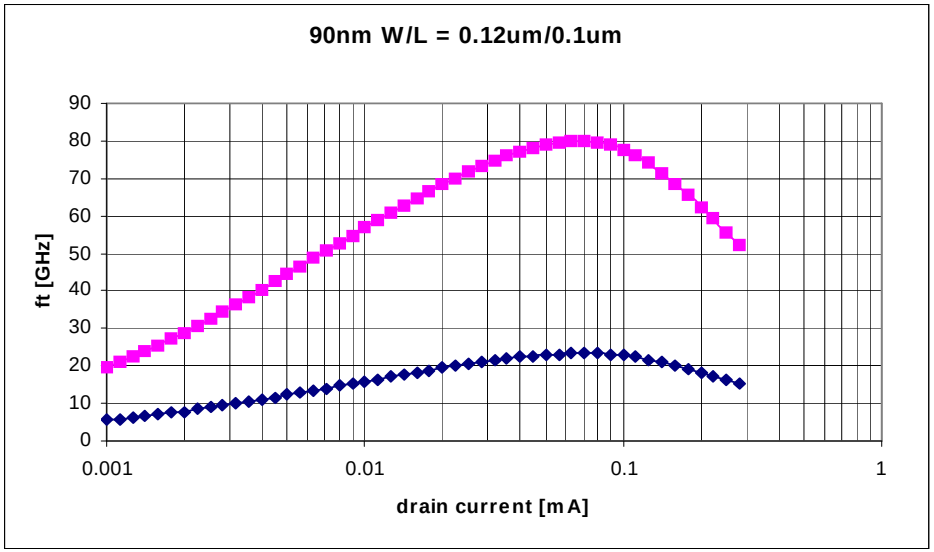
Difference schematic - layout

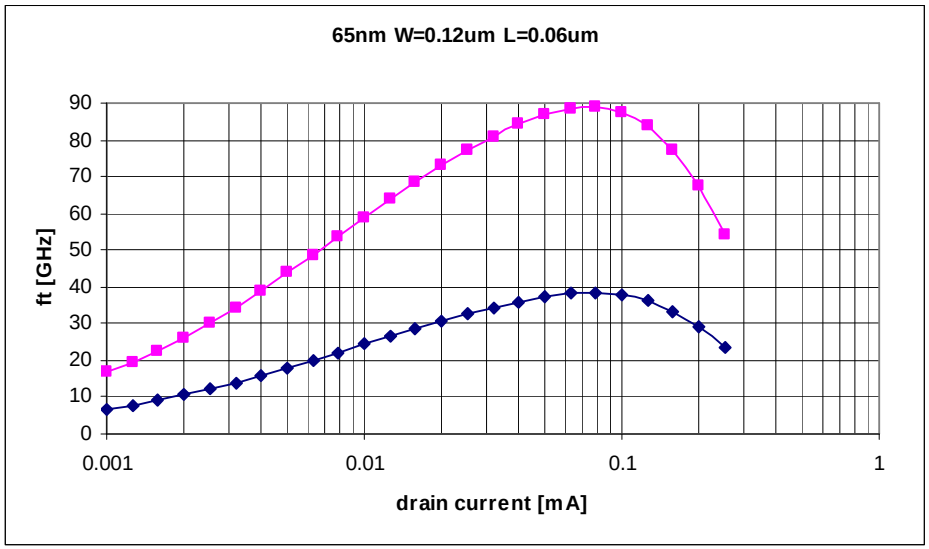


- NMOS device
- L = 0.18 um
- W = 32 um
- contact = 2
- @ fold = 8
  - fT =70 GHz
  - fT =60 GHz



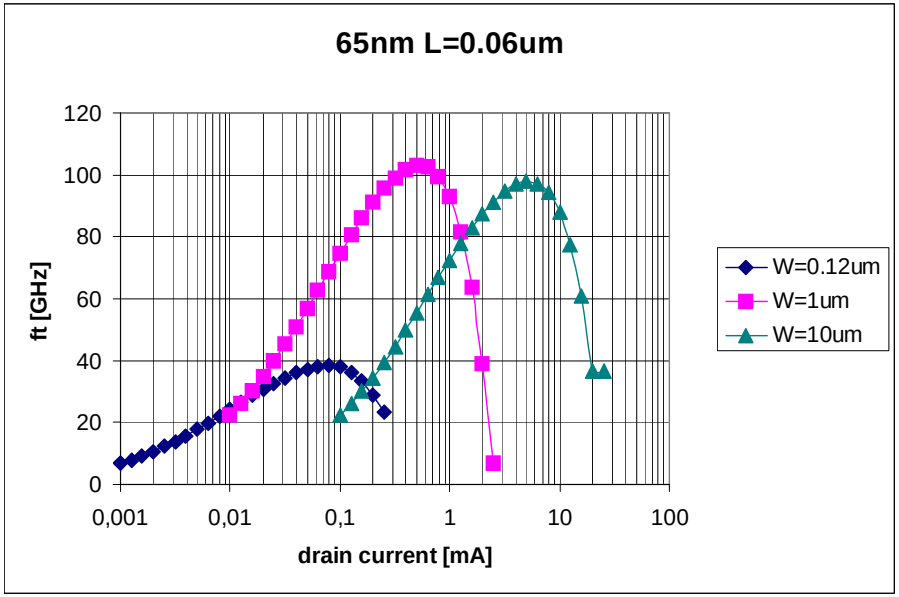
Comparison of this effect

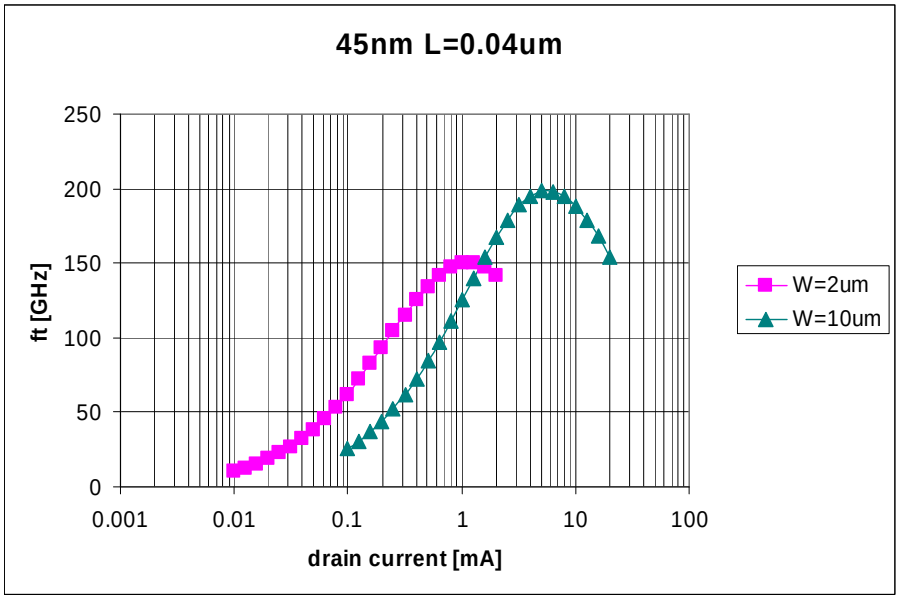




- For both devices: single finger, double gate contact
  - Purple: schematic (naked device)
  - Blue: layout extraction
- Serious impact of metallization
  - 90nm: 70%
  - 65nm: 55%

65/45nm: ft obtained after layout





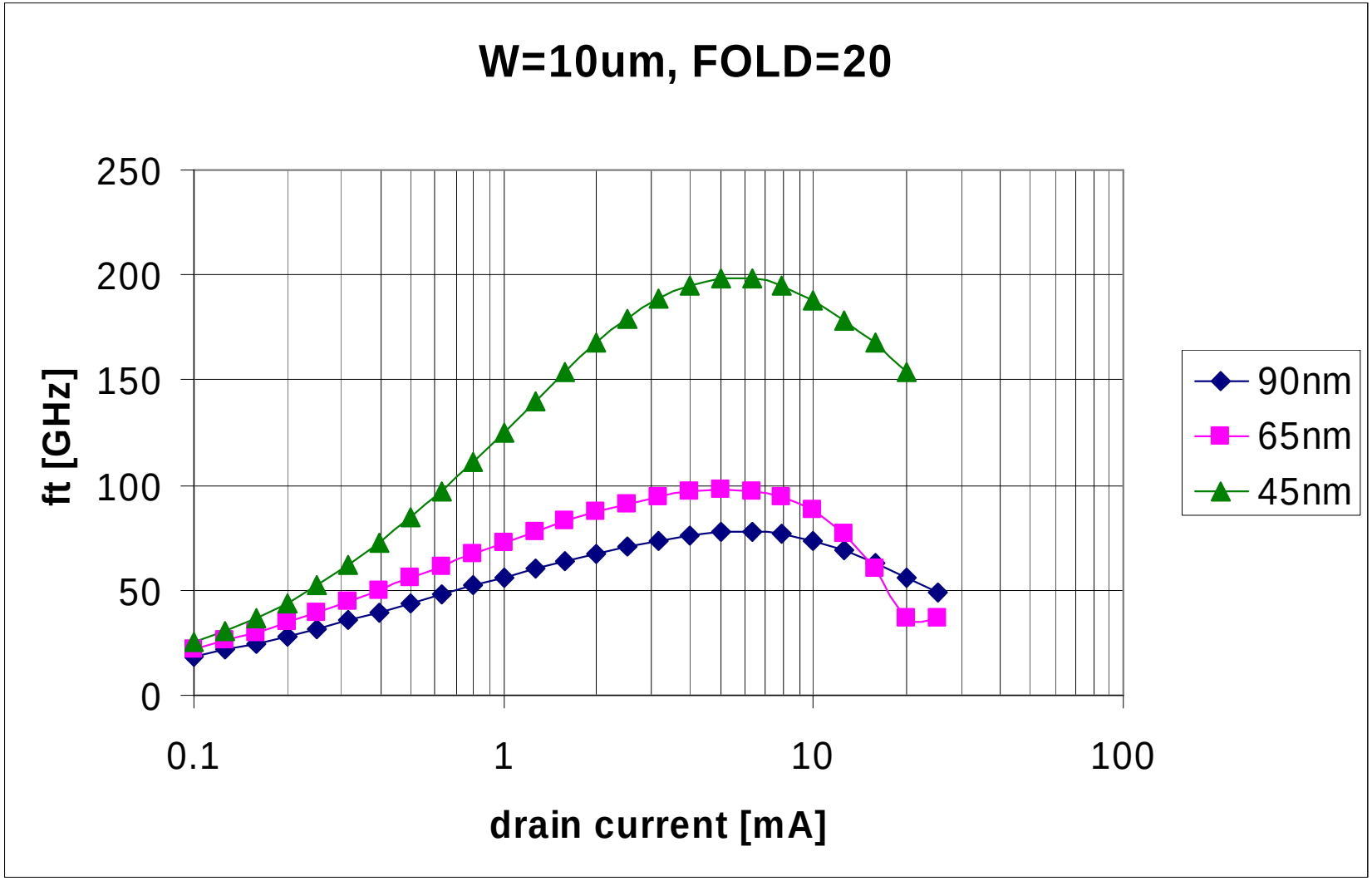
65nm LP: ft naked device: 160GHz

45nm LP: ft naked device: 270 GHz

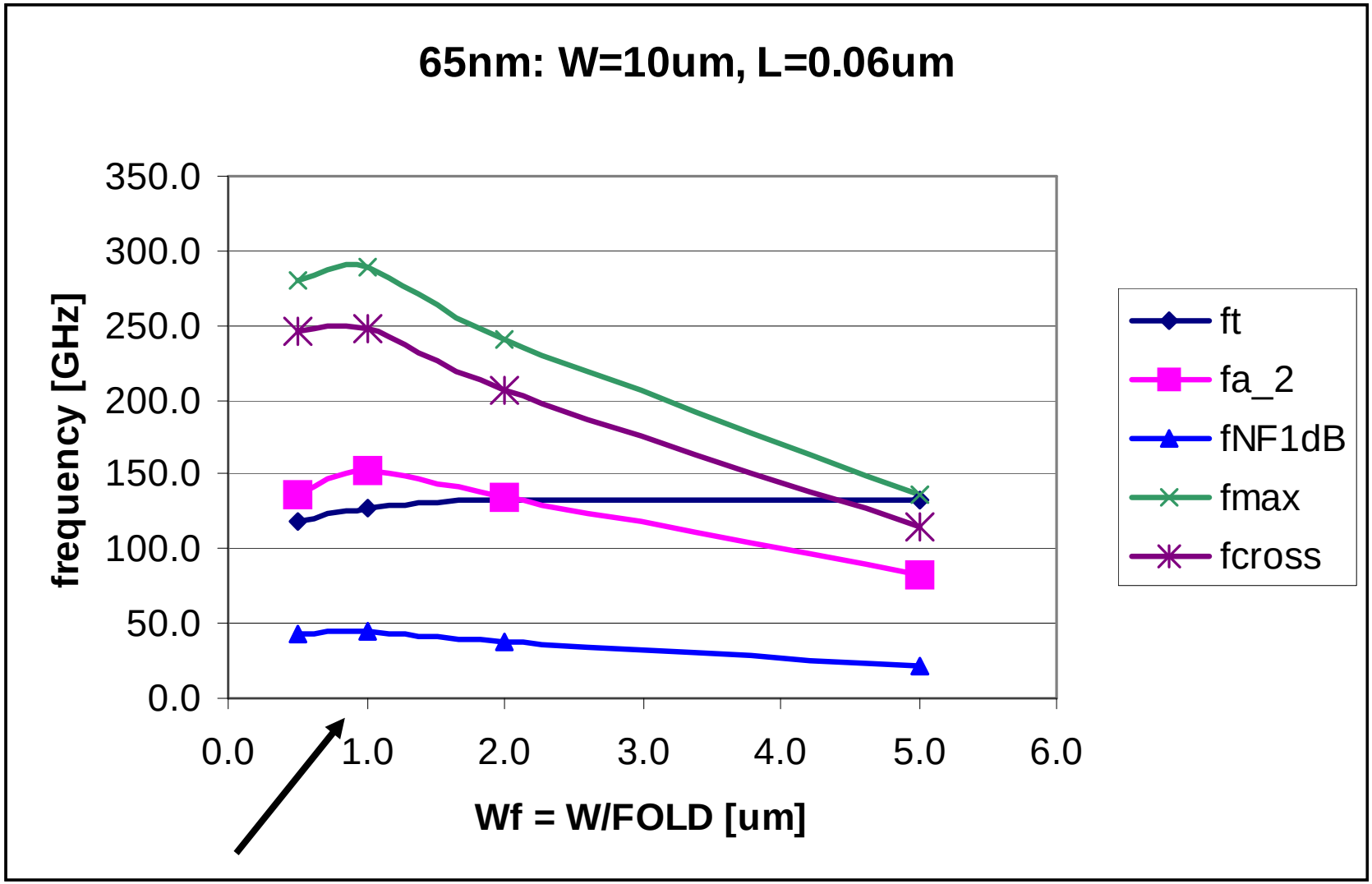
(Wf = 0.5 um for 1 and 10 um)

(Wf = 0.5 um for 2 and 10 um)

Comparison for ft: scaling helps



65nm: influence of finger-width

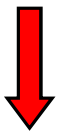


seems optimal

layout includes only M1

RF performance incl. all layout effect

CMOS	ft [GHz]	fa [GHz	fNF1dB [GHz]	Wf opt.
180nm	41	39	10	≈ 3
90nm	80	72	40	≈ 1.7
65nm	120	110	44	≈ 1
45nm	200	130	53	≈ 0.67

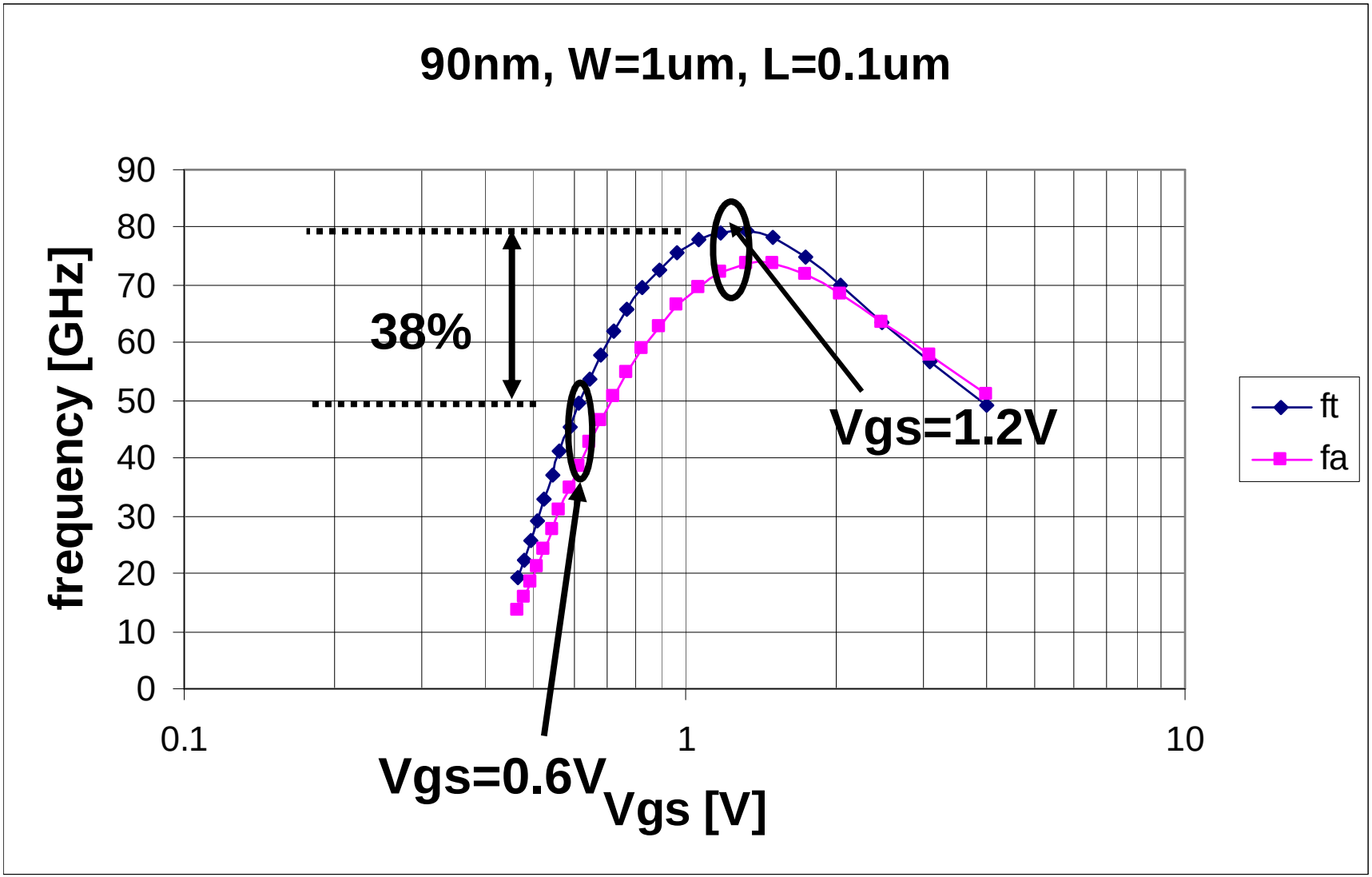


Wf/Lmin ≈ 16

How realistic is peak ft, fa?

- Peak values are normally reached for Vgs close to Vdd
  - happens for instance in cross-coupled diff pair in most VCO topologies
- But what happens in more realistic situations, e.g. Vgs = 1/2Vdd?
  - e.g. situation in frequency divider, LNA, …

How realistic is peak ft, fa?



How realistic is peak ft, fa?

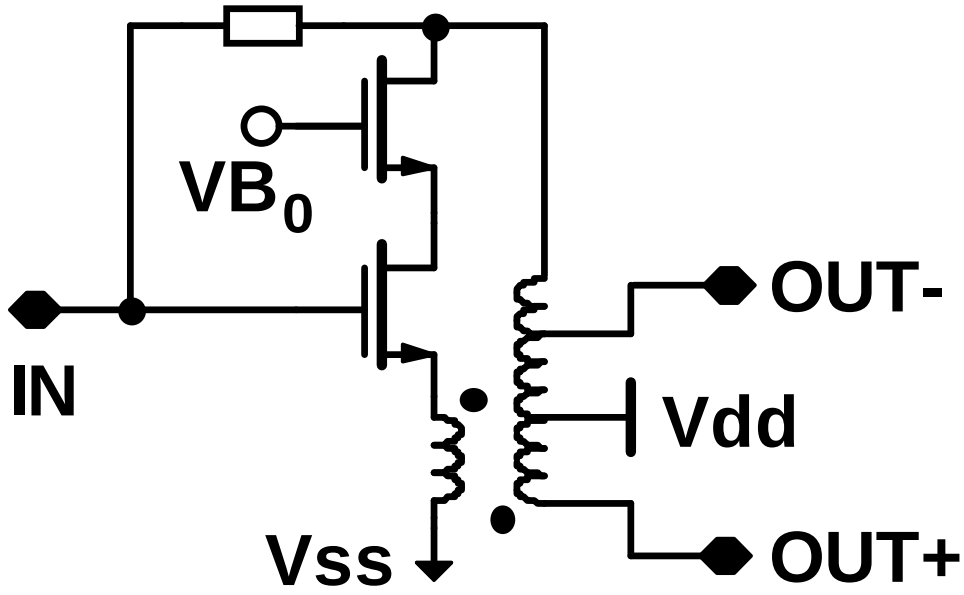
CMOS	90nm	65nm	45nm
Naked device	115	160	270
Vgs=Vdd	80 / 72	120 / 110	200 / 130
Vgs=1/2Vdd	49 / 38	51 / 41	47 / 28

x / y = ft / fa [GHz / GHz]

Scaling and wide band RF

- **LNA performance**
- **Frequency divider performance**
- **Dual band receiver in 65nm**
- **Dual band receiver in 45nm**

A CMOS wide band LNA



Transformer:

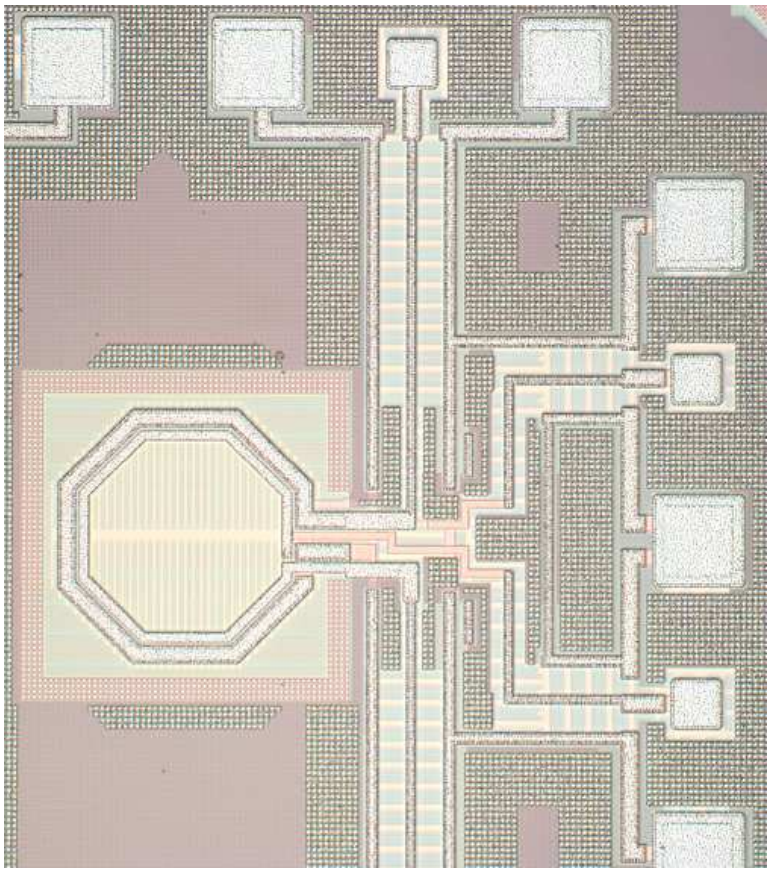
- **Single-ended → differential**
- **Impedance matching**
- **Voltage feedback**

Resistor:

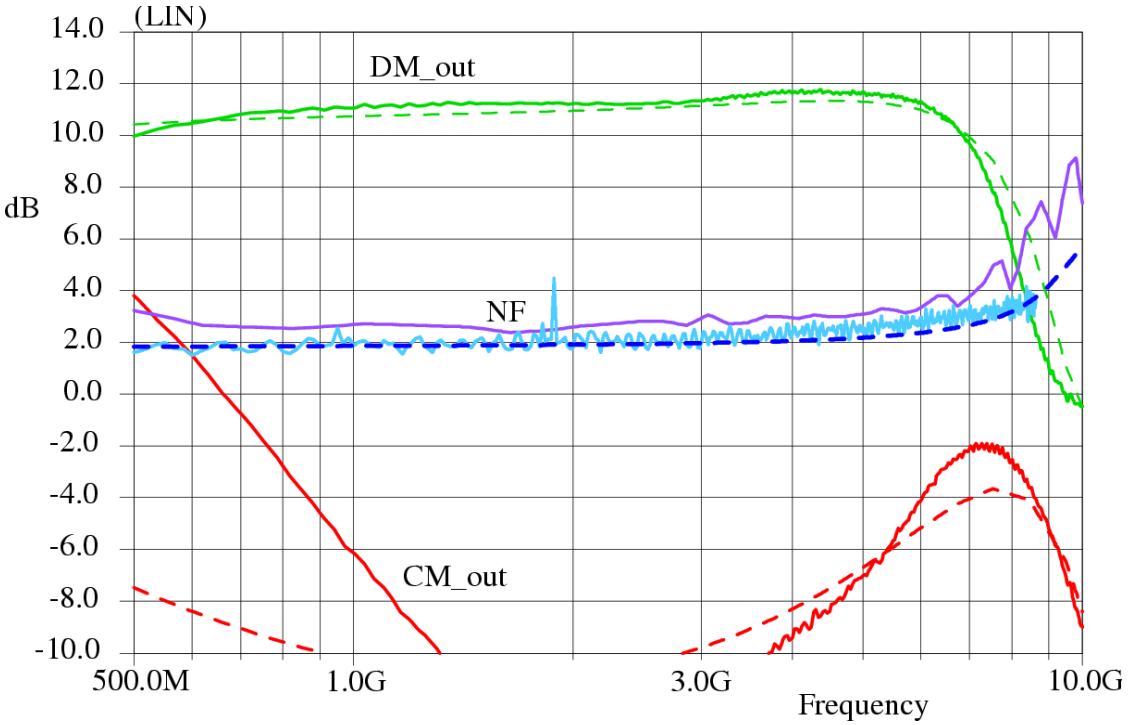
- **Current feedback**

[ISSCC2007, Lee et al.]

A CMOS wide band LNA: 65nm



[ISSCC2007]



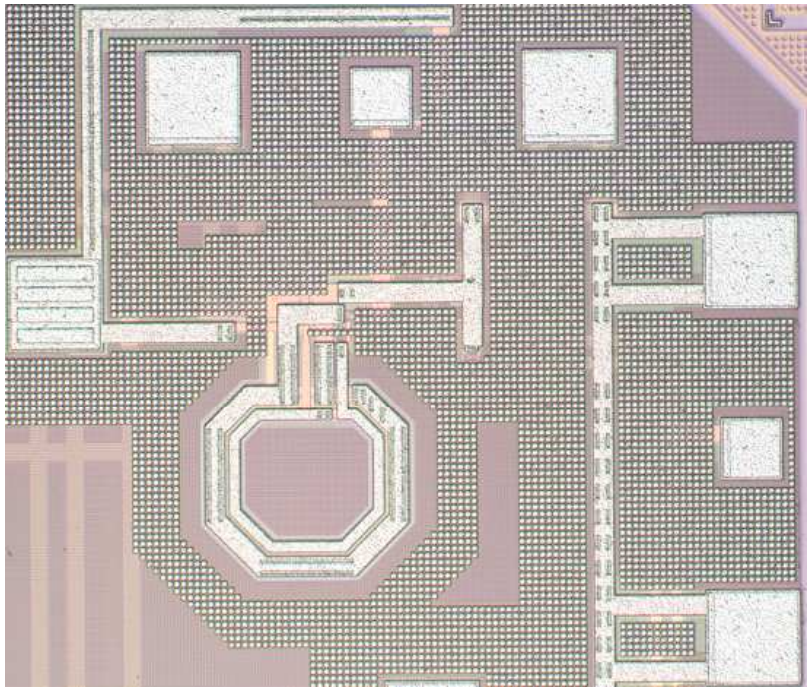
Gain: 11dB

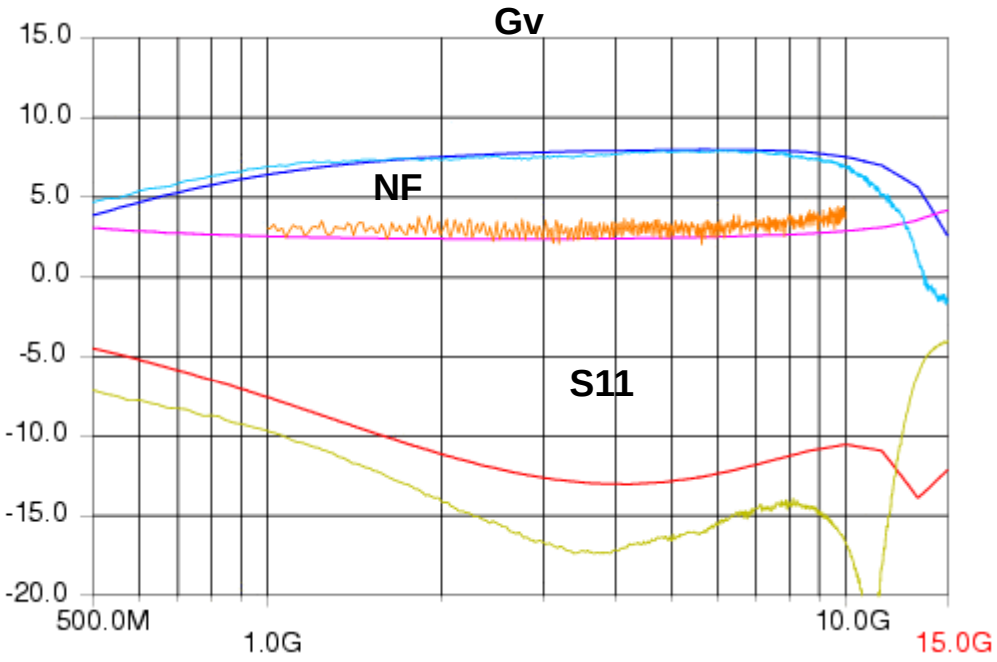
3-dB BW: 7.5GHz

NF: 2.5dB

iIP2: +25dBm

A CMOS wide band LNA: 45nm





Gain: 8dB

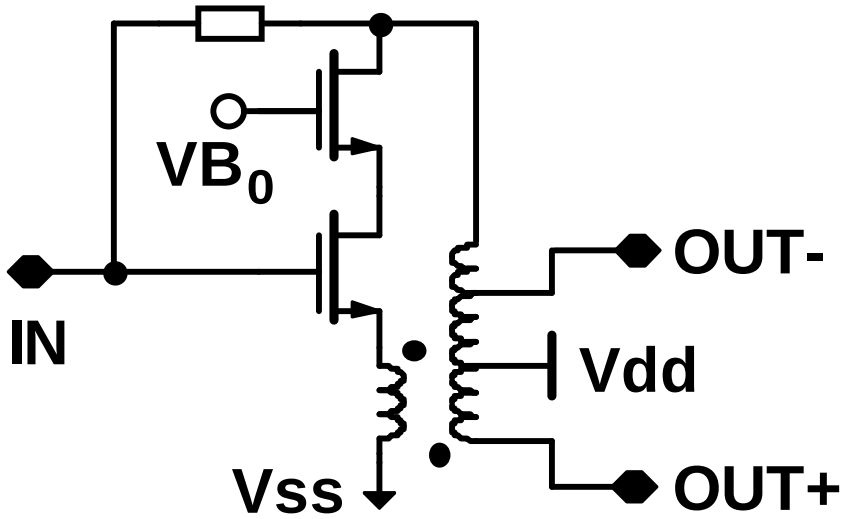
3-dB BW: 11GHz

NF: 3dB

iIP2: +25dBm

CMOS LNA: comparison

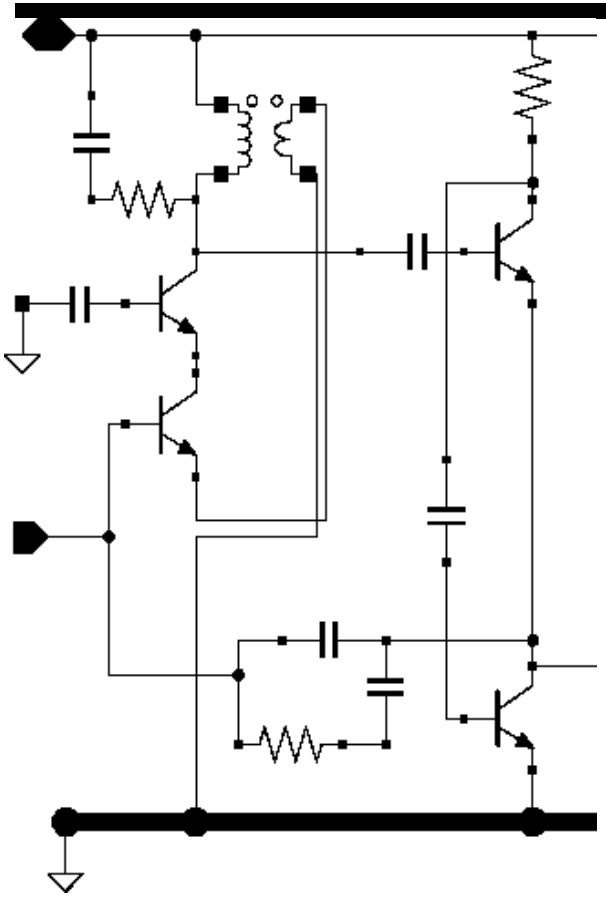
- Input device (for roughly same gm)
  - W/L 90nm: 200/0.1 um/um
  - W/L 65nm: 240/0.06 um/um
  - W/L 45nm: 200/0.04 um/um



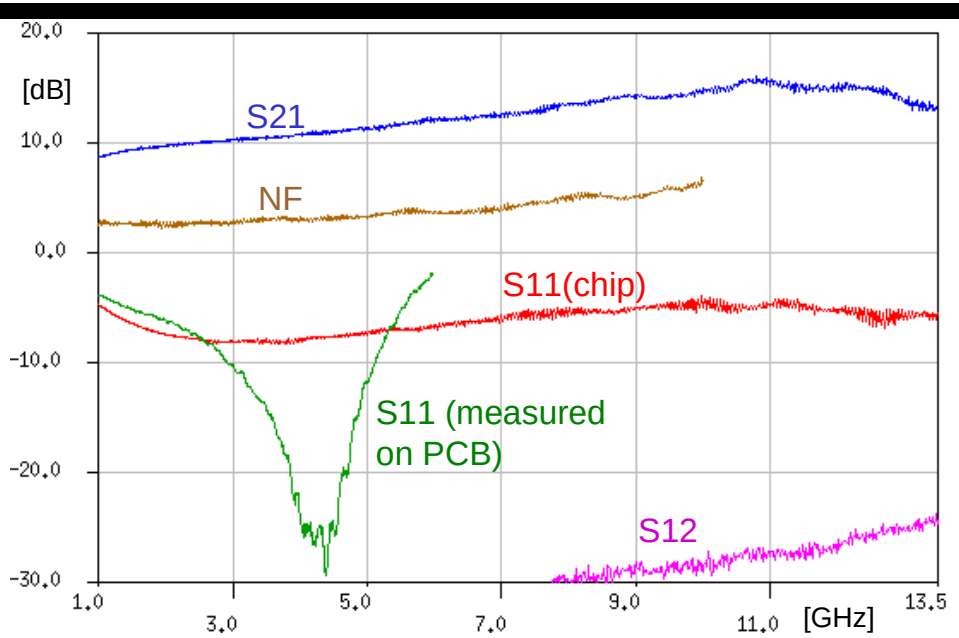
CMOS LNA: comparison

LNA	90nm	65nm	45nm
Gv [dB]	9	11	10
BW [GHz]	7.5	7.5	11
NF [dB]	2.5	2.5	3
iIP2 [dBm]	+15	+25	+25
iIP3 [dBm]	0	+12	+6
Pdiss [mW]	18	20	30

CMOS LNA versus BiCMOS

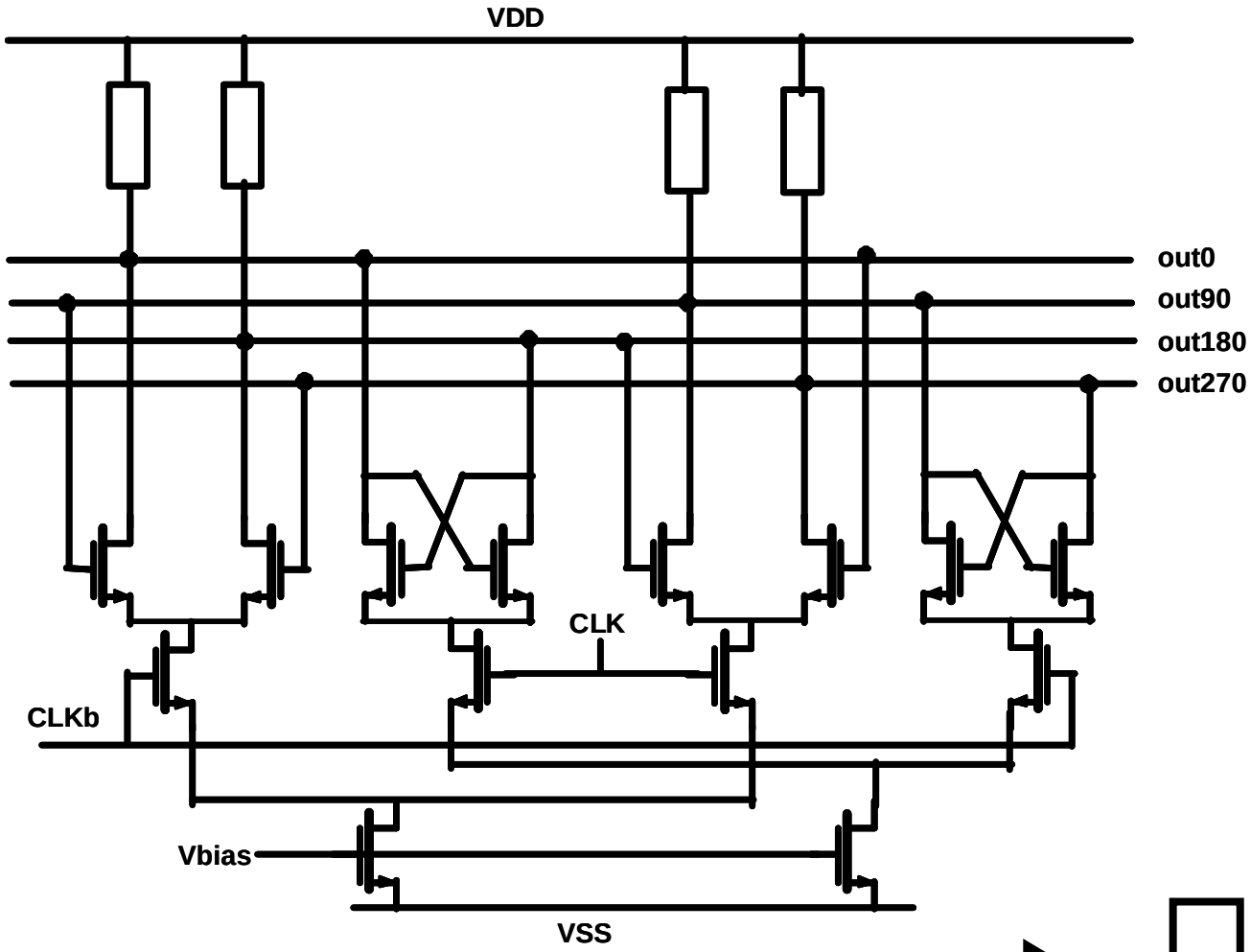


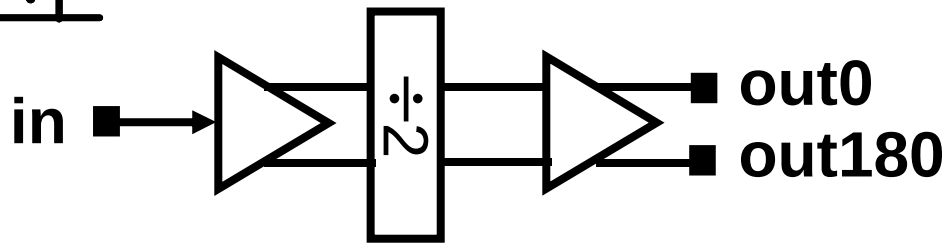
[ISSCC2005]



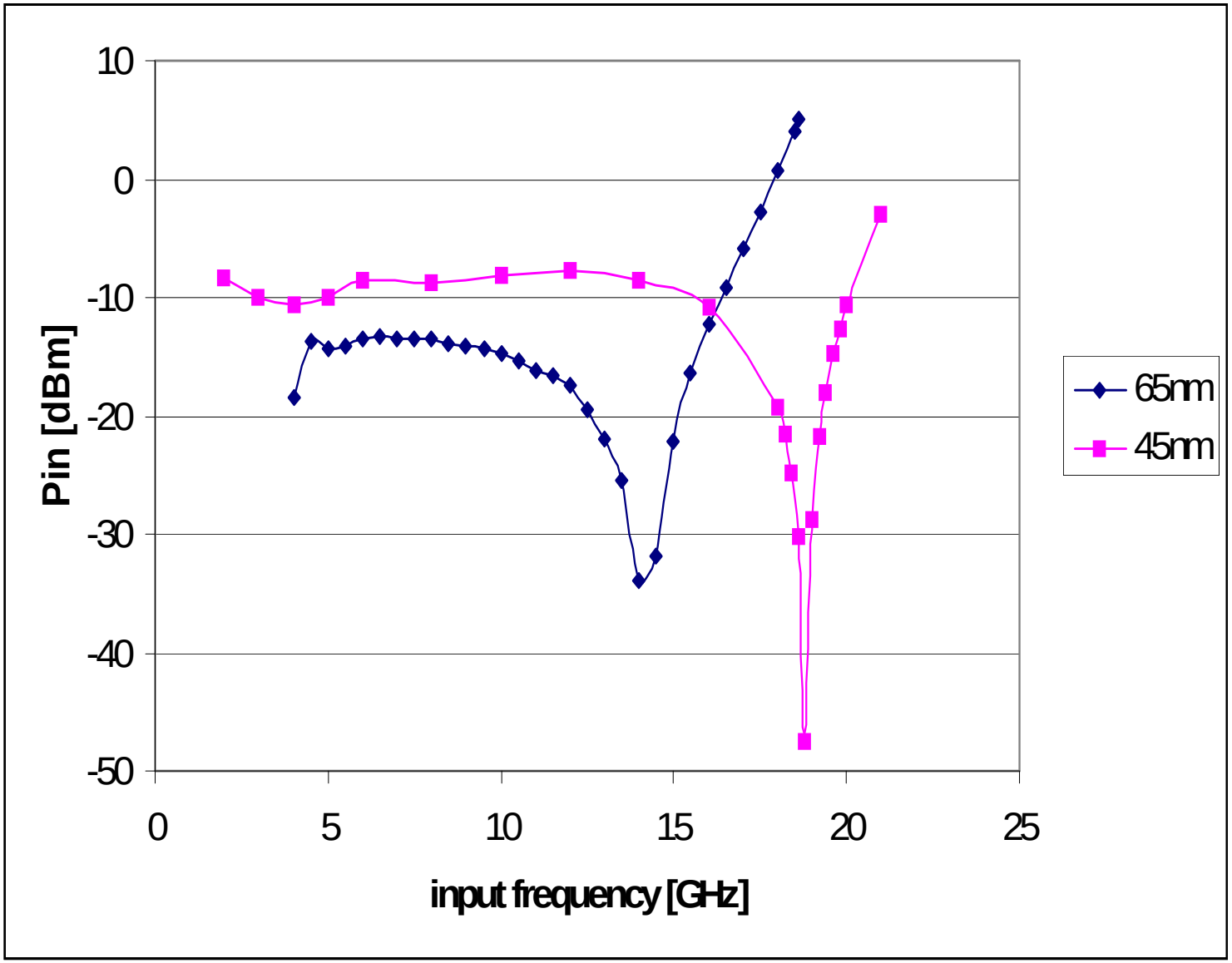
LNA	65nm	SiGe 0.25um
Gv [dB]	11	20
BW [GHz]	7.5	12
NF [dB]	2.5	3
iIP2 [dBm]	+25	+25
iIP3 [dBm]	+12	+10
Pdiss [mW]	20	12

65nm and 45nm divider chain





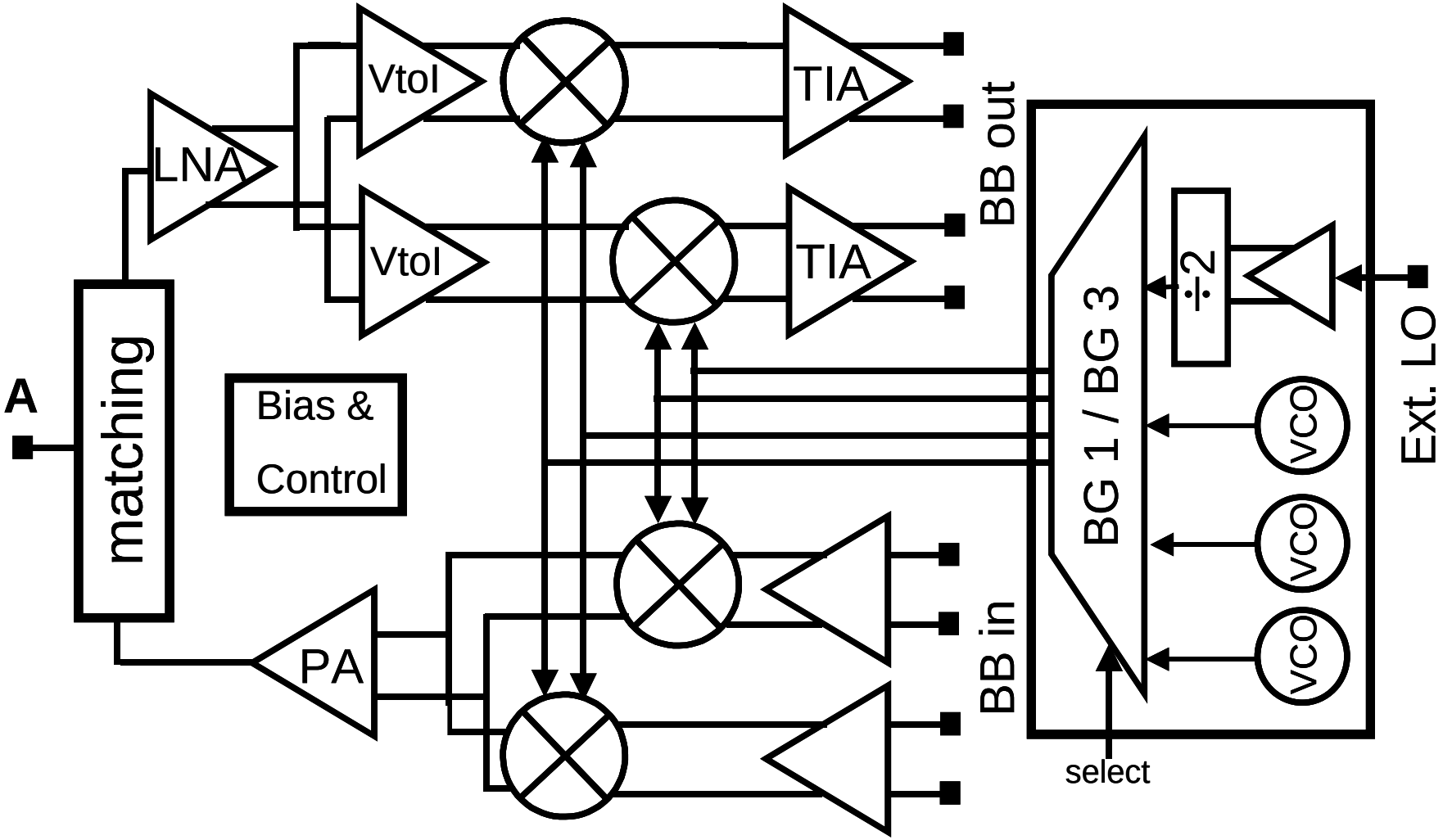
divider measurements



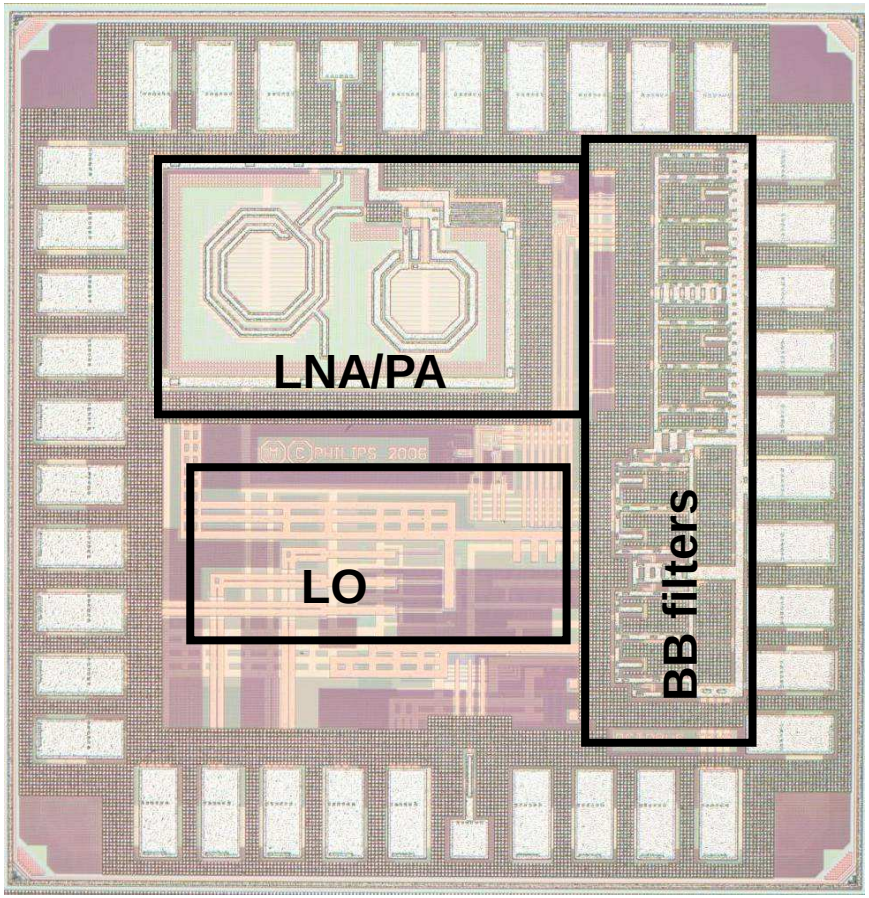
divider measurements

CMOS	65nm	45nm
Self resonance	14GHz	18GHz
Max input freq.	18GHz	21GHz
Pin	-14dBm	-9dBm
Pdiss	18mW	24mW

UWB transceiver in 65nm

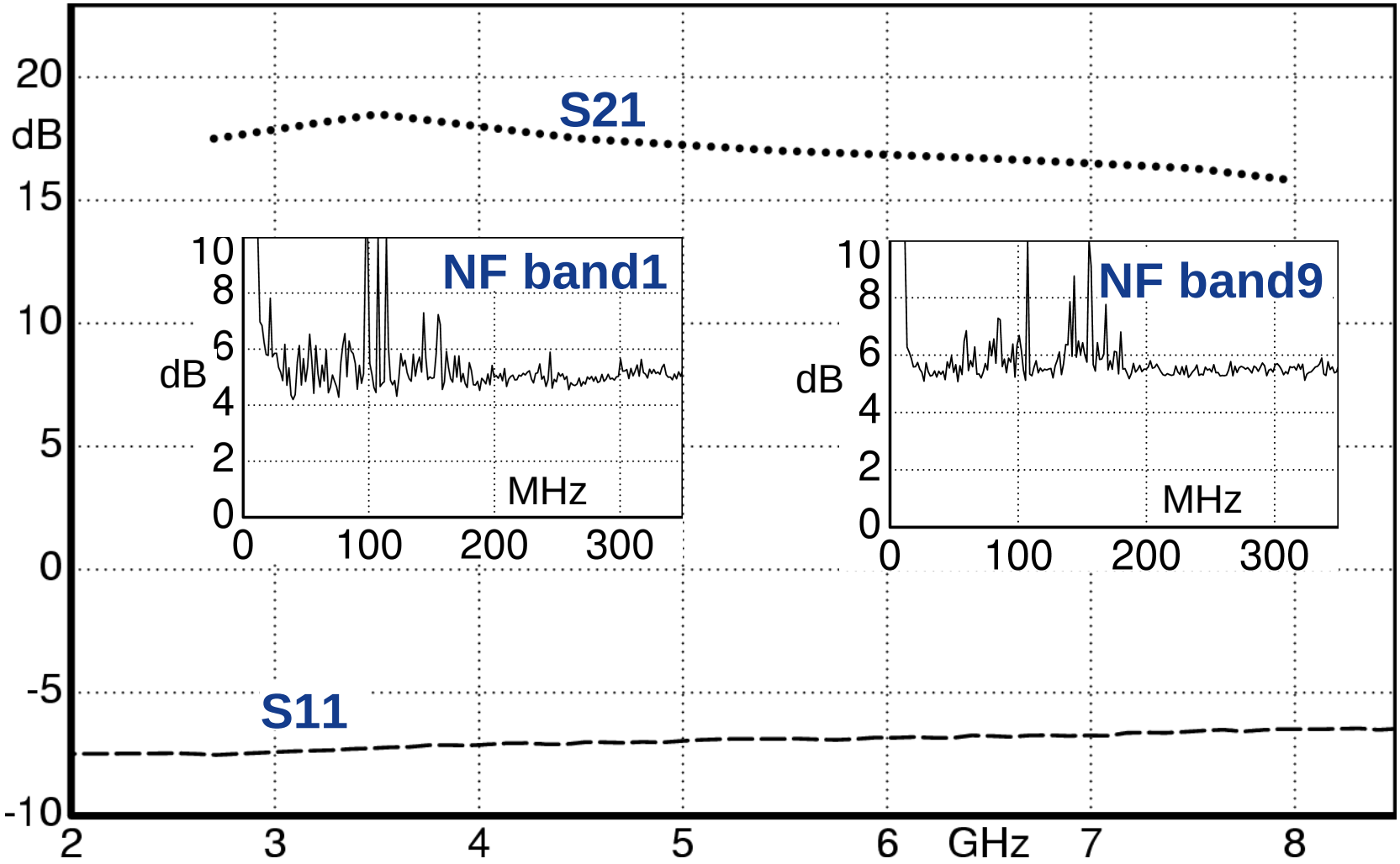


UWB transceiver in 65nm

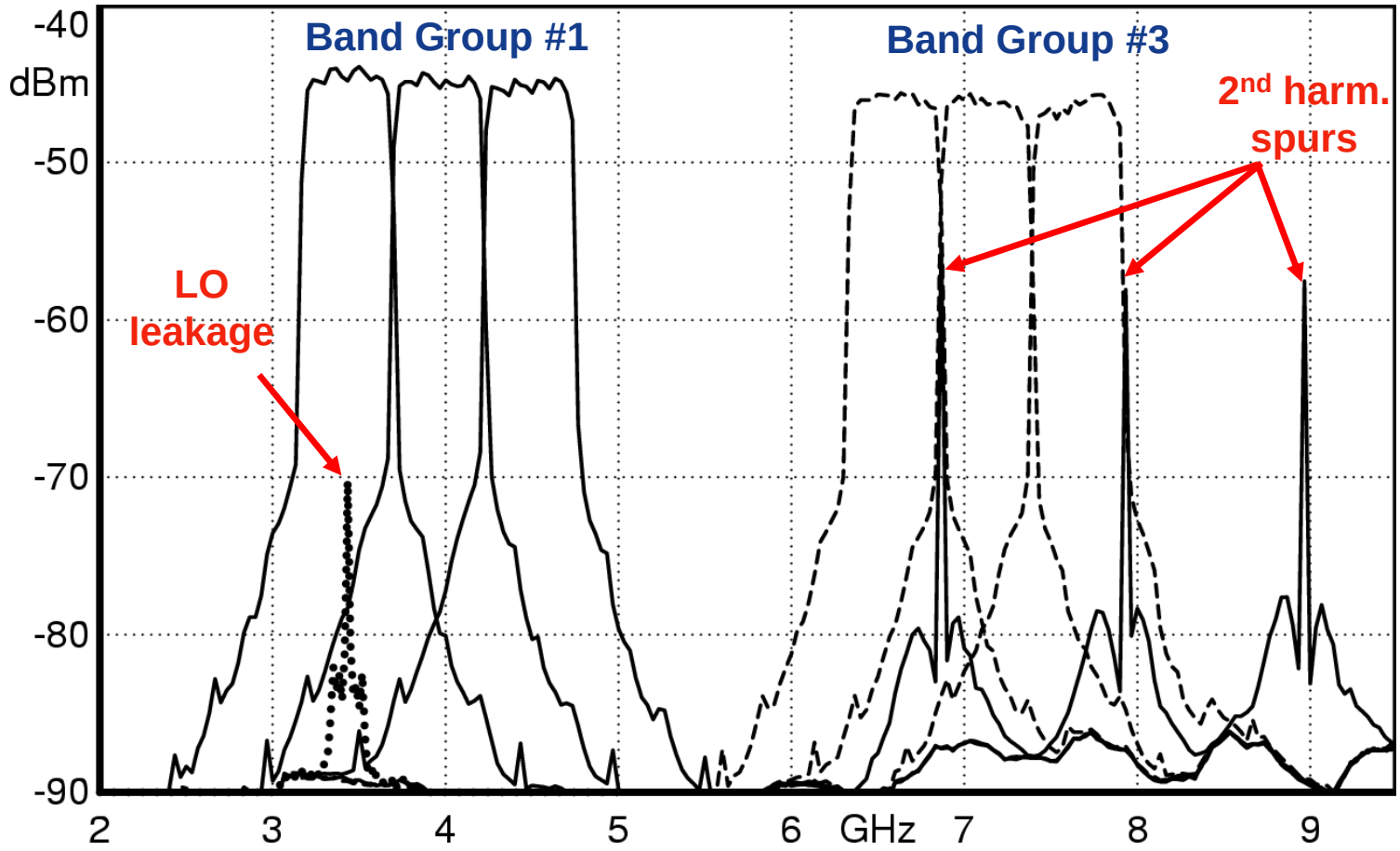


Parameter	Value	Comment
Rx noise figure	5.0 / 5.5 dB	f_{in}= 4 GHz / 7 GHz
Rx Gain	20 dB	Voltage gain, RF input to IF-output
Rx IIP2	+25 dBm	Two-tone: f_{in1}=2.4 GHz, f_{in2}=5.2 GHz
Rx IIP3	+6 dBm	Two-tone: f_{in1}=1.8 GHz, f_{in2}=2.4 GHz
Tx gain	+52 dB	IF-input to mixer output, w/o PA
Tx output EVM	4 %	At mixer output, w/o PA
Tx output flatness	< 2 dB	At mixer output, 3.2 -- 7.7 GHz
Dissipation @ 1.2V	52 mW 48 mW 63 mW	Receiver Transmitter LO generation

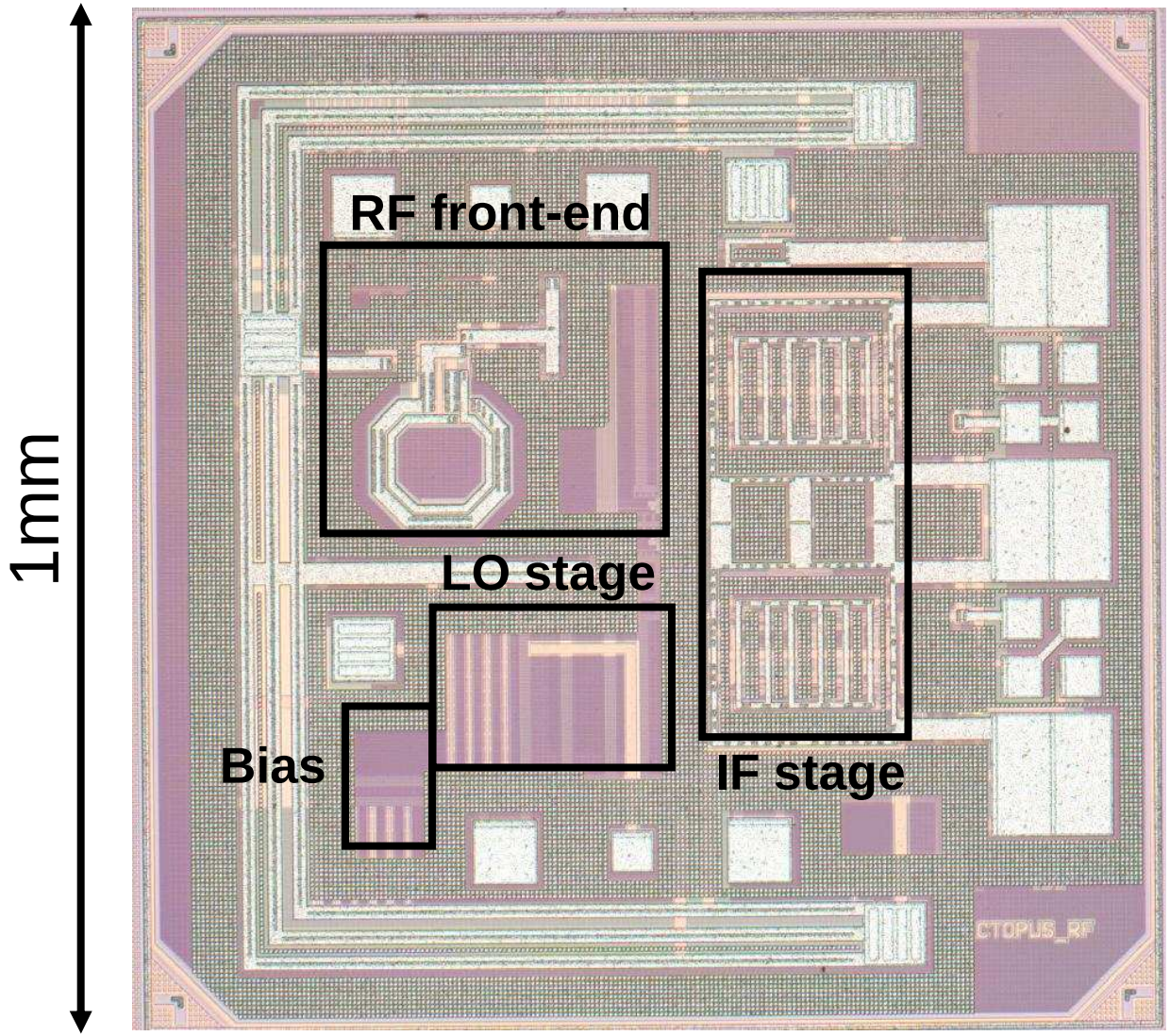
UWB transceiver in 65nm



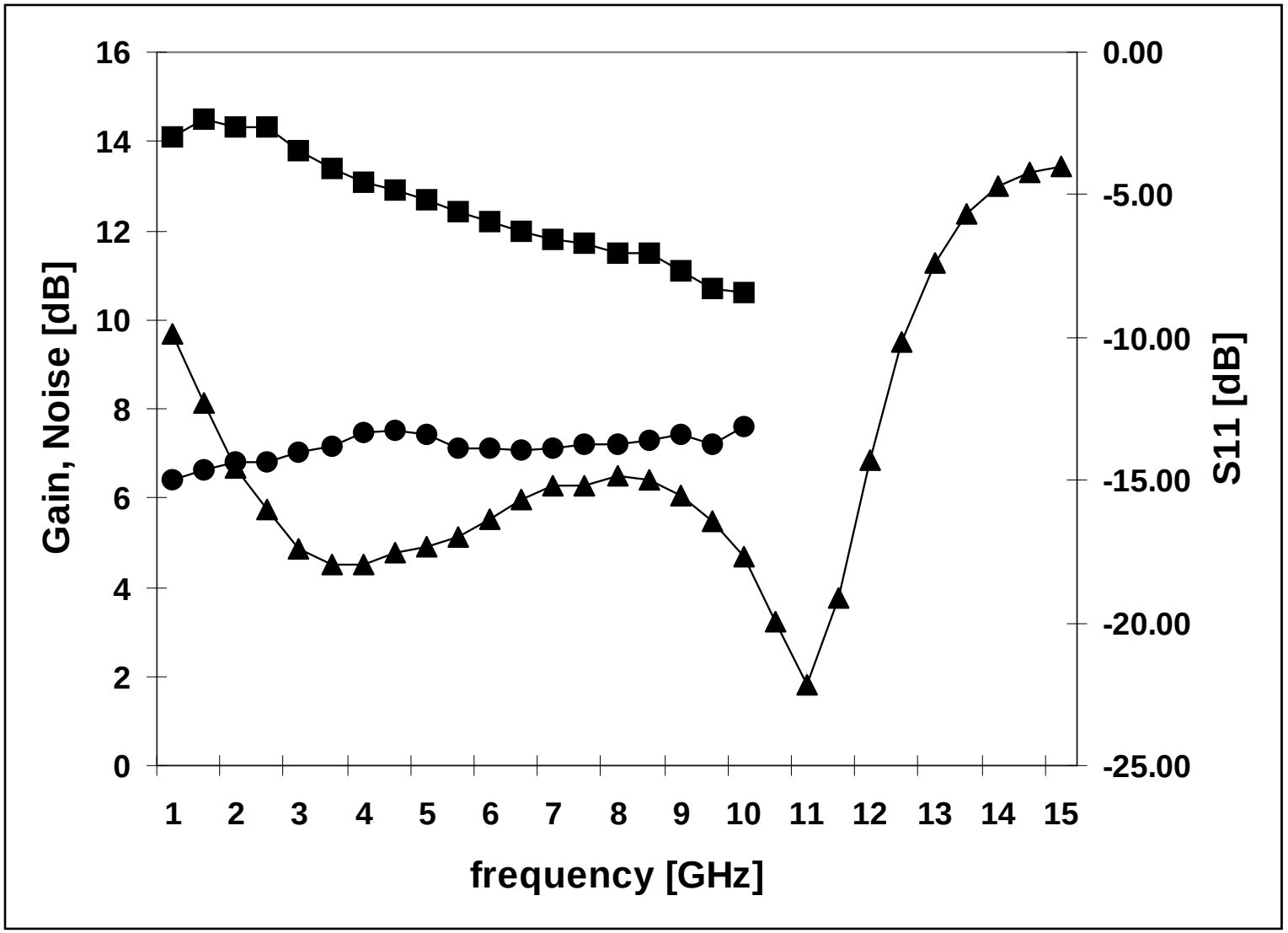
UWB transceiver in 65nm



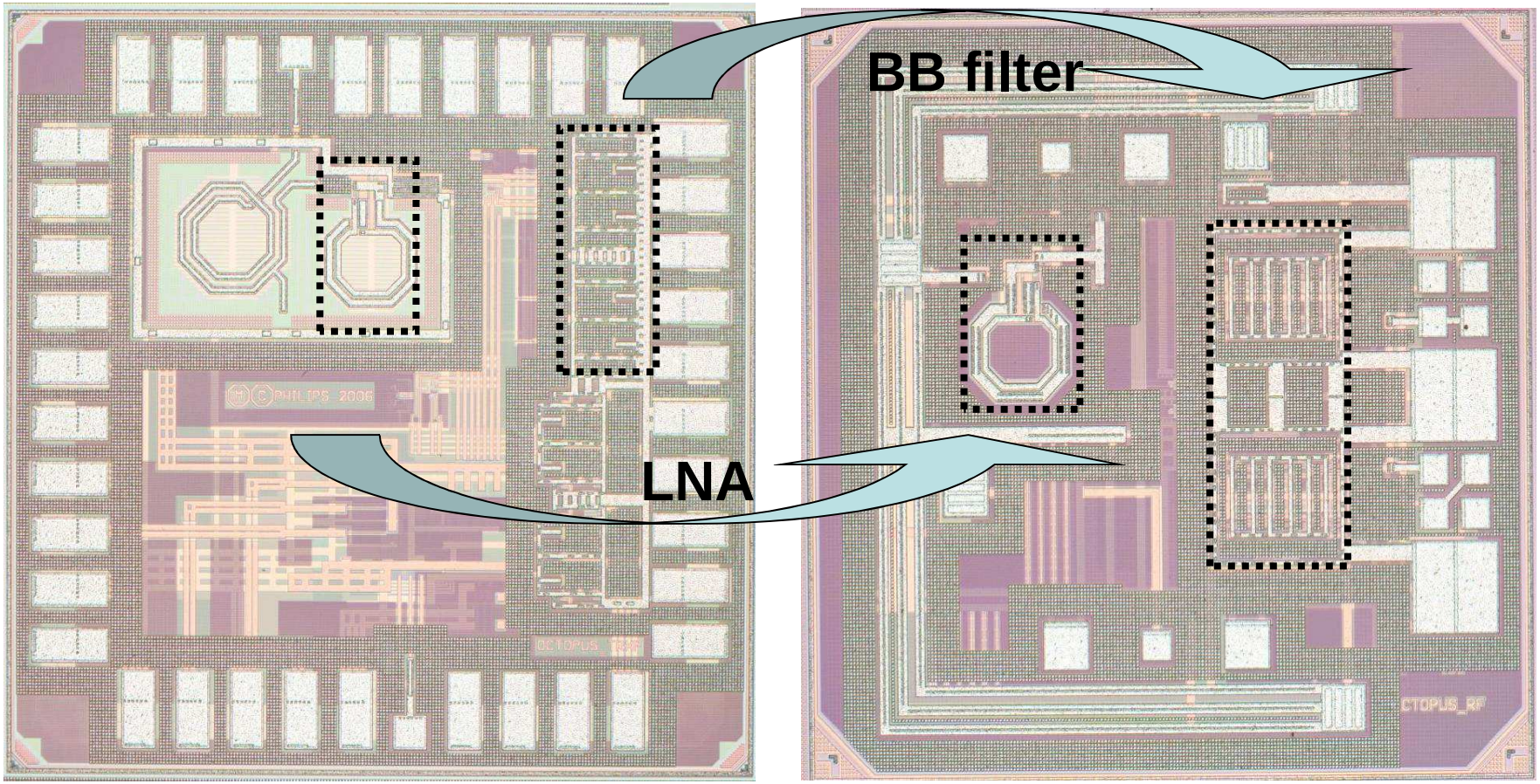
UWB receiver in 45nm



UWB receiver in 45nm



Comparison of 65nm-45nm RX



65nm LP CMOS

45nm LP CMOS

<u>Dies on scale</u>: analog does not necessarily scale!

Comparison of 65nm-45nm RX

Rx performance	65nm	45nm
Gain [dB]	20	14
3-dB BW [GHz]	7	10
NF [dB]	5.5	7
iIP3 [dB]	+5	0
iIP2 [dB]	+25	+20
Pdiss [mW]	52	90

Where do we stand nowadays?

- Wide Band CMOS design is possible
  - Convergence towards a receiver comprising wide band LNA, passive mixers and BB filtering
  - Additional tricks added to cope with interference are still needed
- Impressive f_T of naked device due to scaling does not tell the complete story
  - Layout influence becomes more and more dominant

Thank you for your attention!

Hope you learned something