Transistor Design Issues in Integrating Analog Functions with High Performance Digital CMOS

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Abstract

Pocket or halo designs used in high performance digital CMOS design can degrade analog device performance. A new understanding of this phenomenon is presented using device simulation. The effect of pocket implant parameters on the tradeoff between digital and analog performance is studied experimentally. Experimental data showing the beneficial effects of eliminating the pocket selectively from the drain end, on analog performance is also shown.

Introduction

MOSFET designs for high performance digital CMOS use pocket implants [1-4] for control of Vt rolloff to short Leff, thus resulting in high I_{drive} (and low Ioff) as well as reduced sensitivity of I_{drive} to gate length (L) variations. A high I_{drive} is critical for interconnect limited digital circuits [5] for which performance is proportional to $(C_{load}V_{cc}/I_{drive})^{-1}$. On the other hand, performance of analog circuits depends critically on achieving a high Early voltage, V_A. Experimental data shows that certain pocket processes result in devices with poor V_A, which increases slowly with L, thereby making them unsuitable for analog applications. We detail for the first time an understanding of why pocket designs can result in low V_A by analysis of device and circuit simulations, and correlation to experimental data. Careful design is therefore required for optimum digital (I_{drive}) and analog (V_A) performance. Experimental studies of the effects of pocket implant parameters on V_A and I_{drive} illustrate tradeoffs. An asymmetric solution with a pocket implant only at the source end [6] is shown to have improved V_A compared to the corresponding symmetric pocket case, consistent with the analysis presented. Only nMOS results are shown, but pMOS results are similar.

Experimental data

MOSFETs fabricated using a high performance logic process similar to that described in [1] are used to compare a pocket process optimized for high I_{drive} at L_g=0.13μm with an uniform channel design. The V_T implants for both designs are adjusted for equal I_{off} at minimum L. Fig. 1 compares their V_T vs. L and V_A vs. L characteristics. The pocket devices have relatively small V_T rolloff but low V_A. Drain induced barrier lowering (DIBL) measured as (Vt_{lin}-Vt_{sat}) vs. L for these devices is shown in Fig. 2. Large residual DIBL exists at long gate lengths for the pocket devices. The correlation between DIBL and V_A for the pocket devices is illustrated in Fig. 3.

Simulation results

Two dimensional simulations are presented to understand why pocket processes can result in poor V_A. Simplified doping density profile as a function of position in the channel for a 1 μm device with uniform channel doping and a pocket is shown in Fig. 4. The simulated conduction band edge location as a function of channel length (profiles from Fig. 4), is shown in Fig. 5 for two bias conditions namely: Vgs = Vt and Vgs = Vt + 0.2 V (Vds = 0.75 V). The simulated results of Fig. 5 show the presence of a barrier on the source and drain sides for the pocket device under both bias conditions. The uniform device has a barrier only on the source side. The drain side barrier modulation in the pocket device is shown in Fig. 6 as a function of drain bias. This modulation explains the experimentally observed residual DIBL at long channel lengths (Fig. 2). The conventional explanation of channel length modulation is not entirely valid in pocket devices as there is additional barrier modulation. Furthermore the presence of barriers above threshold at both the source and drain edges show the existence of a diffusion current component at both edges. These new observations have a significant impact on V_A as demonstrated by the circuit simulation results in Fig. 7. The addition of extra gate bias, controlled through the DIBL lowering coefficient α, demonstrates the strong influence DIBL has on V_A. A simulated example is shown in Fig. 8 of how three different pocket and channel designs, optimized to have the same minimum gate length, can have different V_A performance. For the device design simulated in Fig. 8 it is seen that higher dose pocket improves Vt rolloff but reduces V_A.

Process effects and process optimization

Several device design variables such as implant and anneal conditions can be modified to optimize I_{drive} and V_A. Experimentally observed effects of pocket dose and energy on V_A are shown in Fig. 9 and 10. The effect of pocket dose on V_A validates the simulation results (Fig. 8). Other process variables such as drain extender implant conditions and pocket implant angle were varied (using a 0.18 μm L CMOS flow) to map out digital and analog performance boundaries and the results of that experiment are shown in Fig. 11. From the process exploration, the tradeoff between I_{drive} and V_A for a given off current specification can be seen in Fig. 11. Fig. 11 also shows that there are pocket processes that improve V_A while keeping I_{drive} and off current fixed. Similarly, I_{drive} can be improved while keeping V_A fixed. The results demonstrate that understanding of device design is important to optimize digital and analog transistors. An alternate design strategy that does not have the drain side barrier modulation is an asymmetric device with the pocket implant performed only on the source side [6]. The experimental results from asymmetric devices are shown in Fig. 12 where it can be seen that these devices have lower DIBL and higher V_A when compared to symmetric devices with pockets on both source and drain side.

Conclusions

We have presented experimental data showing that certain pocket implants implemented for digital applications can have poor analog characteristics. Two dimensional device simulation shows that the degradation in V_A is due to the drain bias modulation of the barrier created by the heavily doped pocket near the drain. The effect of process variables on V_A is shown along with tradeoff between I_{drive} and V_A. Experimental data from an asymmetric device design is shown to improve V_A, consistent with the understanding developed.

References

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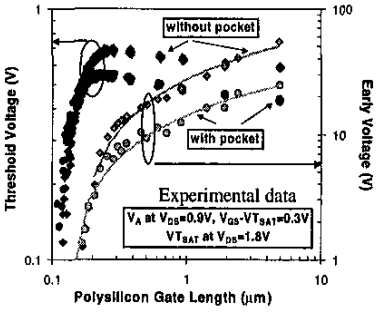

Fig. 1. Vt and V_A vs. L for devices with and without particular pockets. This pocket design improves Vt vs. L but degrades V_A vs. L.

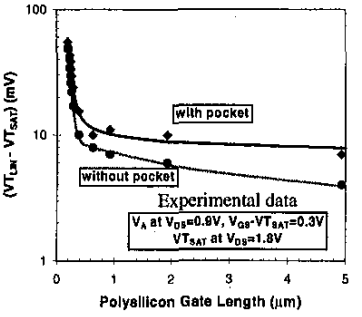

Fig. 2. Experimental DIBL (VT_{LIN}-VT_{SAT}) vs. L. A larger residual DIBL exists at long channel lengths for devices with the pocket design of Fig. 1.

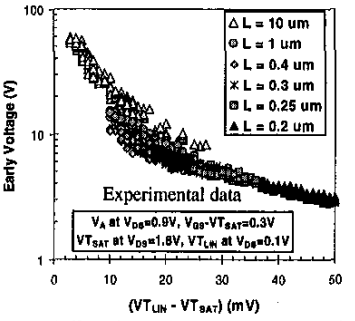

Fig. 3. Experimental correlation between DIBL and V_A for devices with a given pocket. The correlation stands across several gate lengths.

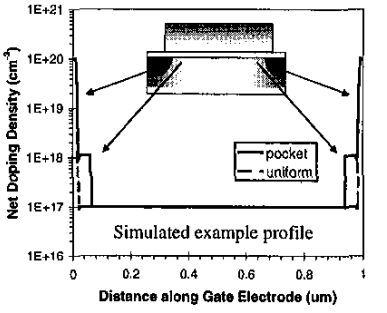

Fig. 4. Simplified doping density across the channel region for a device with and without pocket implants used for device simulations.

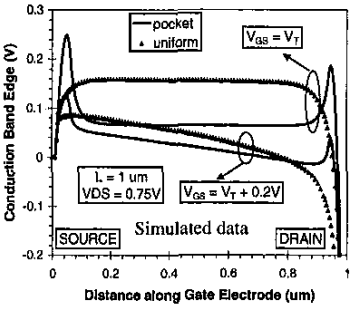

Fig. 5. Simulated band edge location as a function of position in the channel. Devices with pocket implants show barriers at both source and drain edges. Uniform device has only a source edge barrier.

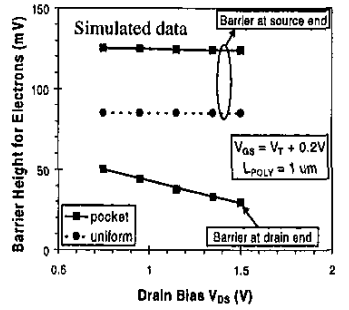

Fig. 6. Simulated barrier modulation as a function of drain bias. Pocket devices show drain edge barrier modulation leading to DIBL (Fig. 3).

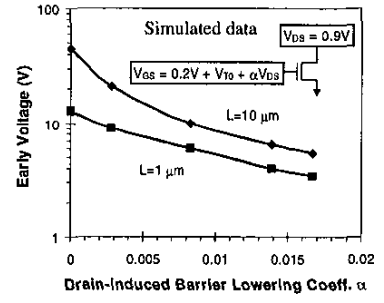

Fig. 7. Simulated effect of DIBL on V_A. Simulations performed using SPICE and inset circuit. Small DIBL reduces V_A considerably.

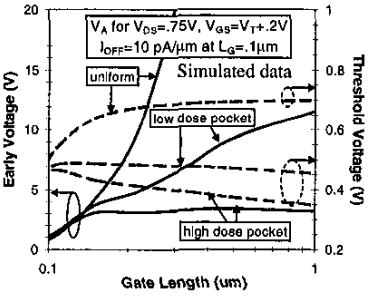

Fig. 8. Simulated effect of pocket dose on V_A while maintaining 10 pA/μm Ioff at Lg=0.1 μm. Higher pocket doses reduces V_A.

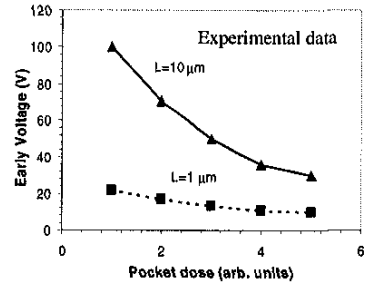

Fig. 9. Experimentally measured effect of pocket dose on V_A. Higher pocket dose reduces V_A.

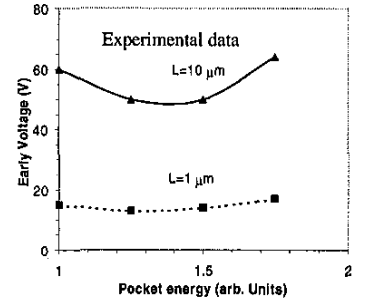

Fig. 10. Experimentally measured effect of pocket energy on V_A.

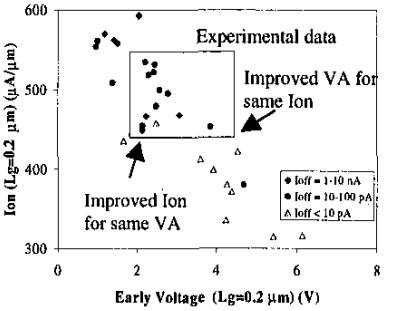

Fig. 11. Experimentally observed tradeoff between performance (Ion) and V_A while maintaining specified Ioff constraint. Some Ion penalty for higher V_A.

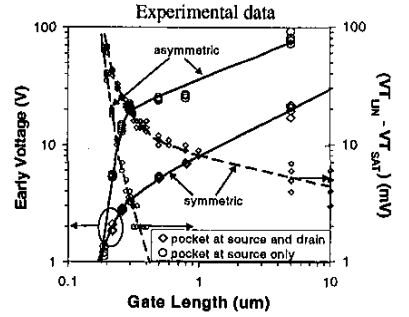

Fig. 12. Experimental comparison between symmetric and asymmetric devices. Asymmetric devices have reduced DIBL and improved V_A.