Accurate Modeling of Trench Isolation Induced Mechanical Stress effects on MOSFET Electrical Performance

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Abstract

A new approach is presented aiming at modeling mechanical stress effects which impact MOSFET electrical behavior. It shows successful in accounting for mobility variations experimentally evidenced on complex MOSFET geometries. The newly developed mobility model proves to be an efficient way to include mechanical stress effects into standard simulation models. We show that stress effects can and should be taken into account in the IC design phase in present and sub 90nm nodes CMOS generations.

Introduction

CMOS devices down scaling demands an increasing complexity in modeling to take into account new effects impacting MOSFET electrical behavior due to the ever increasing density of integration. Shallow Trench Isolation (STI) induced mechanical stress is the dominant source of mechanical stress variations in MOSFET channel following MOSFET geometry variations, such as Active Area (AA) size & shape, gate location inside AA, etc. It may account for more than ±15% mobility variations (see Figure 1).

Other authors have evidenced this phenomenon [1]. Better understanding has been strived for aiming at controlling and reducing the stress [2] [3].

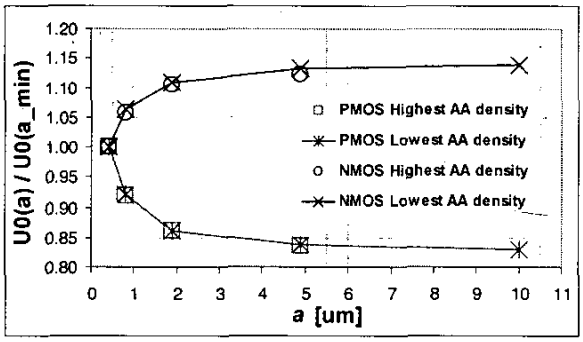

Figure 1. Measurement of low-field mobility variations versus AA size, showing opposite behavior according to MOSFET channel doping.

The originality of the present work is instead to get around its deleterious effects, and potentially take advantage of the phenomenon, by accurately accounting for stress effects in simulation models. The approach is based on mechanical simulations, test structures design and tests, performed on 0.12µm and 0.18µm CMOS technologies, to extract phenomenological laws to be implemented in simulation models delivered to designers.

Mechanical Simulations

Former work [4] allowed an estimation of stress evolution along the process flow. Based on ANSYS FEM simulation, we now focus on the STI contribution to in-plane stress variations according to MOSFET shape.

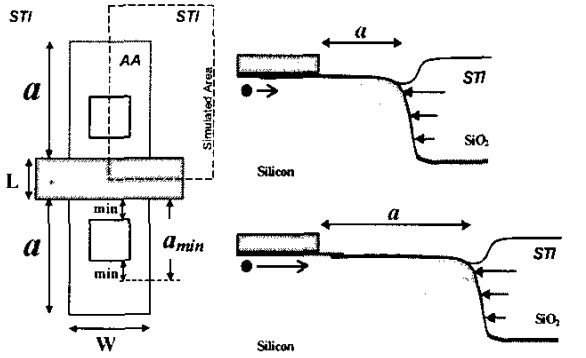

Figure 2. Standard shape MOSFET (rectangular AA and centered gate) planar & cross section views (a_{min}: minimum "a" including a single contact row).

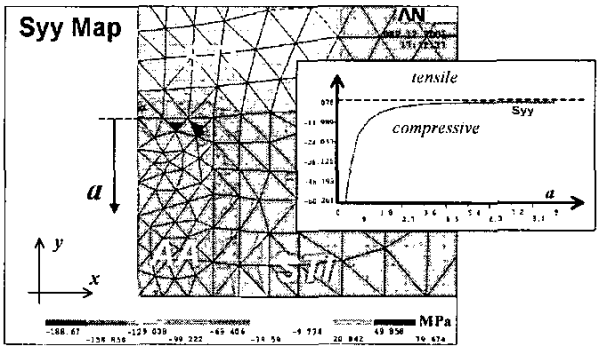

Figure 3. Mechanical simulation of Syy stress on the upper-right quarter of a rectangular AA (dashed frame area in Figure 2). Along "y" axis, compressive stress decreases when "a" increases.

Here the simulated process is limited to a 1000°C ramp down from a high temperature relaxed viscous state towards ambient state of the STI oxide. The geometrical model is limited to a two-material oxide/silicon pattern in 3D. Due to a difference in thermal expansion coefficient between silicon and silicon-oxide in the STI, a compressive state of stress develops as a peak at the AA-STI interface. The level of local compressive stress "Syy" attenuates as a function of distance to the STI edge "a" as shown in Figure 3, and according to the following model:

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$$Syy(a) = Syy(a_{min}) \cdot \left[1 + Vm_{Syy} \cdot \left(\frac{a - a_{min}}{a}\right)\right] \quad (1)$$

where an "a_{min}-MOSFET" is taken as a reference (see Figure 2) and "Vm_{Syy}" represents the maximum Syy(a) variation (i.e. when $a \rightarrow \infty$) with respect to Syy(a_{min}), as shown in Figure 4 and Figure 5.

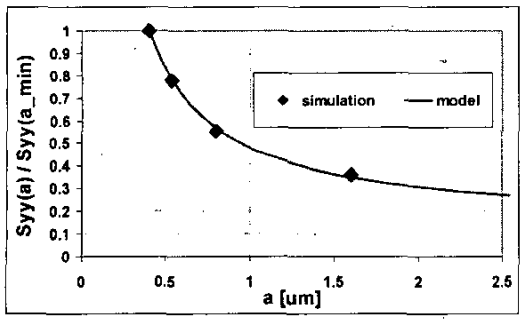

Figure 4. Evolution of simulated Syy stress at the center of the channel with respect to AA size.

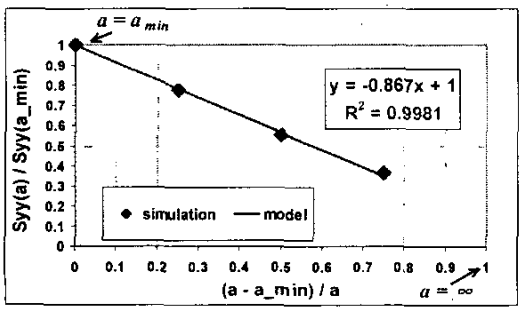

Figure 5. Simulated Syy stress and linear model fitting.

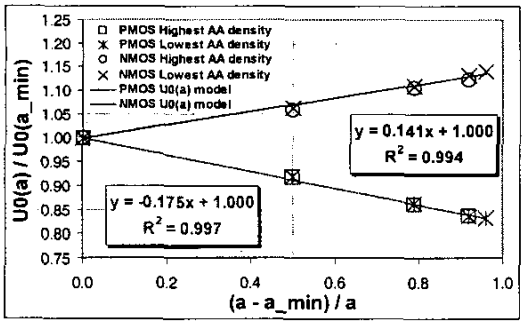

Figure 6. Measurement of low-field mobility variations, and linear model fitting, performed on NMOS and PMOS transistors of various sizes and densities.

Phenomenological Low-Field Mobility U0(a) Model

Assuming a linear relation between low-field mobility U0 and Syy variations, equation (1) form can be successfully used to model U0(a) too:

$$U0(a) = U0(a_{min}) \cdot \left[1 + Vm_{U0}(W,L) \cdot \left(\frac{a - a_{min}}{a}\right)\right] \quad (2)$$

$Vm_{U0}(W,L)$ is the maximum U0(a) variation with respect to U0(a_{min}), which is quite W-independent but is increasing for decreasing L (see Figure 7). Consequently, L and a_{min} down scaling in future advanced CMOS technologies may lead to even more pronounced stress effects on mobility. Figure 6 shows a very good fit between experimental data and model as well as no significant AA density effect.

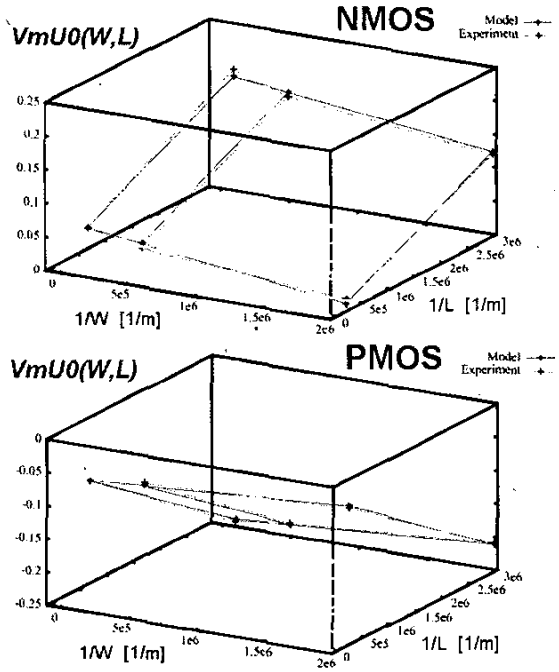

Figure 7. Experimental data and interpolation surfaces of maximum mobility variation $Vm_{U0}(W,L)$. Both NMOS and PMOS $Vm_{U0}(W,L)$ are rather W-independent and they increase with decreasing L.

Irregular MOSFET shapes

The aim is to extract an equivalent gate-to-STI distance "a_{eq}" from any irregular MOSFET shape, so that equation (2) model can be applied.

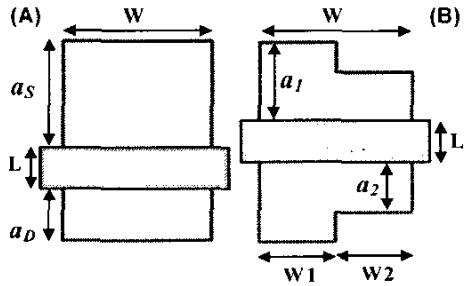

Figure 8. Asymmetric (A) and Composite (B) MOSFET shapes.

To address asymmetrical MOSFET shapes (i.e. $a_D \neq a_S$, see Figure 8) we isolate in (1) the respective source and drain side contributions to stress variation, to obtain the

expression for the equivalent distance to STI "a_{eq}", as follows:

$$\frac{Syy(a_{eq})}{Syy(a_{min})} = 1 + \frac{Vm_{Syy}}{2}\cdot\left(\frac{a_S - a_{min}}{a_S}\right) + \frac{Vm_{Syy}}{2}\cdot\left(\frac{a_D - a_{min}}{a_D}\right) \Rightarrow \frac{1}{a_{eq}} = \frac{1}{2a_S} + \frac{1}{2a_D} \quad (3)$$

❑ We assume the composite MOSFET in Figure 8 to behave as two independent shunt standard-shape MOSFETs. Taking into account the total mobility U0(a_{eq}), at any conduction regime, and equation (2), we obtain the following expression for the equivalent distance "a_{eq}",

$$U0(a_{eq}) = \frac{U0(a_1)\cdot W_1 + U0(a_2)\cdot W_2}{W} \Rightarrow \frac{1}{a_{eq}} = \frac{W_1}{W\cdot a_1} + \frac{W_2}{W\cdot a_2} \quad (4)$$

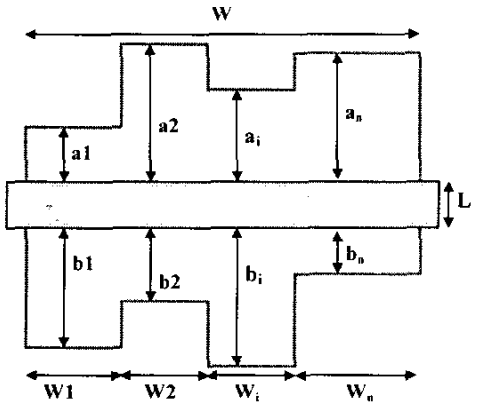

Figure 9. General shape MOSFET planar description.

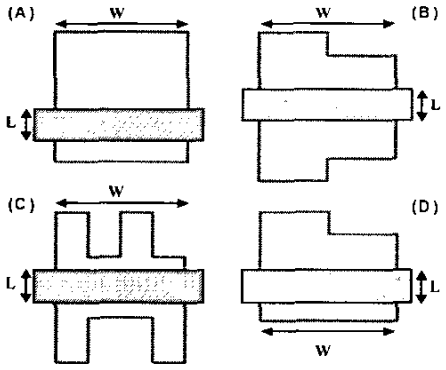

Figure 10. Tested irregular shape MOSFETs.

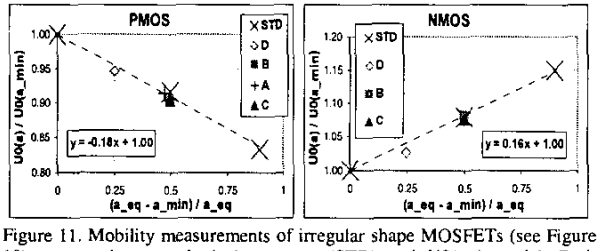

Figure 11. Mobility measurements of irregular shape MOSFETs (see Figure 10) compared to standard shape ones (STD) and U0(a_{eq}) model. Both standard and irregular shape MOSFET mobility variations can be described by the same model.

❑ The general MOSFET shape in Figure 9 can then be modeled by (2) replacing "a" by "a_{eq}", the latter being computed with the following expression, obtained from (3) and (4),

$$\frac{1}{a_{eq}} = \sum_{i=1}^{n}\frac{Wi}{W}\cdot\left(\frac{1}{2a_i} + \frac{1}{2b_i}\right) \quad (5)$$

The low-field mobility U0 of irregular shape MOSFETs in Figure 10 have been tested and compared to standard shape MOSFETs and to U0(a) model, by means of "a_{eq}" calculation. Figure 11 shows that both standard and irregular shape MOSFET mobility variations can be described by the same model: U0(a_{eq}) according to respectively (2) and (5).

STI Induced Stress versus Cobalt Silicide Stress

In the past, stress effects with respect to AA size have been attributed to Cobalt Silicide ($CoSi_2$) formation process on Drain/Source regions [5], and the need for lower stress $CoSi_2$ processes has been suggested.

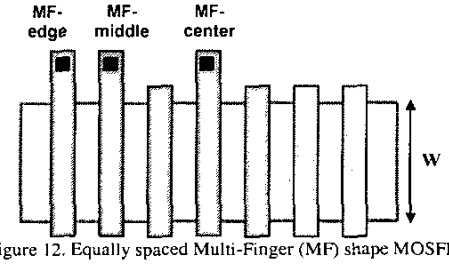

Figure 12. Equally spaced Multi-Finger (MF) shape MOSFETs.

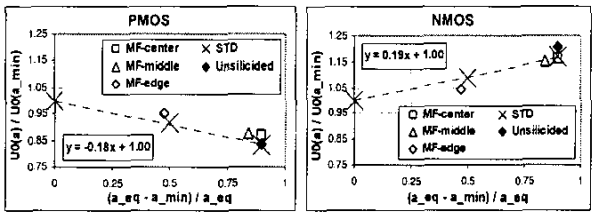

Figure 13. Mobility measurements on Unsilicided and Multi-Finger shape MOSFETs (see Figure 12) compared to standard shape ones (STD) and U0(a_{eq}) model. Both Unsilicided and Multi-Finger MOSFET mobility variations fairly match STD shape ones (with cobalt silicide) and U0(a_{eq}) model. Thus, stress effects of $CoSi_2$ formation process can be neglected.

To compare the importance of present-day $CoSi_2$ processes stress, versus STI induced one, an unsilicided version of the standard shape MOSFETs has been tested. Indeed, to check whether distance to STI "a_{eq}" or "Drain/Source" size is the relevant dimensional parameter for stress modeling, individual gate fingers in an equally spaced Multi-Finger structure with $CoSi_2$ (see Figure 12) have been tested too.

Identical mobility variations are observed on Unsilicided and on STD shape (with $CoSi_2$) MOSFETs (see Figure 13) and each finger of the Multi-Finger structure closely match STD shape MOSFETs and U0(aeq) model. Consequently, the stress effects of the used $CoSi_2$ formation process can be neglected.

SPICE Models Correction and Applications

BSIM3 simulation models, calibrated on "a_{min}-MOSFETs", have been modified adding (2) to account for mobility variations according to MOSFET geometry (see Figure 14 and Figure 15). Algorithms for "a_{eq}" computing have been added to Layout Extractor Tools, in 0.12µm and 0.18µm Design Kits (DK), in order to generate Spice-like circuit net lists including "a_{eq}" data.

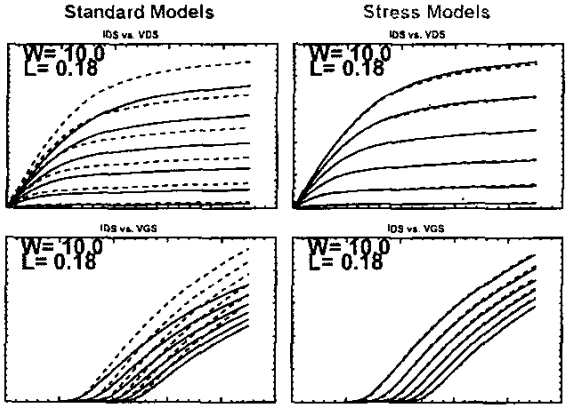

Figure 14. PMOS transistor stress modeling for a=10um: measurements (solid lines) versus simulations (dashed lines). Stress effects account leads to an accurate model.

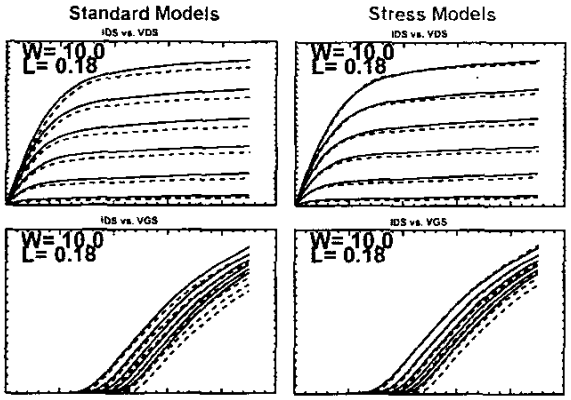

Figure 15. NMOS transistor stress modeling for a=10um: measurements (solid lines) versus simulations (dashed lines). Simulation model accuracy is significantly improved by stress effects account.

The modified DK has been used to optimize a special I/O circuit in 0.18µm CMOS technology (see Figure 16). In this I/O circuit version major functional characteristics rely on the "$U0_{NMOS}/U0_{PMOS}$ ratio" of output stage MOSFETs, presenting "a_{eq} >>10µm" (i.e. maximum U0 discrepancy with respect to standard simulation models). $U0_{NMOS}$ and $U0_{PMOS}$ discrepancy contribution to "$U0_{NMOS}/U0_{PMOS}$ ratio" are additive, leading to up to 30% simulation error.

The circuit has been fabricated and tested showing proper functionality. Simulation results of the fully functional I/O circuit, using the standard and our novel simulation model, are shown in Figure 17. The latter allows proper simulation, closely matching circuit measurements. The former predicts an overestimated Crossing Point and a wrong T_{RISE}/T_{FALL} ratio.

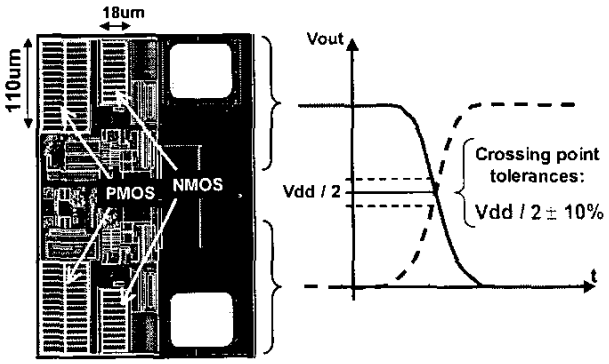

Figure 16. I/O Circuit and Crossing Point tolerances. Differential output signals Crossing Point and "T_{RISE} / T_{FALL} ratio" relies on "$U0_{NMOS}/U0_{PMOS}$ ratio" of output stage MOSFETs, presenting "a_{eq}>>10µm" (shunt multi-finger MOSFETs sharing a huge Active Area).

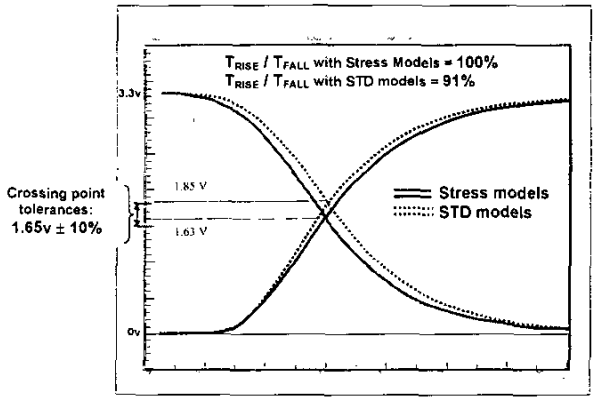

Figure 17. Fully functional I/O Circuit simulated with Standard Models (STD) and Stress Models. The latter allows proper simulation, which predictions closely match circuit measurements. The former predicts an overestimated Crossing Point and a wrong T_{RISE} / T_{FALL} ratio.

Conclusions

The excellent agreement between mechanical simulations, modeling and electrical results confirms that STI induced mechanical stress is the dominant mechanism for stress variation in the channel, resulting in carriers mobility modulation as a function of MOSFET geometry.

The presented mobility model proved to be an efficient way to modify standard MOSFET simulation models, so that STI induced mechanical stress effects can be taken into account in IC design. This early validation allows to extend its use to the 90nm node and below.

References

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