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Front End Manufacturing Technology

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Topics

- Transistor Performance Trends
- Transistor Scaling Challenges
- New Device Architectures
  - Advanced CMOS
  - Non-Classical CMOS
  - Memories
- New Front End Materials & Modules
- Lithographic Trends
- Summary

Moore's Law / Productivity

The definition of "Moore's Law" has come to refer to almost anything related to the semiconductor industry that when plotted on semi-log paper approximates a straight line.

– Gordon Moore, 1995

Transistor Performance Trend

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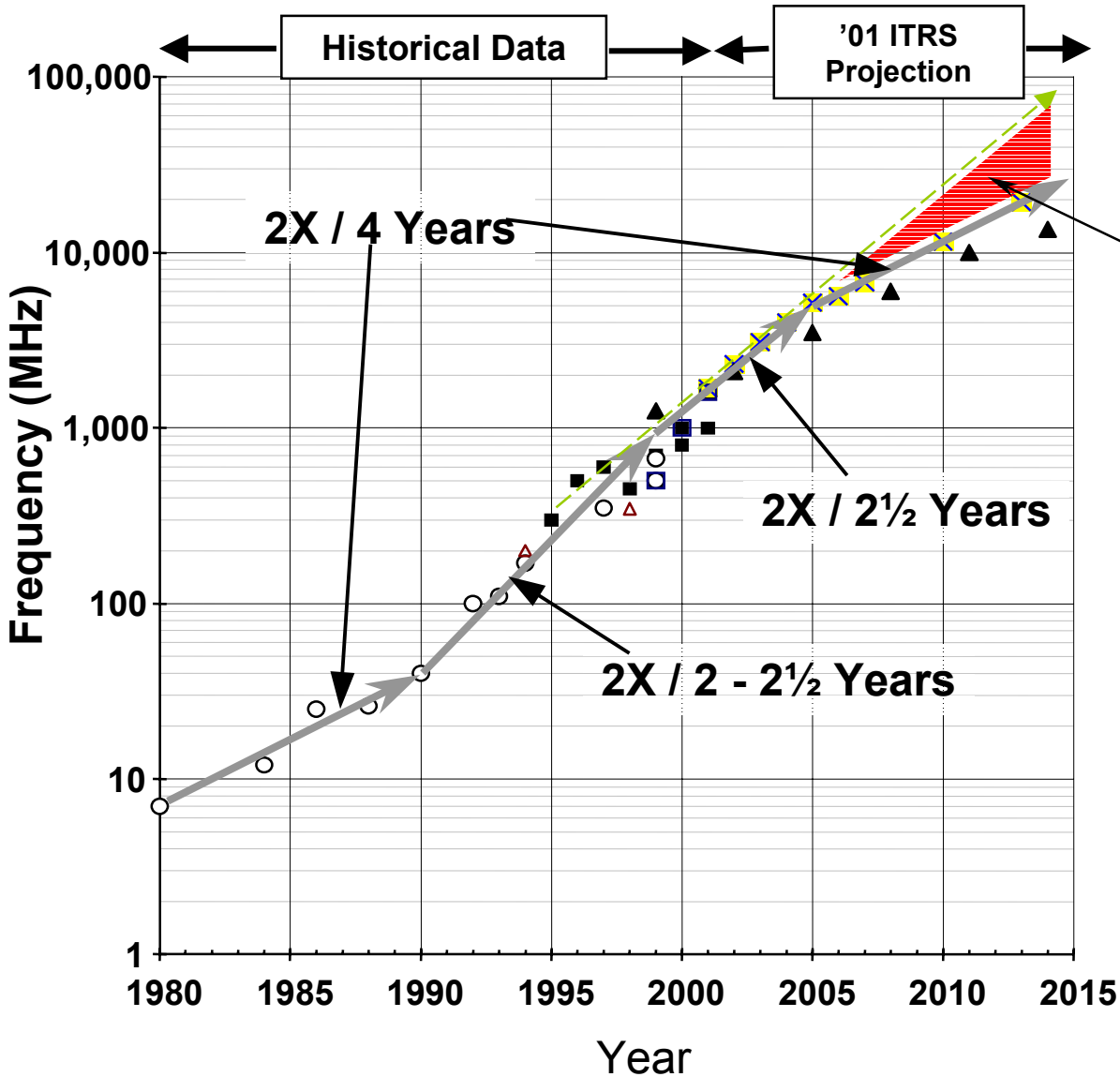

Innovation needed to maintain historical trend

MPU Clock Frequency Historical Trend:

Transistor scaling has contributed ~ 17-19%/year

Architectural Design innovation contributed additional ~ 13-21%/year

Sources: SEMATECH, 2001 ITRS ORTC

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  - Non-Classical CMOS
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Transistor Scaling Key Challenges

- Isolation: Minimum Pitch and SOI
- Gate Dielectric: Leakage vs Speed
- Gate Electrode: polySi vs Metal (Mid-gap vs Dual Work Function)
- Ultra-Shallow Junctions (USJ)
  - Low resistance contacts
  - Low resistance abrupt S/D extensions

2001 ITRS Scaling Projections

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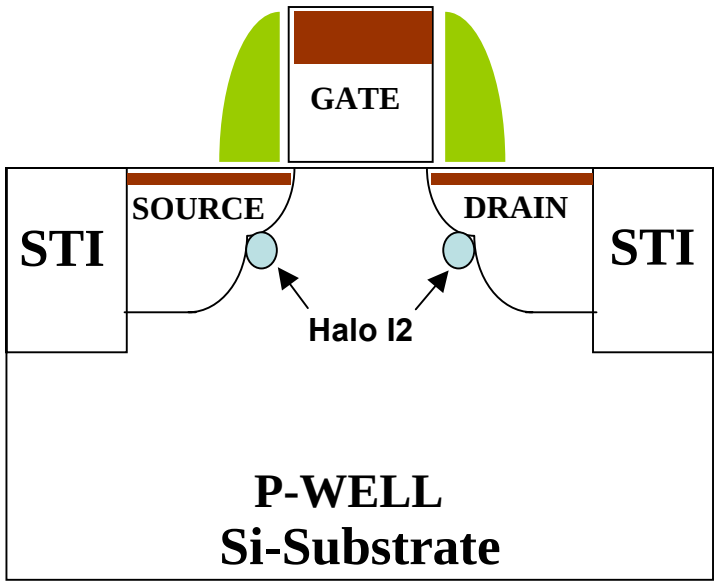
Technology Generation	130 nm	90 nm	65 nm	45 nm	32 nm	22 nm
Year Production	2001	2004	2007	2010	2013	2016
MPU Gate Length (nm)	*65*	*37*	*25*	*18*	*13*	*9*
DRAM (production)	512M	1G	4G	8G	32G	64G
DRAM chip (cm^2)	1.27	0.93	1.83	1.81	2.39	2.38
DRAM cost (μ ¢/bit)	7.7	2.7	0.96	0.34	0.12	0.042
Wafer Diameter (mm)	*300*	*300*	*300*	*300*	*450*	*450*
Logic M gates	97	193	386	773	1546	3092
Logic M gates/cm^2	69	138	276	552	1104	2209
Logic chip (cm^2)	1.4	1.4	1.4	1.4	1.4	1.4
Frequency (GHz)	1.7	3.9	6.7	11.5	19.3	28.7
μP cost (μ ¢/T)	97	34	12	4.3	1.5	0.54
Power/ Chip (W)	130	160	190	218	251	288
Power Supply MPU (V)	1.2	1.0	0.7	0.6	0.5	0.4
Levels of Metal	7	8	9	9-10	9-10	10
EOT (nm)	*1.3-1.6*	*0.9-1.4*	*0.6-1.1*	*0.5-0.8*	*0.4-0.6*	*0.4-0.5*
X_j at Channel (nm)	*27-45*	*15-25*	*10-17*	*7-12*	*5-9*	*4-6*

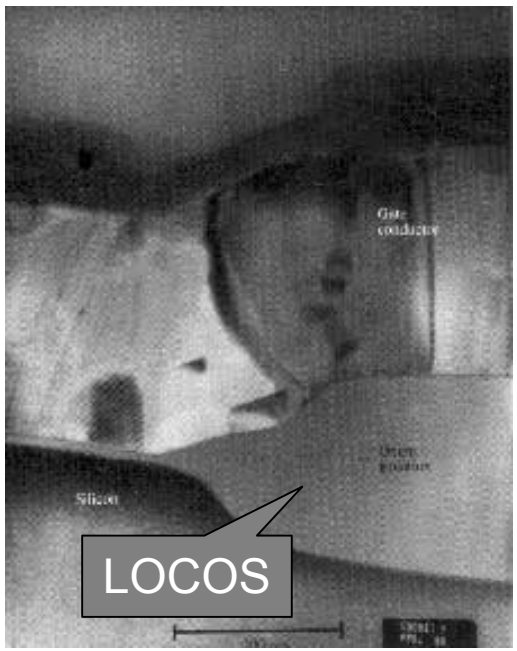
Device Scaling Issues: Beyond 65nm



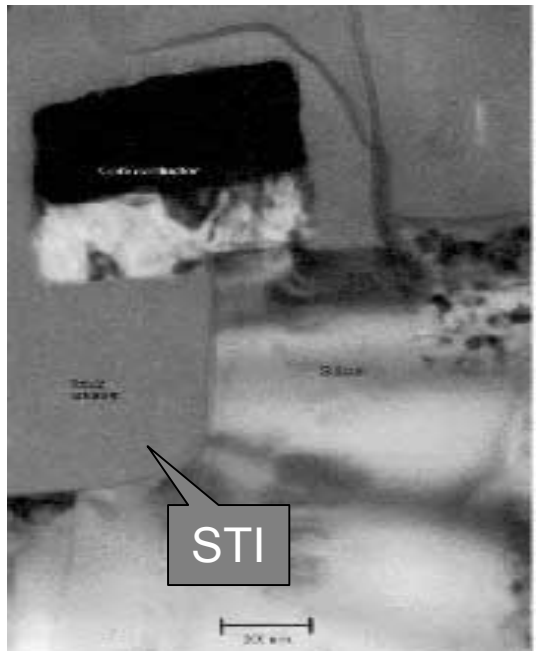
Threshold Voltage:
- $V_{DD} - V_T$ decreases
- Subthreshold Slope – kT/q
- CD Control

- Gate Stack
  - Tunneling => high I_{off}
  - Inversion Layer => EOT limit
  - PolySi Depletion => I_{on} reduced
  - Mobility degradation => I_{on} reduced
  - CD control
  - Reliability
- Source/Drain
  - Series Resistance => I_{on} reduced
  - Dopant Profile Control
    - TED suppression
    - USJ abrupt S/D extensions
    - Contacts to S/D
  - Tunneling
    - Drain to body & source to drain

Isolation Roadmap



IBM 4MB DRAM

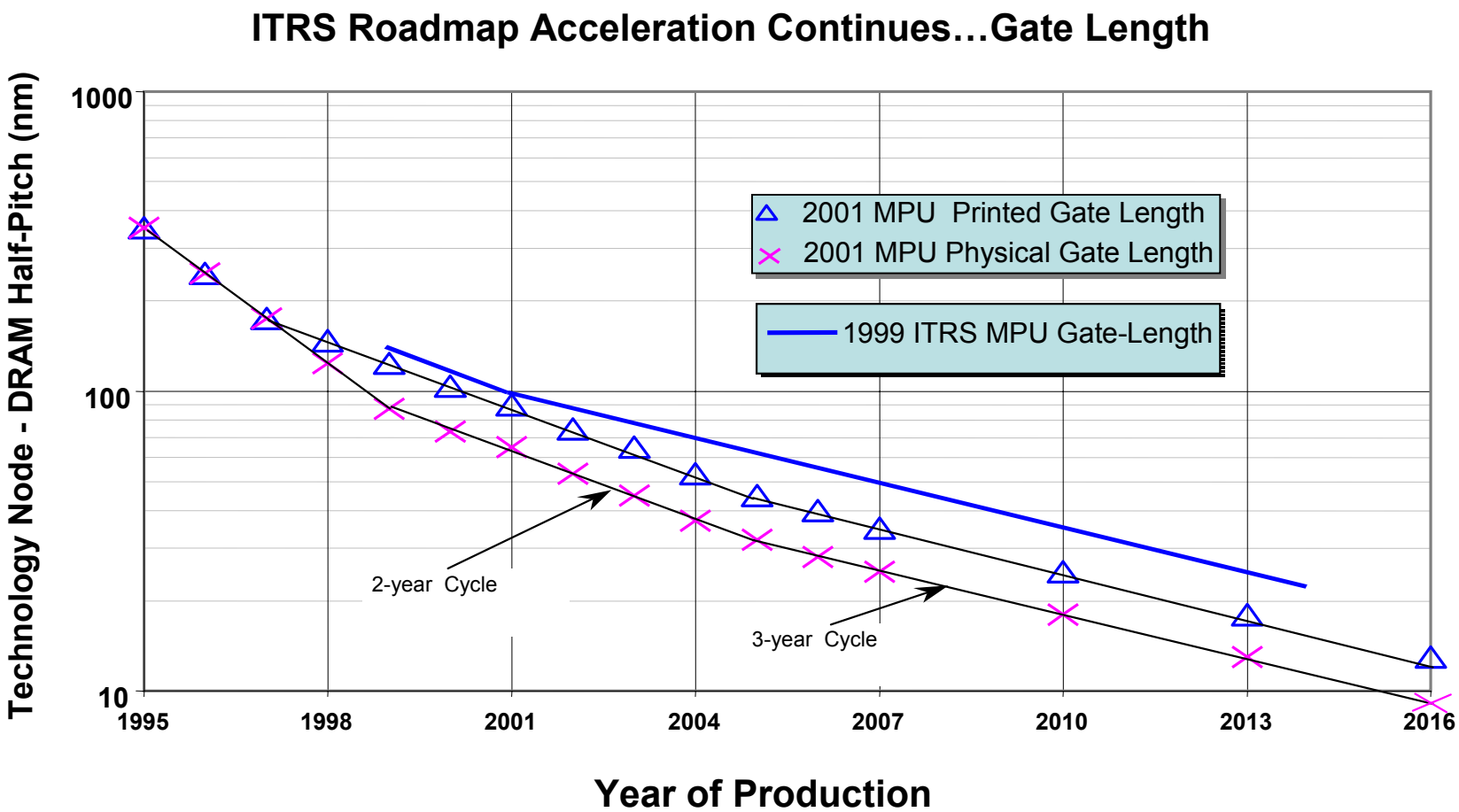


IBM 16MB DRAM

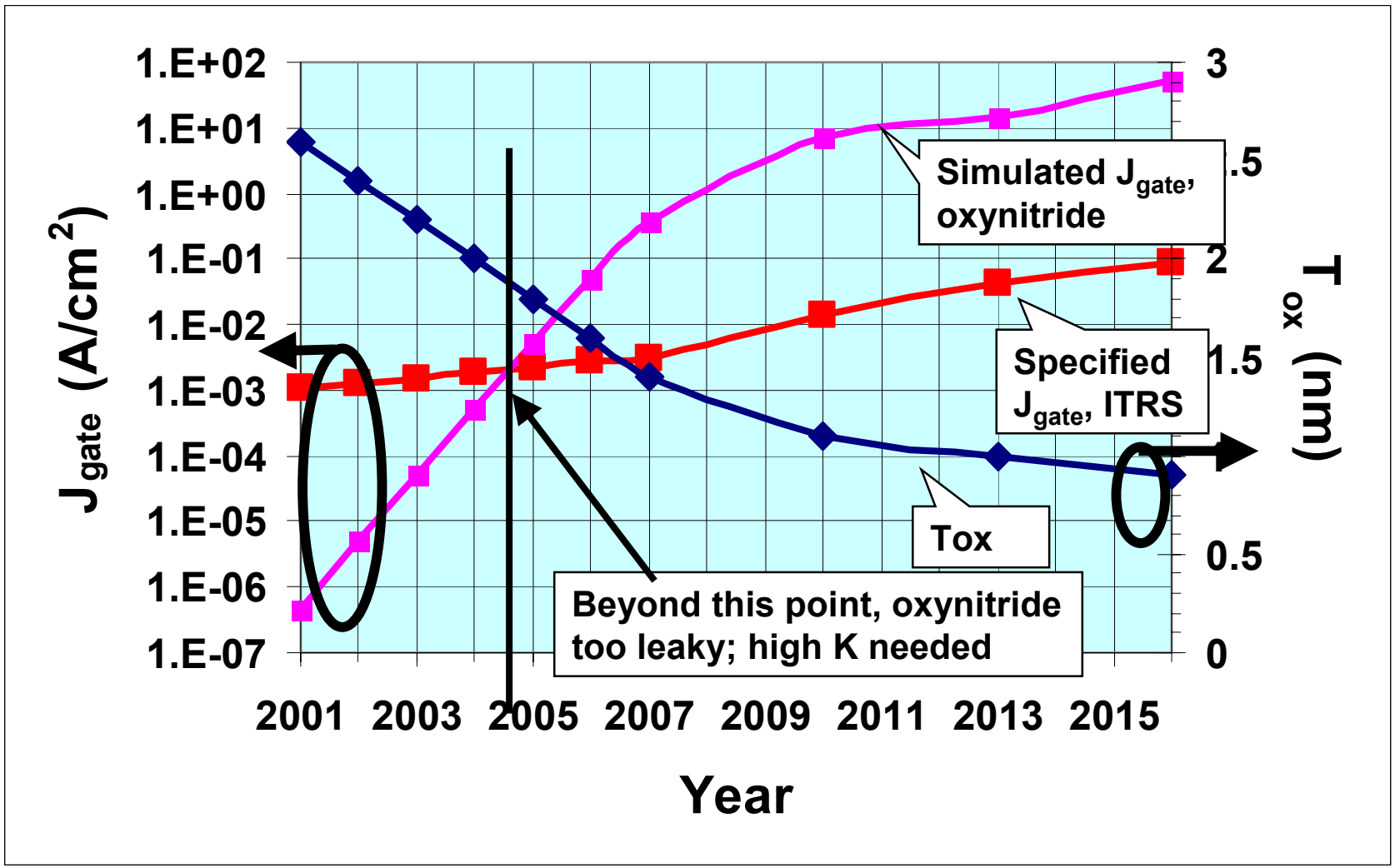
- STI induced to resolve LOCOS Bird's Beak
- Future device scaling and alternate structures such as Double Gate Logic devices and new member elements may lead to SOI only isolation.

LOCOS → Shallow Trench Isolation – STI → STI / SOI→ SOI only?

Gate Length Scaling: ITRS



2001 ITRS Projections Versus Simulations of Direct Tunneling Gate Leakage Current Density for Low Standby Power Logic



Simulations by C. Osburn, NCSU and ITRS

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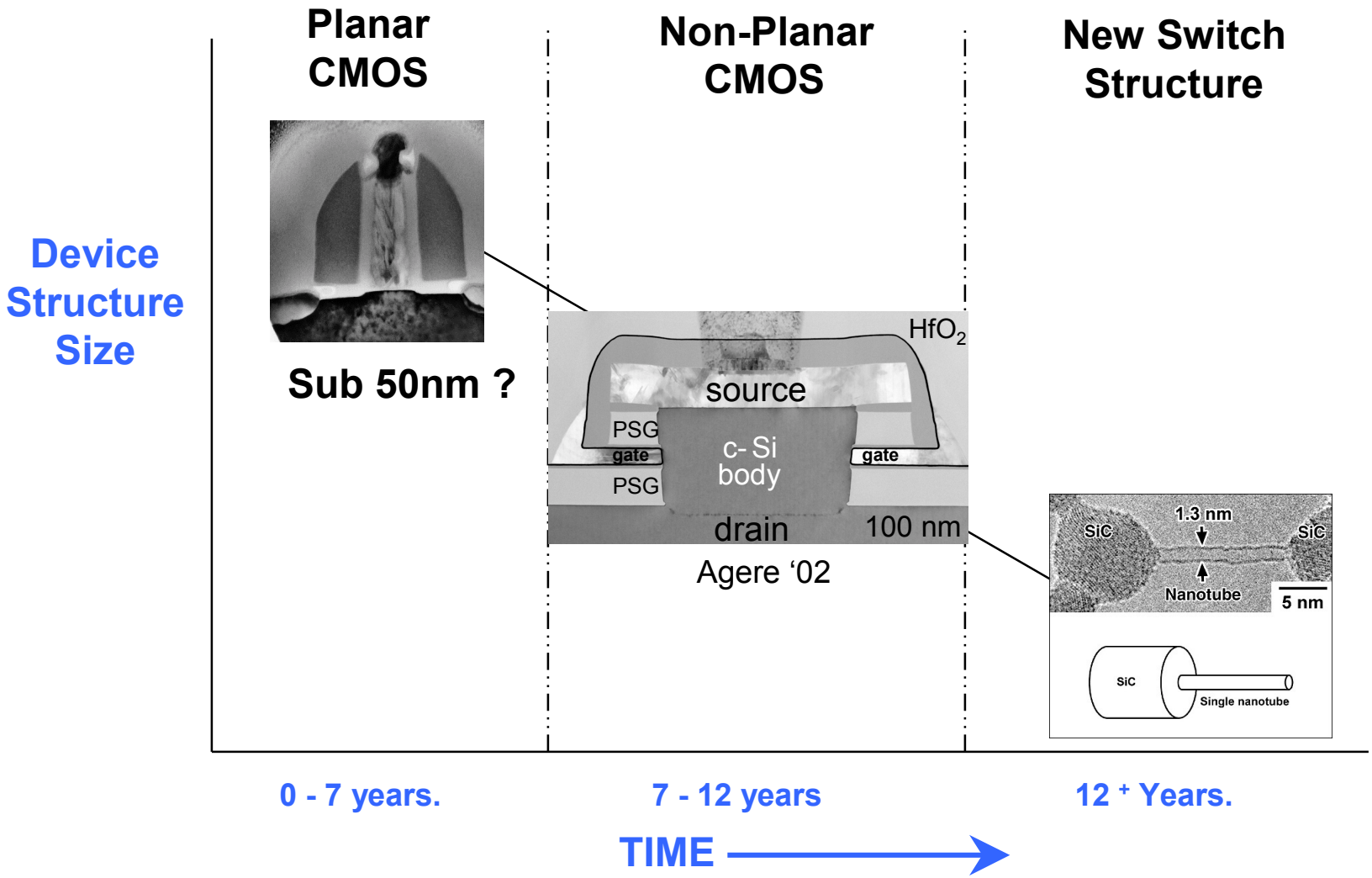
Limits of CMOS Scaling

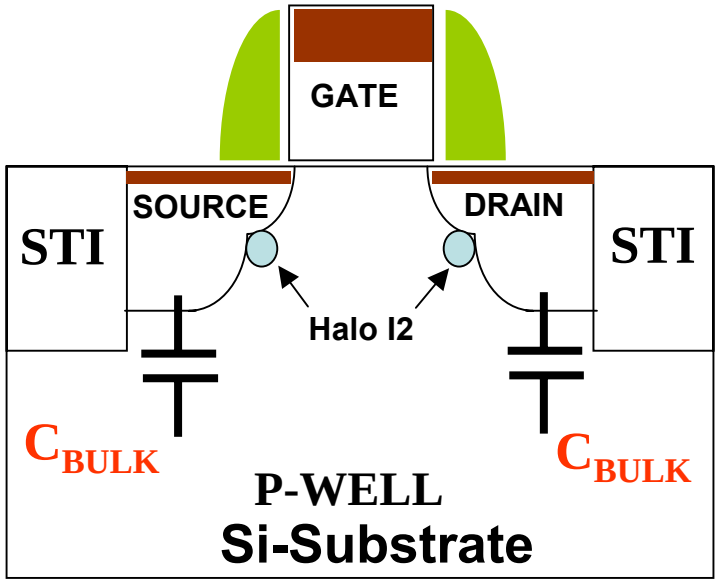


Device Evolution

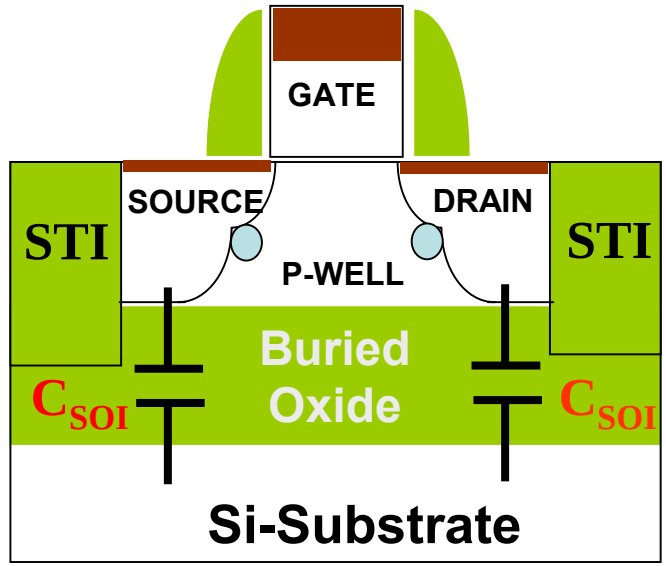
New Device Architectures

- SOI
  - Partially Depleted (PD)
  - Fully Depleted (FD): Ultra-Thin Body
- Double Gate Structures
  - FinFET
  - Tri, Pi Gate
  - DG-SOI
- Memory Innovations
  - FeRAM, MRAM, Ovonics, etc

SOI Device Structures



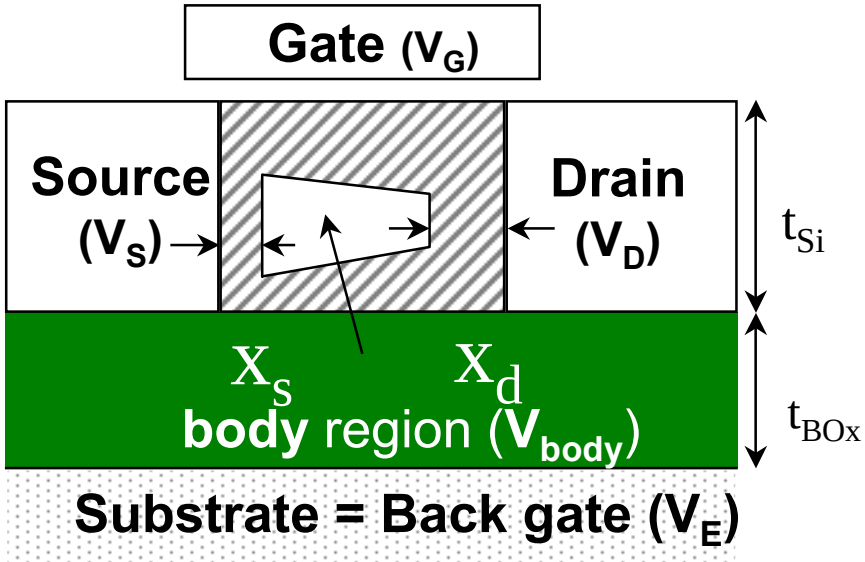
Bulk CMOS

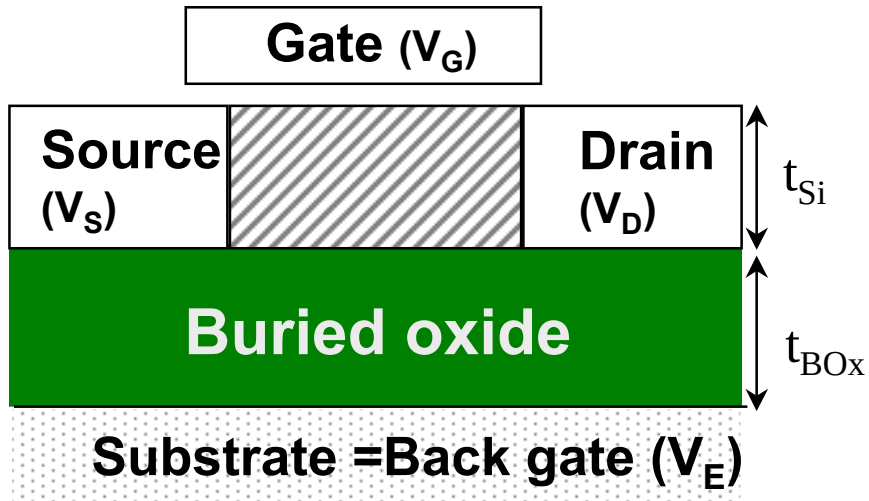


Partially Depleted CMOS

- Short Channel Effect controlled by channel doping/halo as in Bulk
- Reduced junction capacitances => faster speed, lower leakage
- Device design translation straight forward between Bulk and PD SOI
- Complete isolation between devices
- Rad-hard

Partially versus Fully Depleted





Partially depleted device

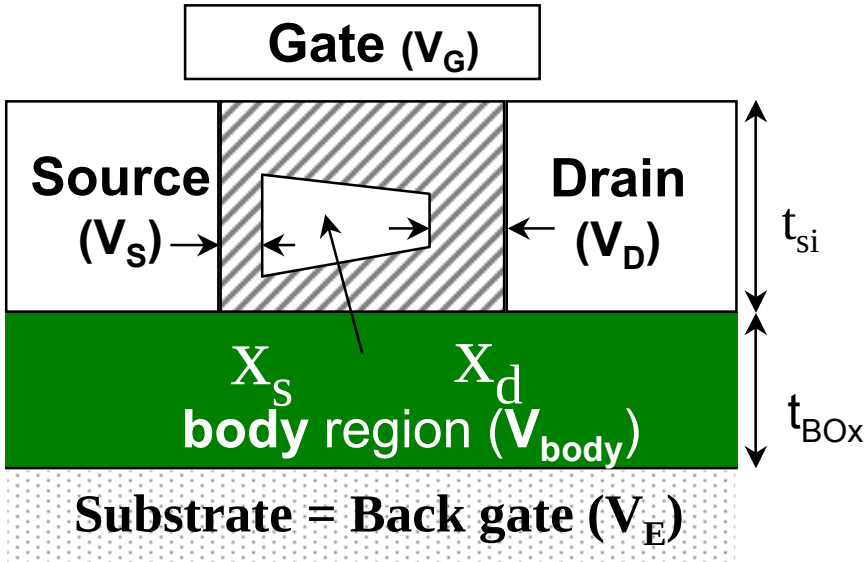
- Bulk bottom junction capacitances replaced by thick oxide capacitance
- Gate side lateral junction capacitance comparable to Bulk case. Can be smaller for PD in case of silicon film thinning

Fully depleted device

- Bulk bottom junction capacitances replaced by thick oxide capacitance
- Full depletion of silicon film suppress lateral junction capacitance
  - Speed improvement compared to PD
  - Smaller power consumption

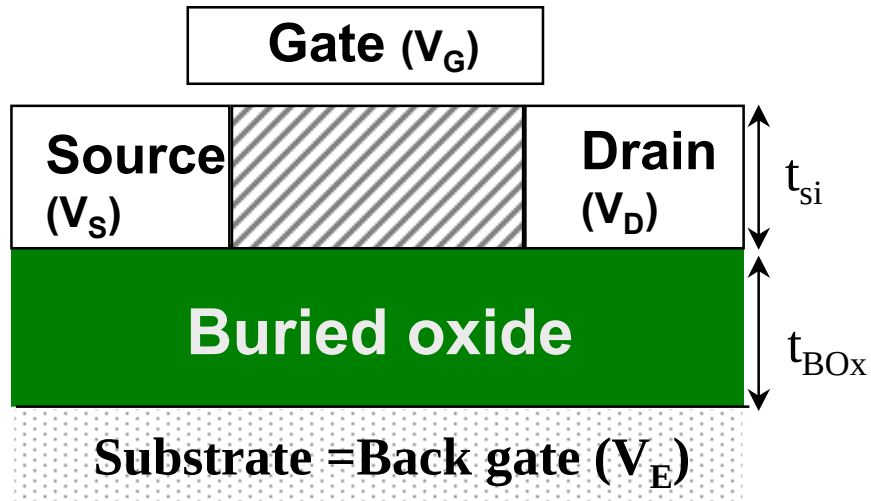
Courtesy of Olivier Faynot, LETI

Partially versus Fully Depleted



Partially depleted device

- 4 or 5 nodes
- Front and back gate decoupled
  - internal floating body node
- Floating-Body effects
- V_T=f (V_{body}) independent of V_E

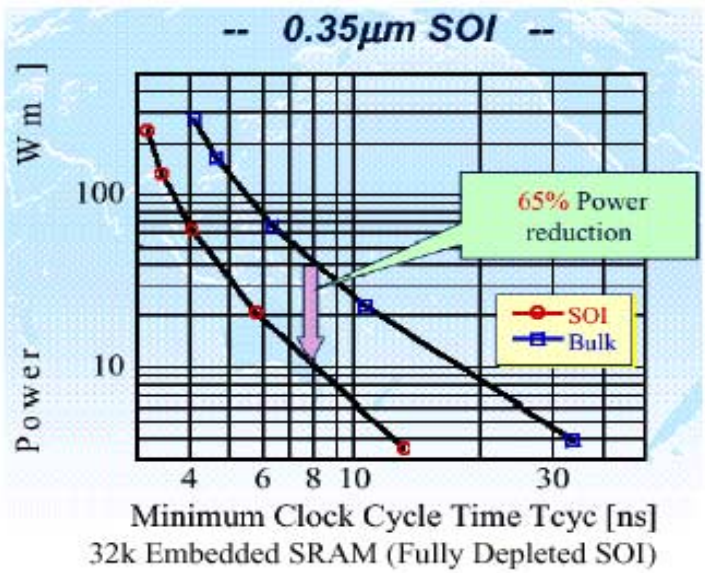


Fully depleted device

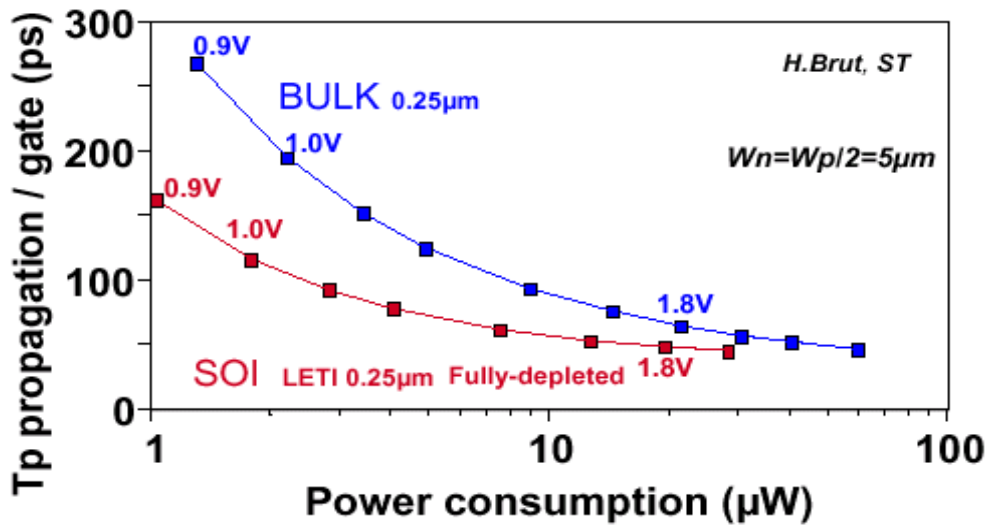
- 4 nodes
- t_{si}<40nm (for deep sub-µm MOS)
- No neutral floating region
  - independent of 'body' voltage
  - subthreshold swing=60mV/decade
- Front-Back interface coupling
  - V_T= f (V_E)

Courtesy of Olivier Faynot, LETI

SOI: Power Reduction



Ichigawa & al OKI VLSI Research Center . Sept 2000



Merits of Device Scaling <50nm Options

	Strengths	Weaknesses
Standard FD device	- Small parasitic capacitances - Simpler FD architecture	- Scalability: Ultra-thin film
Ground Plane	- Reduced SCE - Relaxed constraint on Tsi	- Parasitic capacitances increase - Subthreshold swing increase
Partial Ground Plane	- Reduced SCE - Relaxed constraint on Tsi	- Parasitic capacitances increase
Double Gate	- Best case for SCE control - Relaxed constraint on Tsi	- Fabrication very difficult - Parasitic elements?

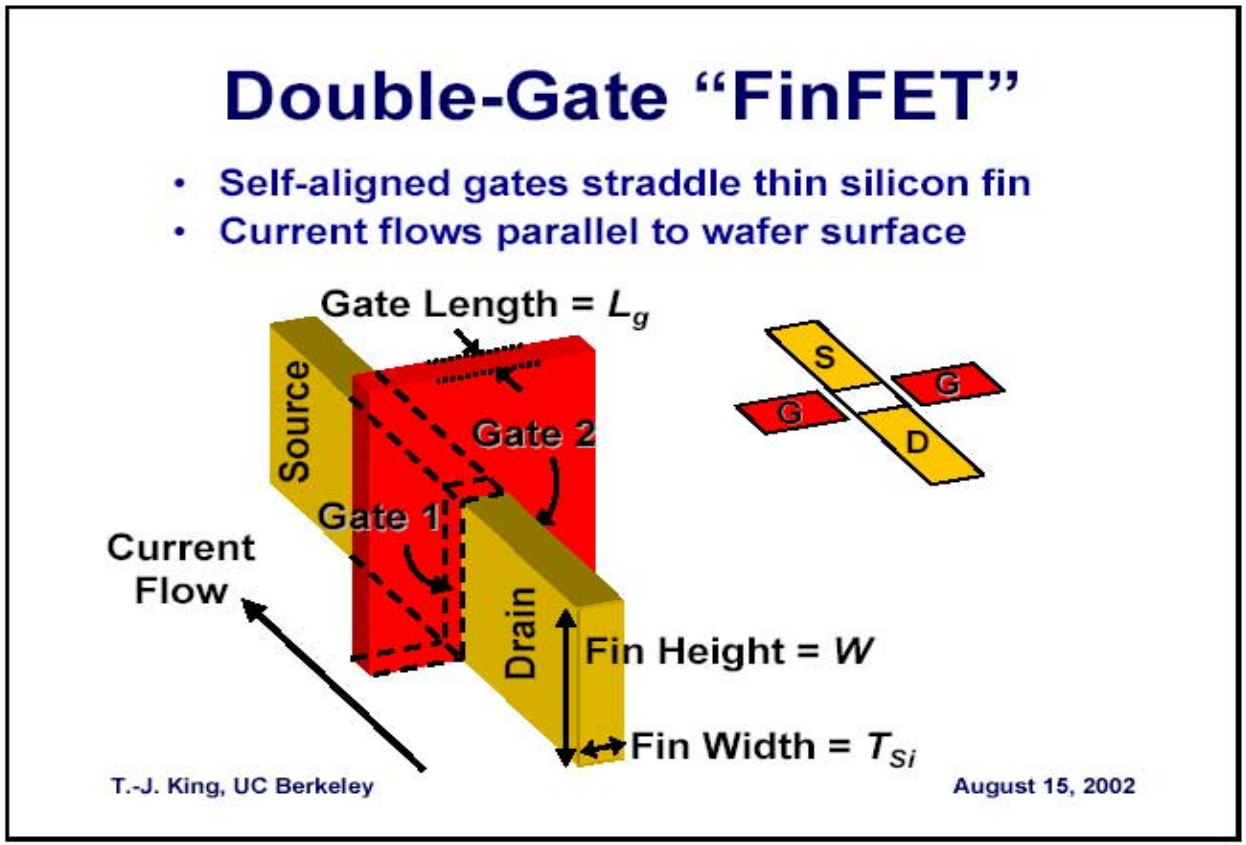
SOI Fabrication/Process Issues

- SOI is ~1.5 – 3x over bulk wafer pricing
- Etch Pit Density, typically ~600-1000/cm^2
- PD and to lesser extent FD have floating body effects which must be comprehended
- FD requires Silicon body thickness control less than ~0.2 - 0.4x of Lg or for example 18nm Lg, t_{si}~36 - 72A for 45nm node

New Device Architectures

- SOI
  - Partially Depleted (PD)
  - Fully Depleted (FD): Ultra-Thin Body
- Double Gate Structures
  - FinFET
  - Tri, Pi Gate
  - DG-SOI
- Memory Innovations
  - FeRAM, MRAM, Ovonics, etc

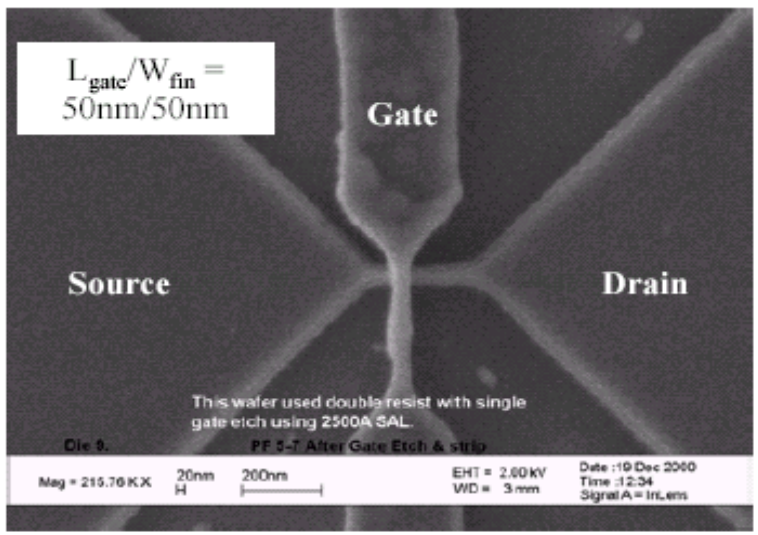
Double Gate Structures: FinFET



- **Fin width must be less than 2/3 x L_g**
  - Formation of narrow fin is primary challenge
    - sub-lithographic process needed

Double Gate Structures: FinFET Gate

50 nm FinFET Plan-View SEM



Remaining steps:

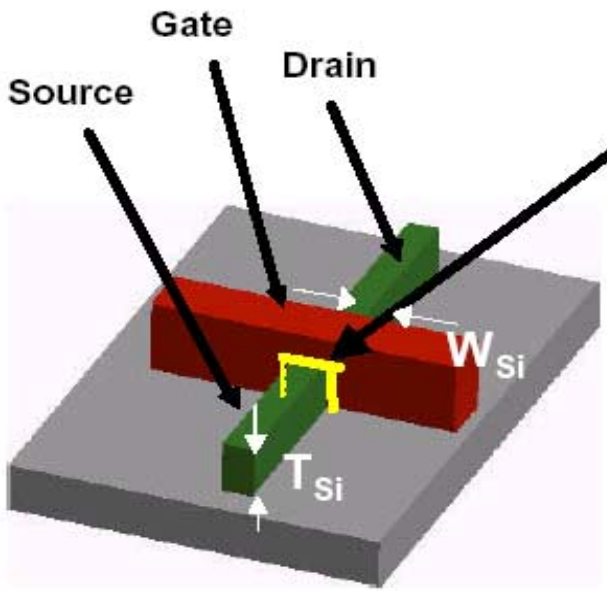
- Spacer formation
- (optional: selective Ge deposition)
- S/D ion implantation
- Thermal annealing
- LTO passivation
- Pad lithography & etch
- FGA (450°C)

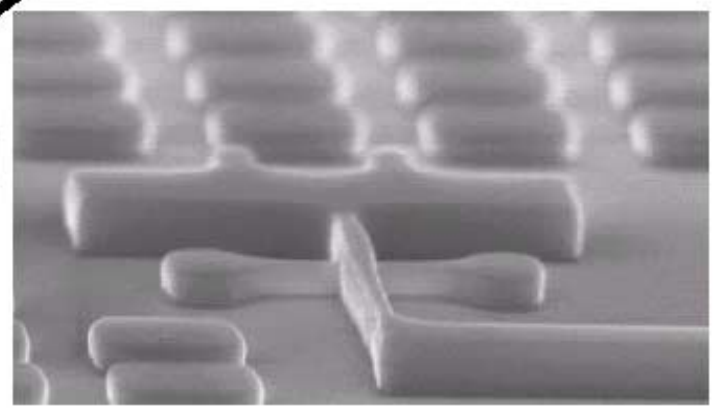
T.-J. King, UC Berkeley

August 15, 2002

Double Gate Structures: Tri-Gate

Tri-Gate DST



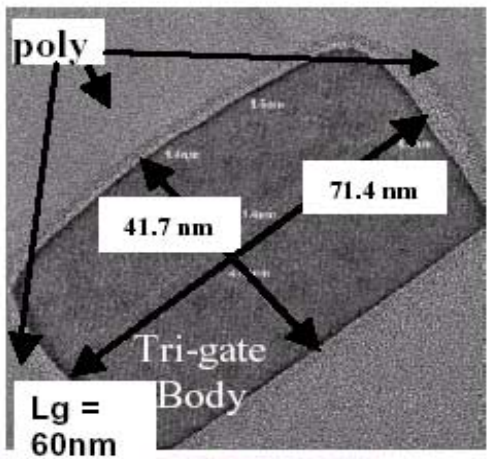


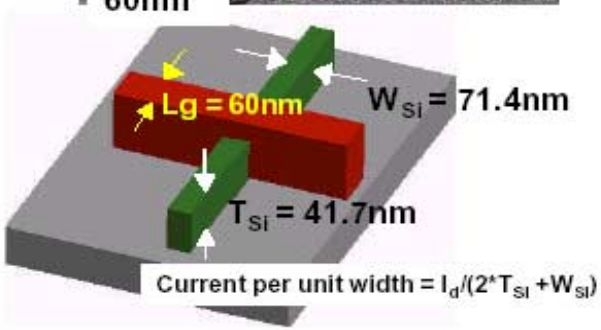
- Taller T_{Si} than single-gate; shorter T_{Si} than double-gate
- Wider W_{Si} than double-gate

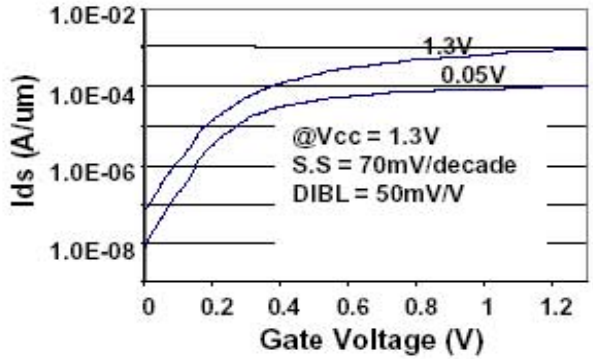
SSDM 2002, Nagoya, Japan

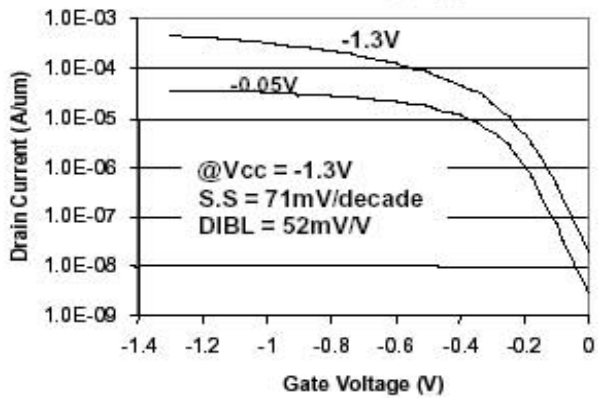
Double Gate Structures: Tri-Gate

Tri-gate DST Relaxes Si Body Dimensions









- Tri-gate relaxes Si body dimensions: 2.3X thicker T_{Si} than single-gate DST, and ~2X wider W_{Si} than double-gate FINFET

DG Fabrication/Process Issues

- **Moat etch**
  - Defines vertical gates
  - Etch and gate dielectric interaction on vertical gate structures
- **Gate dielectric (including high-K integration)**
  - Integrity, mobility, manufacturability
- **Gate materials and etch**
  - Depletion issues, hence Metal gate
- **Junction and Contact**
  - Ion Implant, PLAD, SEG
- **Ground plane design**
  - Implant through thin BOx

Options Below 50nm

	Doping	Mobility	Silicon film	Parasitic cap	Perf
BULK	10^{18}-10^{19}	Low	/	-	Ref. **o**
PD	10^{18}-10^{19}	Low	50-150nm	+	High +
FD & N^+ Poly	10^{18}-10^{19}	Low	5-15nm	++	Very High ++
GP, PGP, DG & N^+ Poly	10^{18}-10^{19}	Low	10-20nm	+	High +
DG & N^+ /P^+ Poly	10^{17}-10^{18}	Medium	10-20nm	++	High ++
FD & Metal gate	10^{15}-10^{16}	High	5-15nm	++	Very High +++
GP, PGP & Metal gate	10^{15}-10^{16}	High	10-20nm	+	High ++
DG & Metal gate	10^{15}-10^{16}	High	15-30nm	++	Very High +++

New Device Architectures

- SOI
  - Partially Depleted (PD)
  - Fully Depleted (FD): Ultra-Thin Body
- Double Gate Structures
  - FinFET
  - Tri, Pi Gate
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Memory Technologies

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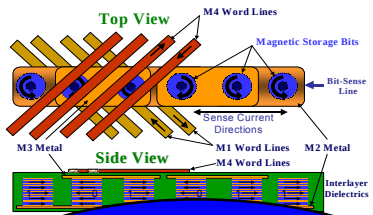
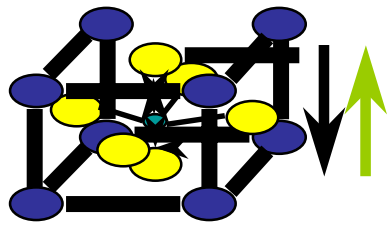
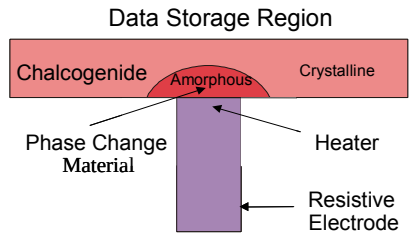
MRAM



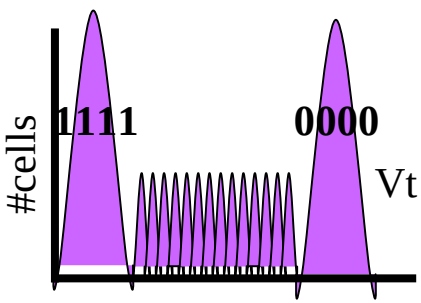
FERAM



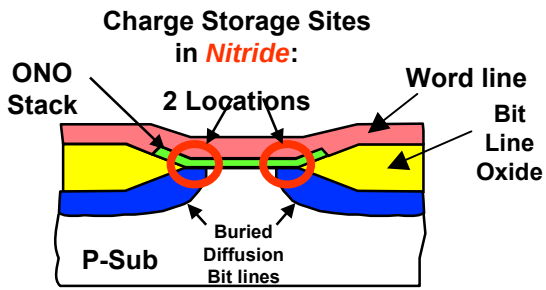
OUM



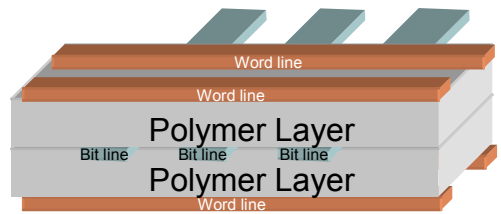
ETOX®-4bpc



NROM



Polymer

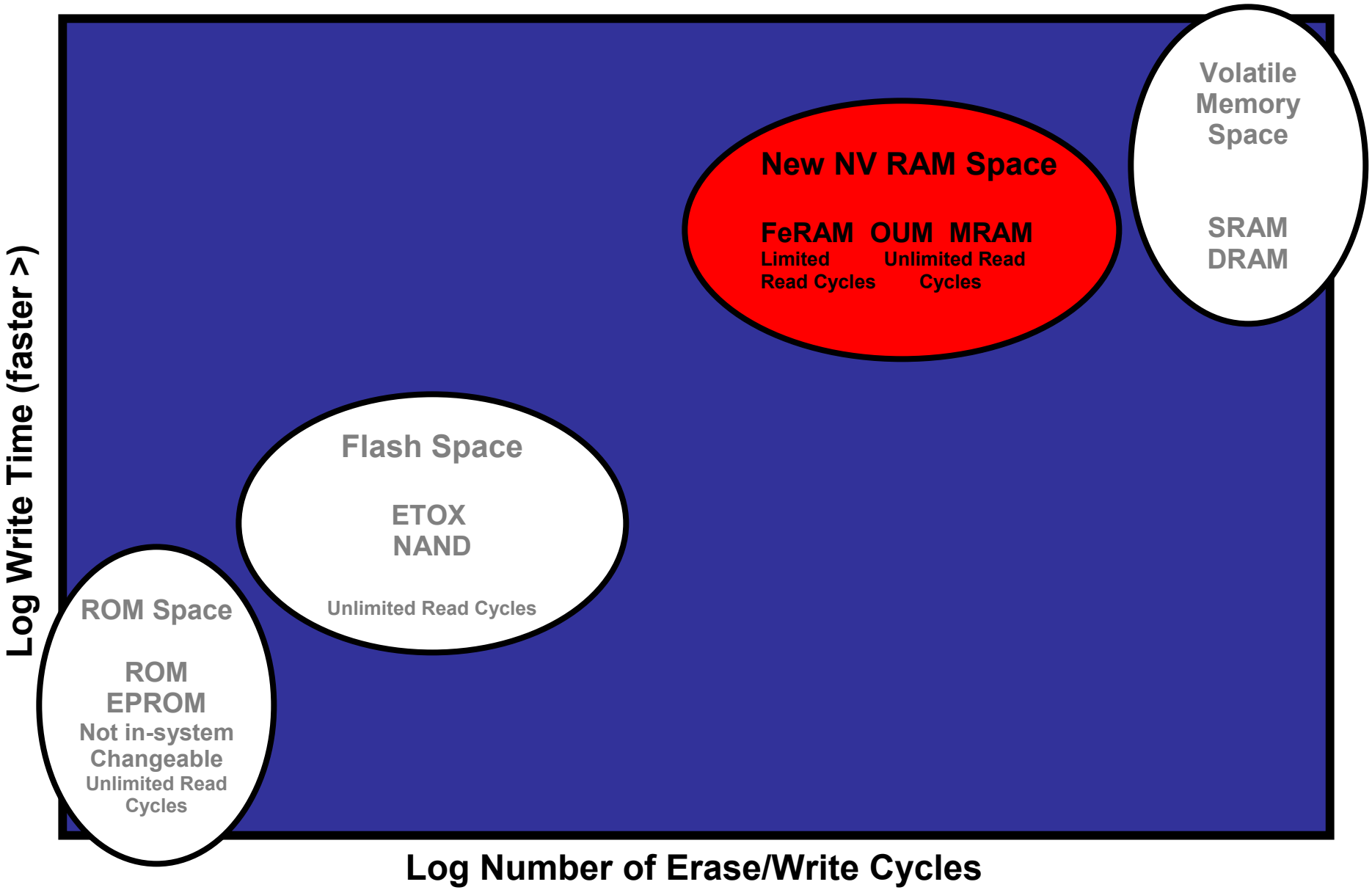


** Other brands and names are the property of their respective owners*

S. Lai - Intel

Many choices in development

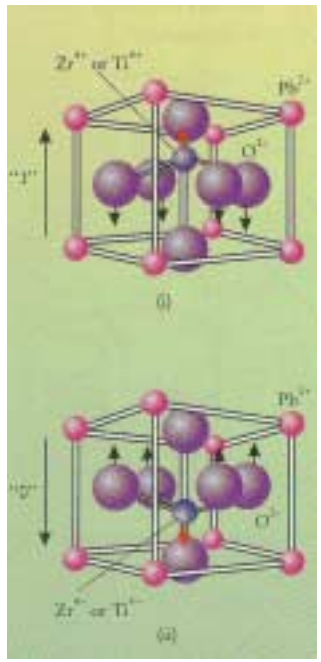
Memory Technologies Comparison

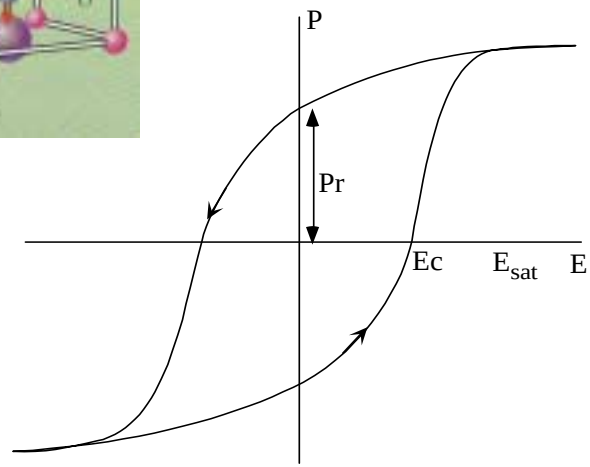


FeRAM

What Is FeRAM?

- **Operation**
  - Selected crystalline materials have spontaneous polarization
  - Data is stored by applying a voltage to align the internal dipoles “Up” or “Down”
- **Attributes**
  - Non-Volatile
  - “Fast” Random Read Access
  - Fast Write with very low power consumption
  - Destructive read, limited read and write cycles

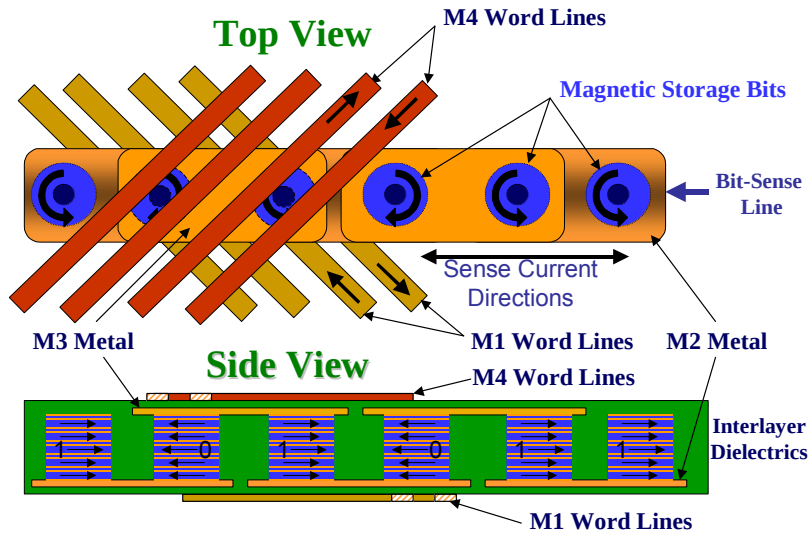


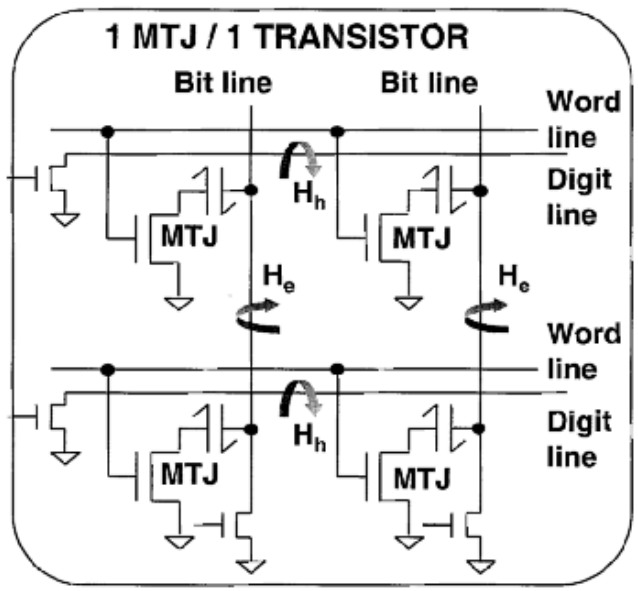


Source: Physics Today 7/98

MRAM

- Operation
  - Cell is 1 MJT + 1 Transistor
  - Electric current switches the magnetic polarity
  - Change in magnetic polarity sensed as resistance change
- Attributes
  - Non-Volatile, High Density
  - Non Destructive Read
  - Low Voltage & Low Power
  - Write = Read Speed, < 50 nsec
  - Unlimited R/W Endurance
  - Material compatibility with CMOS a key challenge





S. Lai - Intel

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New Front End Materials & Modules

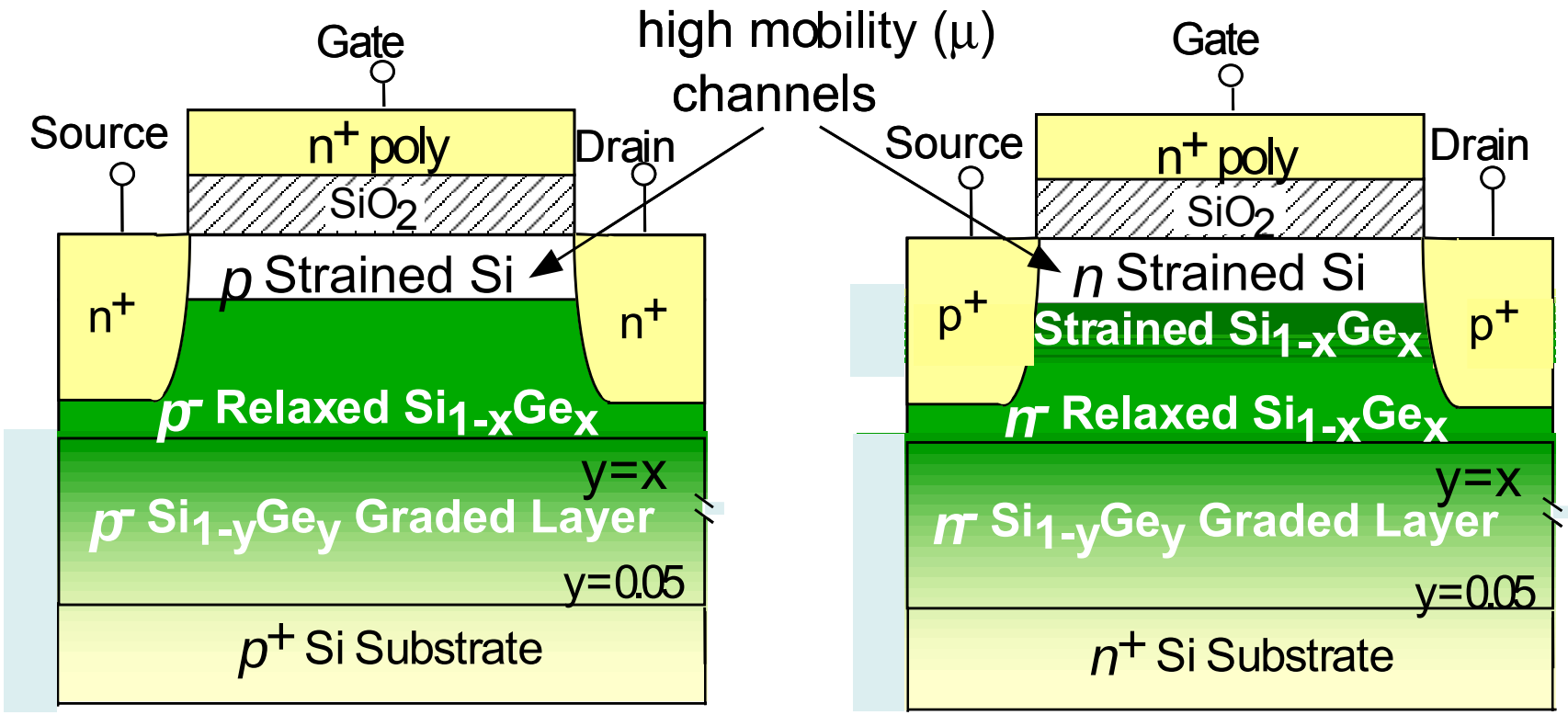
- **Substrates:**
  - Strained Si
  - SOI; Ultra Thin Body (UTB) Si
  - 450mm
- **Gate Dielectrics: Oxide to High-k**
- **Gate Electrodes: doped polySi to metal gate**
- **Ultra-Shallow Junctions:**
  - Raised S/D
  - Non-equilibrium annealing
- **Gate Etch / CD Control and Clean**

Substrates

Progression of *CMOS* substrate technologies:

- ▼ Bulk Silicon
- ▼ Bulk Silicon with Backside Gettering
- ▼ Epitaxial Silicon (P/P^+)
- ▼ Partially Depleted (PD-SOI)
- ▼ Strained Silicon (SiGe Relaxed Hetero-structure)
- ▼ Partially Depleted Strained Silicon
- ▼ Fully Depleted (FD-SOI)
- ▼ Fully Depleted Strained Silicon

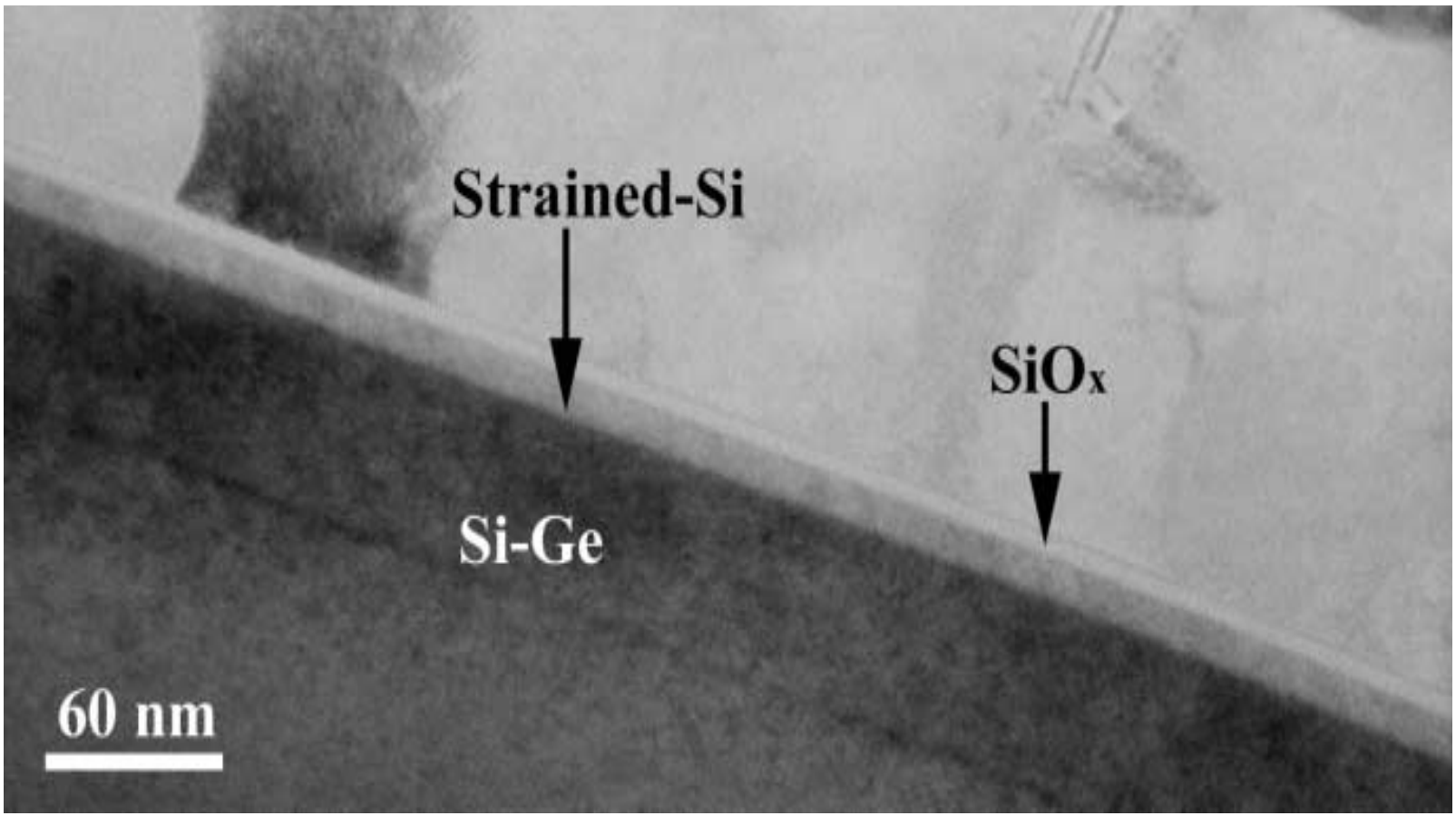
Strained-Si MOSFET Structures



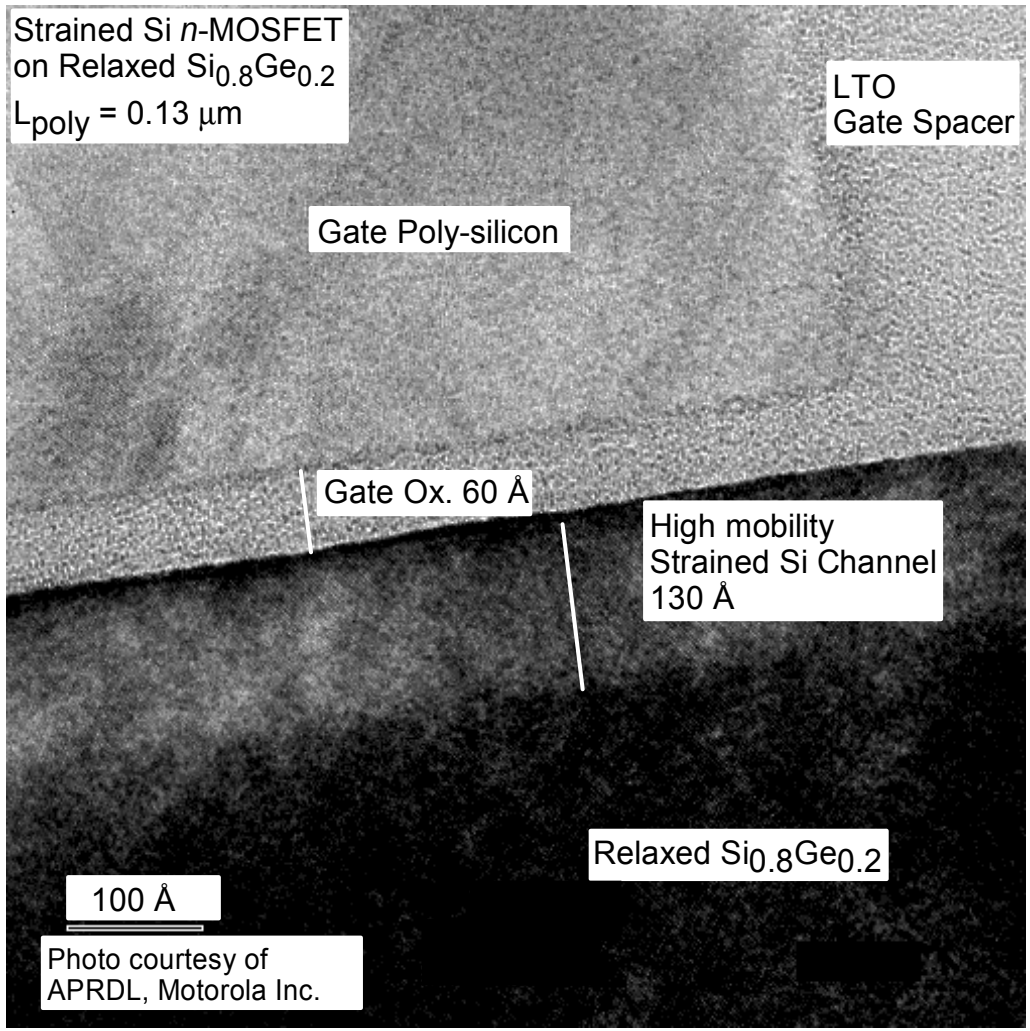
- **+ Increased effective mobility, increased I_{on}**
- **- Difficult integration issues: manufacturability**
- **- Compatibility with ultra-thin body SOI**
- **- Cost (~50% cost adder @300mm)**

Courtesy of J. Hoyt - MIT

Strained Silicon CMOS

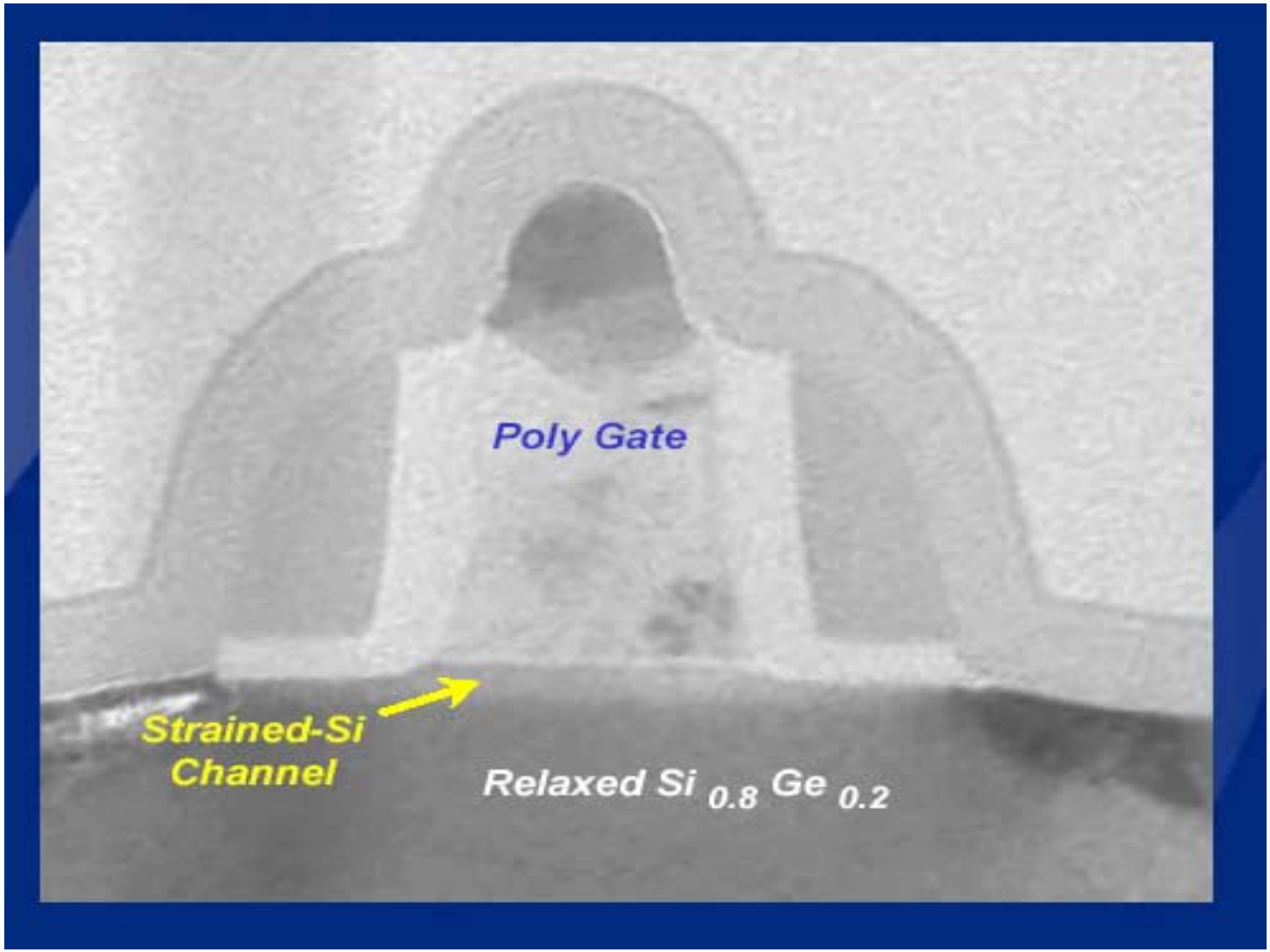


Cross-Section TEM of Strained Si Channel



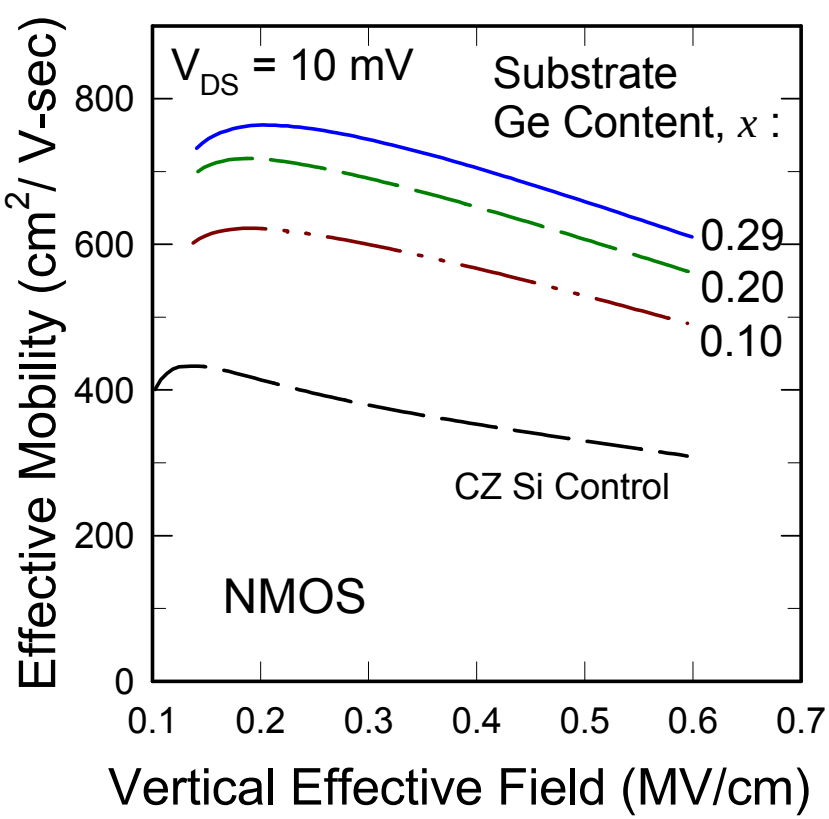
Rim, Hoyt, and Gibbons, IEDM 1998

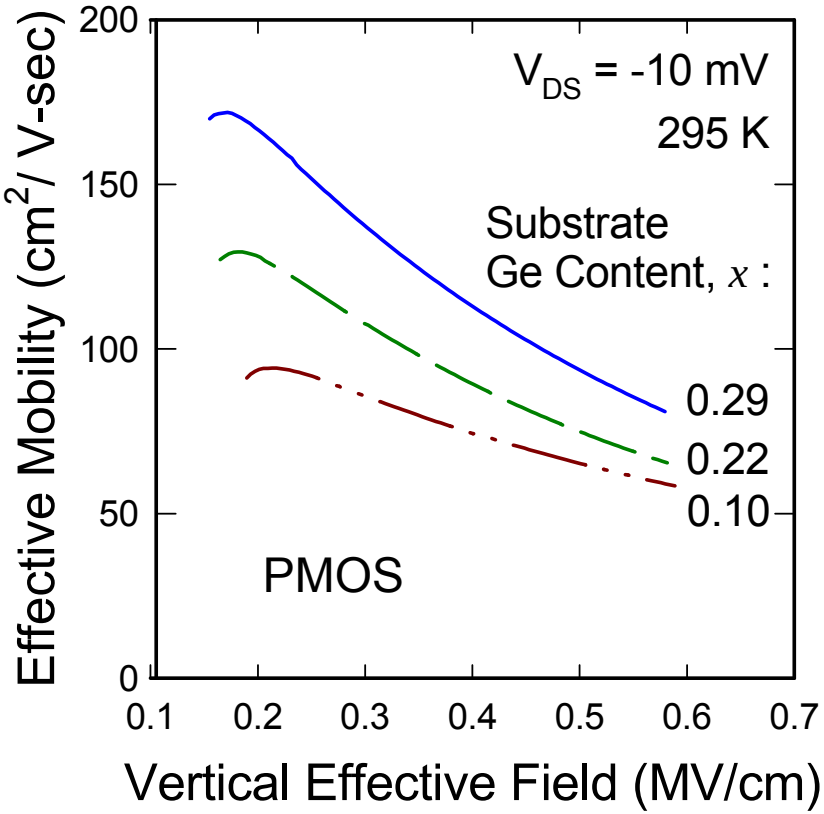
Cross-Section TEM of Strained Si Transistor



Courtesy UMC/Amberwave

Strained Silicon Mobility Enhancement

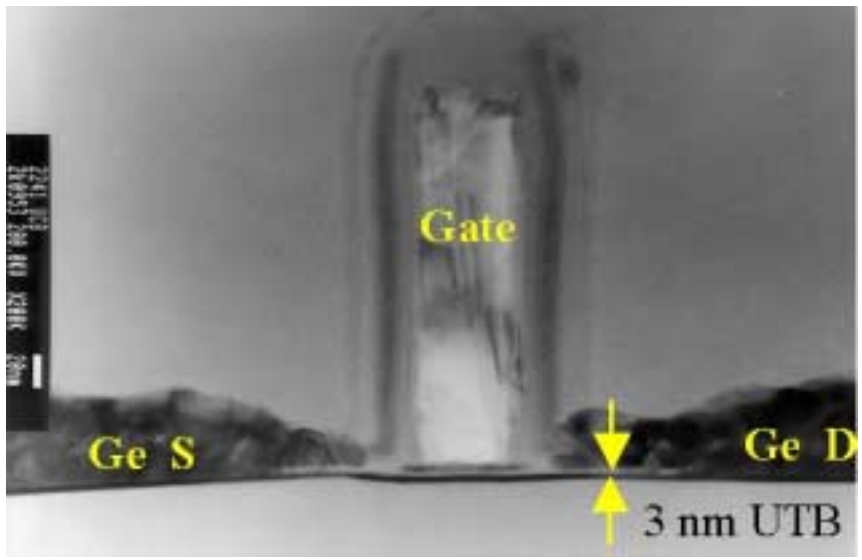


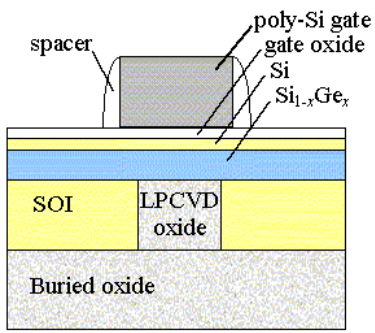


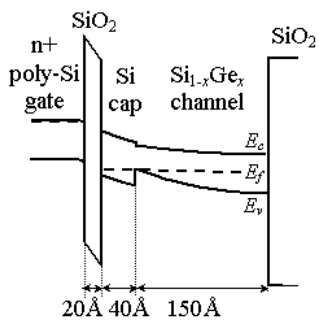
- low-field electron and hole mobilities increase with tensile strain in Si
- peak mobility enhancement ratios: ~ 1.8 for 30% Ge substrate

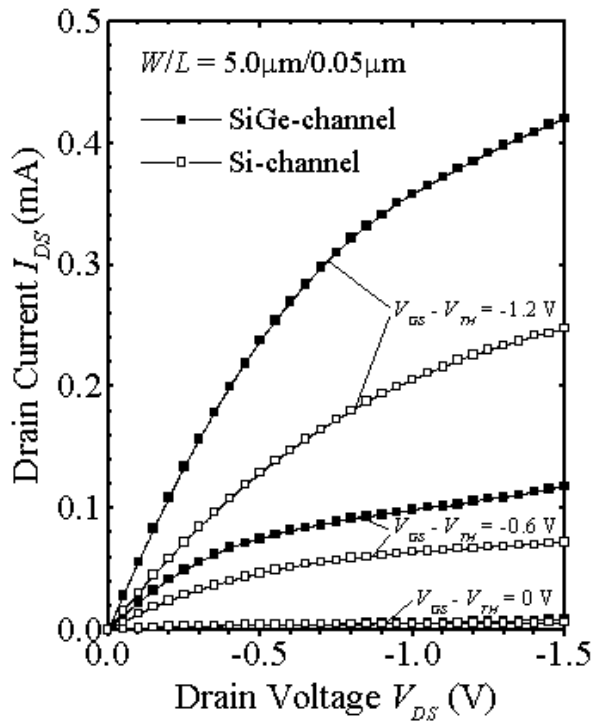
Courtesy Judy L. Hoyt

SOI: Ultra Thin Body (UTB) Si





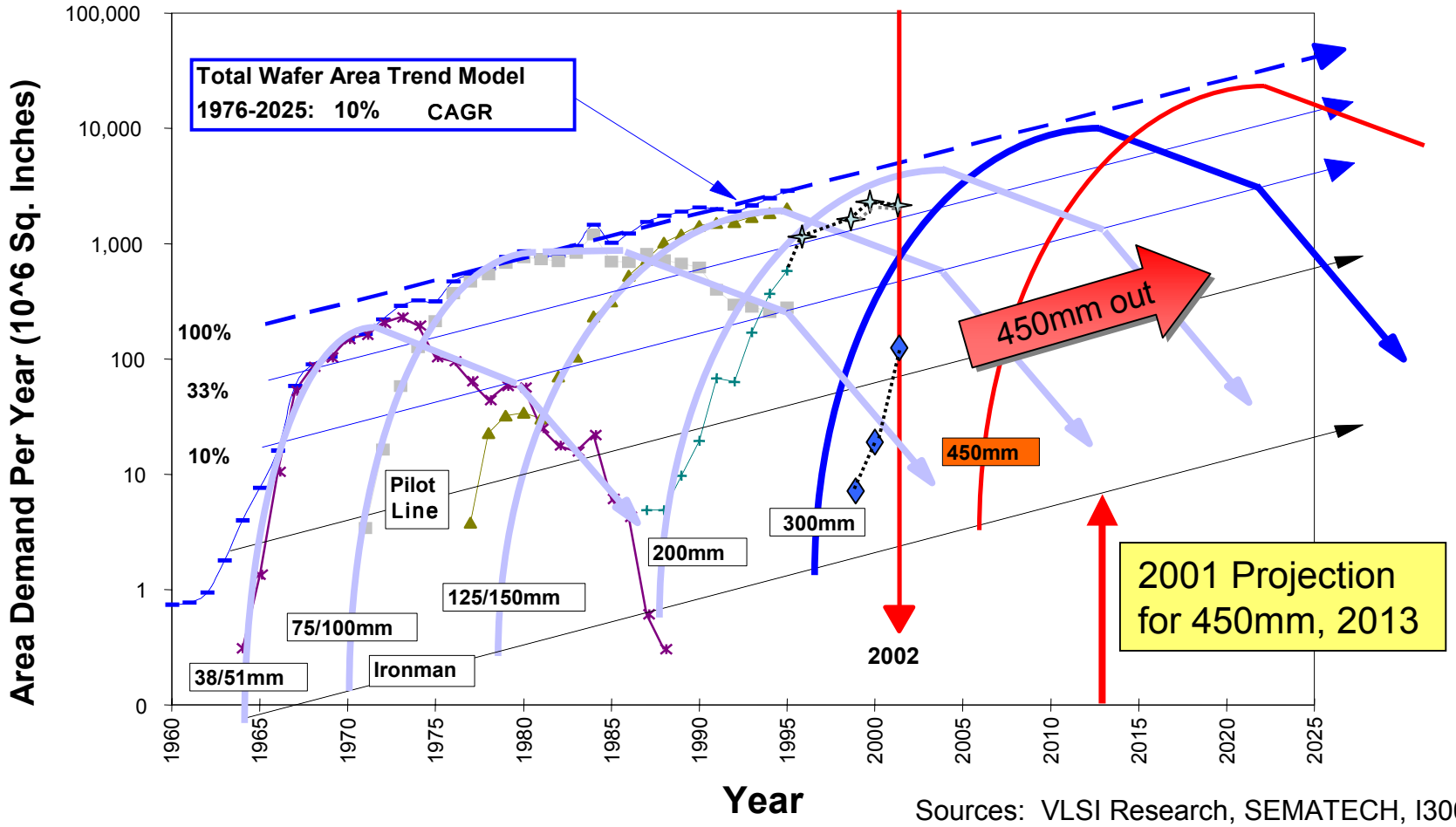




UTB SI with Strained Si combines advantages of SiGe/Si heterostructure with UTB low leakage

Yee-Chia Yeo, et. al. UTBFET for NanoCMOS

Wafer Area Generation Model

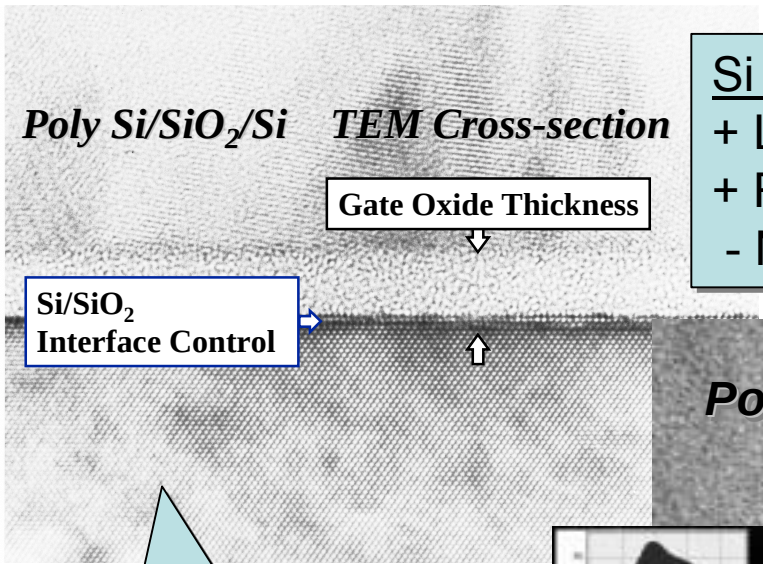


Sources: VLSI Research, SEMATECH, I300I

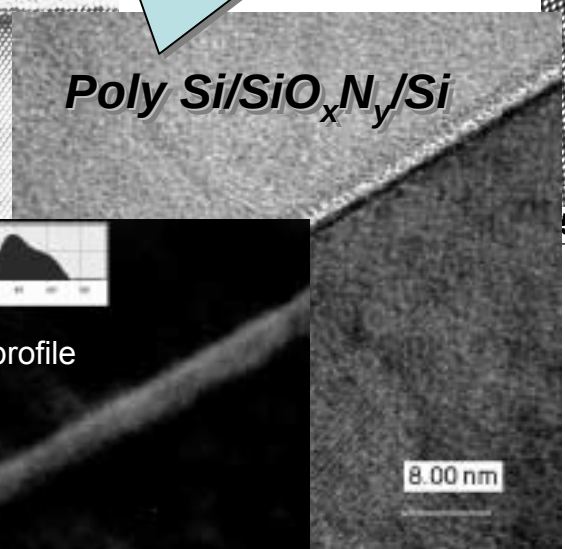
New Front End Materials & Modules

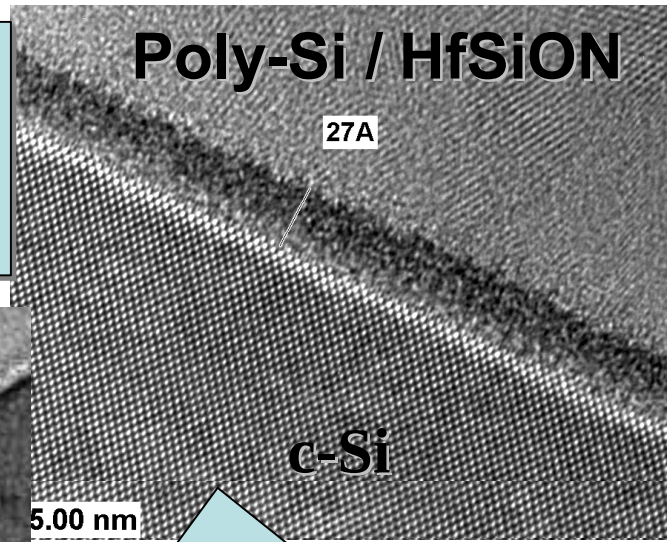
- **Substrates:**
  - Strained Si
  - SOI; Ultra Thin Body (UTB) Si
  - 450mm
- **Gate Dielectrics: Oxide to High-k**
- **Gate Electrodes: doped polySi to metal gate**
- **Ultra-Shallow Junctions:**
  - Raised S/D
  - Non-equilibrium annealing
- **Gate Etch / CD Control and Clean**

Gate Dielectric: SiO_2 to High-k



Si Oxynitride
+ Low B penetration
+ Reliable
- Not scalable <1nm





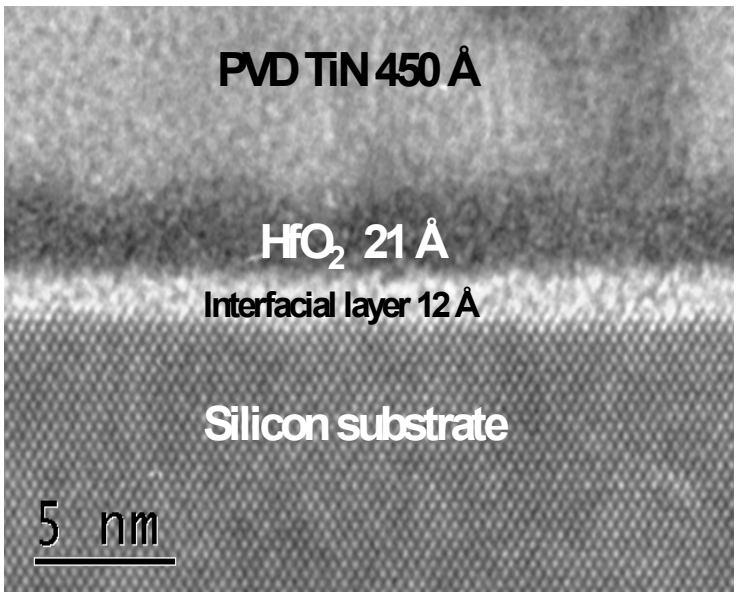
Si Oxide
+ Long History
+ Reliable
- Leaky < 25A

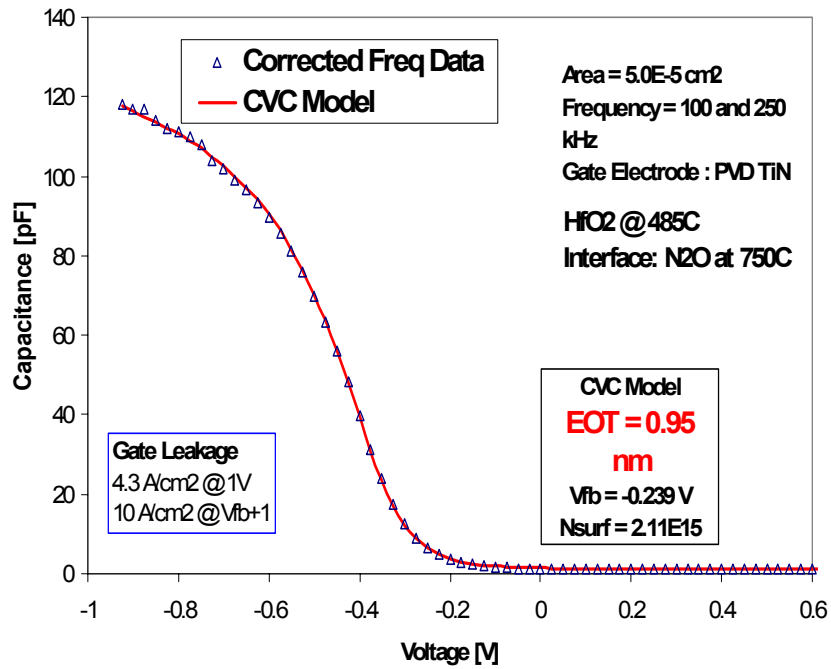
HfSiON
+ Mid High-k
+ Scalable <1nm
+ Low B penetration
- Mobility degraded ~15%

Node: >/~250nm **180nm – ~65nm** **≤65nm?**

MOCVD HfO_2 High-κ Dielectric

Effective Dielectric Constant ~ 13.5

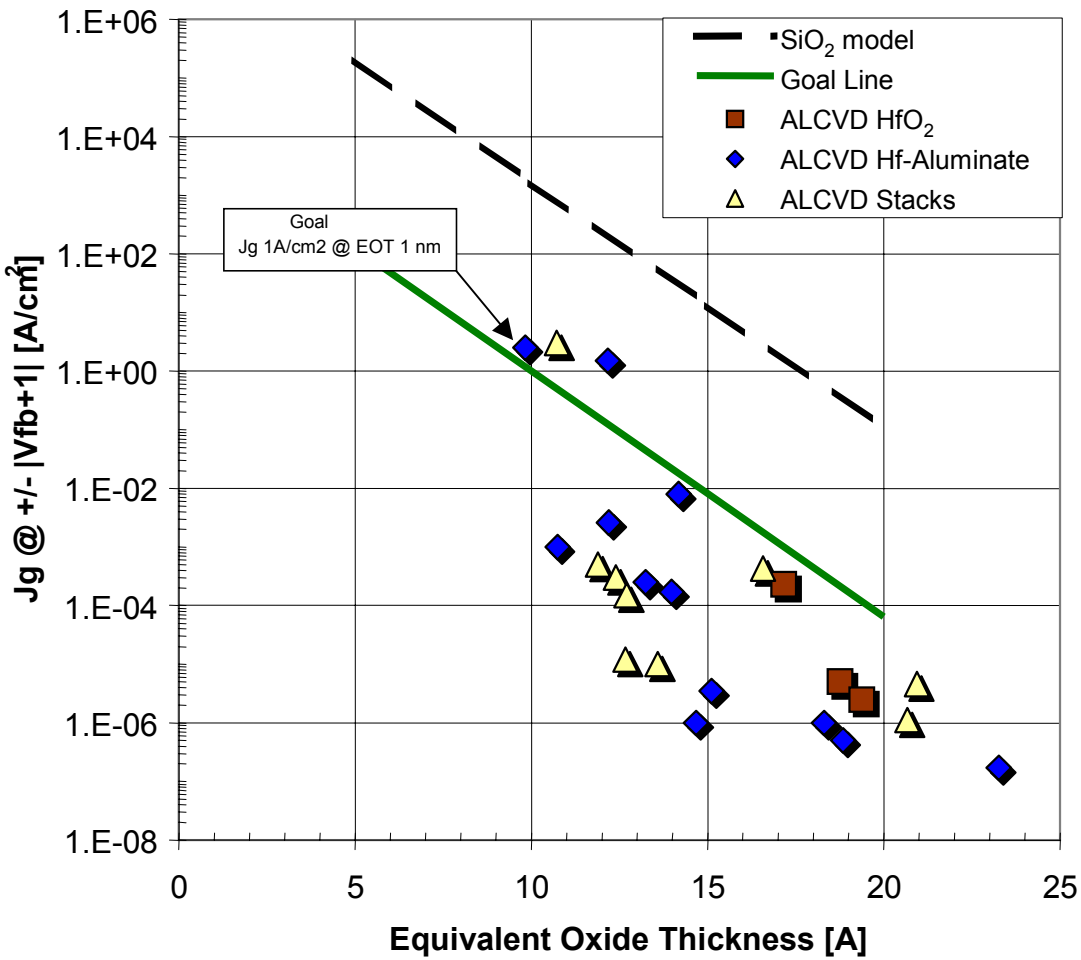




TEM (left) for MOCVD HfO_2 with EOT = 0.95 nm and CV curve (right) [80]

Courtesy International SEMATECH

High-k Leakage Current versus EOT (trends)

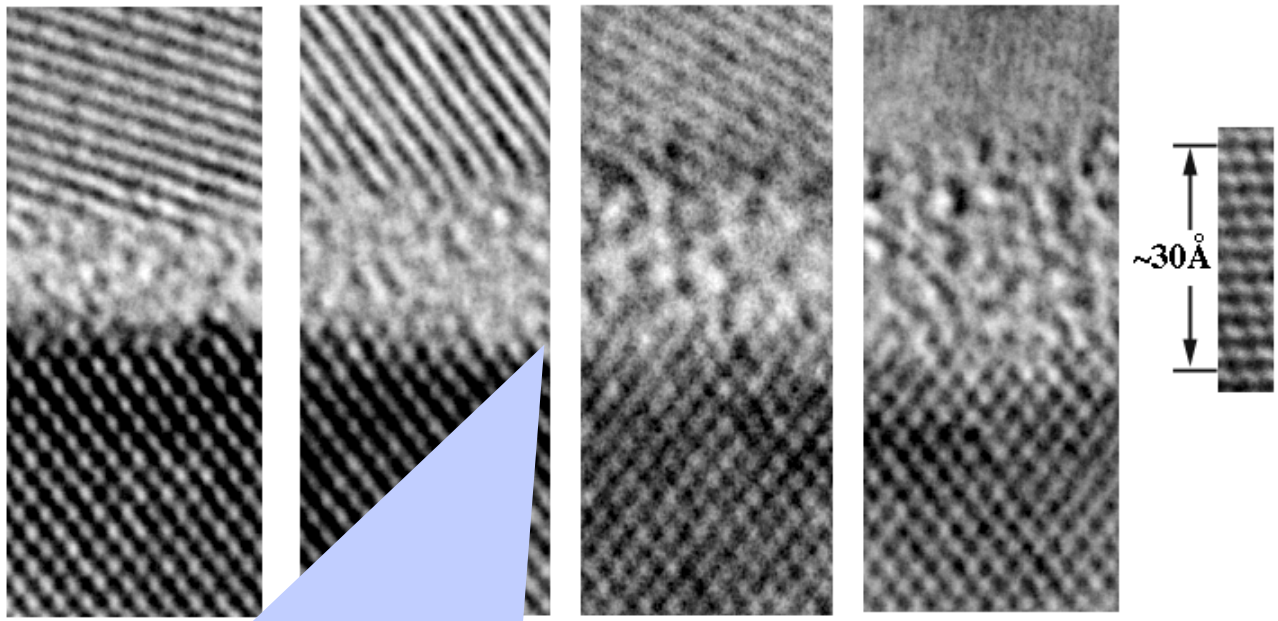


High-k Manufacturability Issues

- Interface dielectric preparation and control
- High-k dielectric amorphous phase thermal limitations
- Material etch characteristics / selectivity
- Boron penetration resistance
- High-k dielectric interactions with gate electrode
- Deposition complexities for multi-component dielectric materials
- Conformal depositions for non-planar gate structures
- Metrology of heterogeneous multilayer dielectric films

Gate Dielectric Scaling

Vertical Scaling



HRTEM 14.2 ± 1.7 Å 18.6 ± 1.7 Å 26.2 ± 2.2 Å

"Interface Control is critical to achieve <10A effective Gate Dielectric - To achieve 7A effective thickness:

Interface Dielectric	**<1A**
High-k dielectric	**<1A**
Poly Depletion	**<1A => Metal Gate**
Channel Quantum Effect	**~4A**

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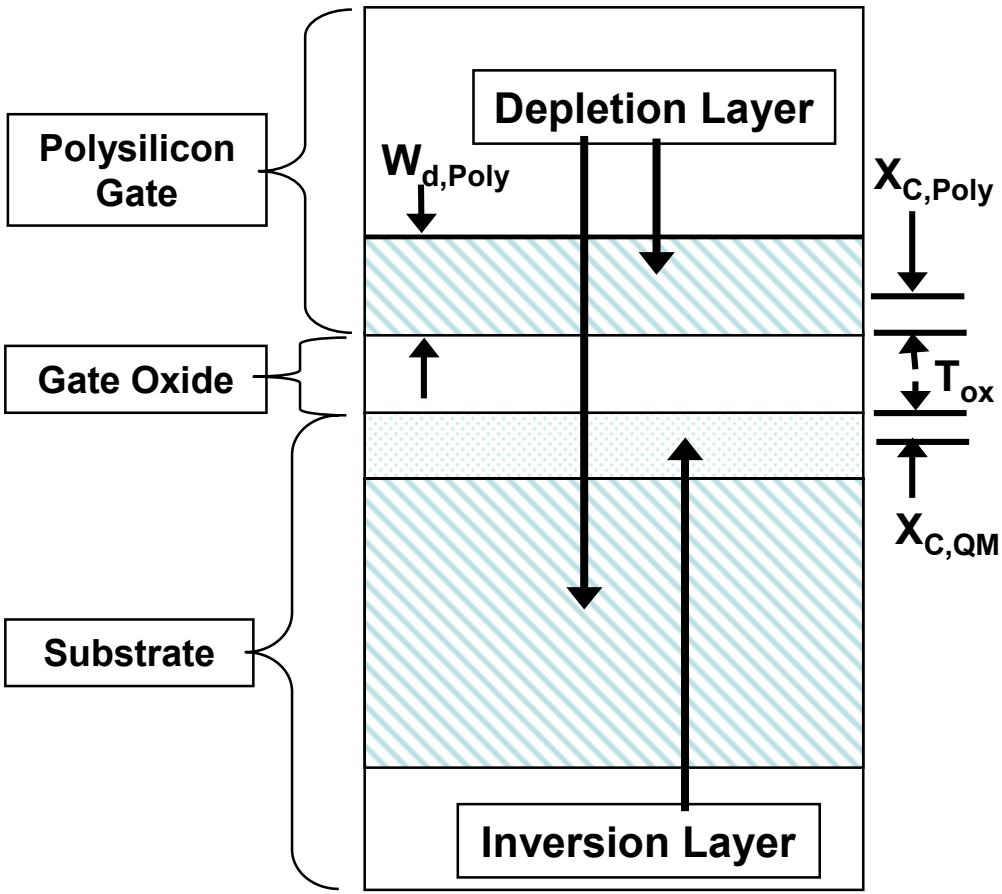
Gate Electrode: Why metal gate?



- polySi depletion
  - EOT reduces => Eox lower => inversion charge lower
  - For EOT scaling => polySi doping must increase
- PMOSFETs: B penetration with thin gate dielectrics
  - Nitrided gates used to reduce B penetration
- Compatibility of polySi with high-k dielectrics
- Gate resistance of very thin gates even with silicide

Gate Electrode Options

	Pro's	Con's
N+ Poly gate	- Simpler Process	- Required doping level higher than PD/Bulk
Mid-gap gate	- No poly depletion - Intrinsic devices: (high μ expected)	- V_T can not be lower than 0.4V
Metal gate	- No poly depletion - V_T can be lower than 0.4V - Intrinsic devices: (high μ expected)	- Identification of Dual Metal system - Integration difficult, esp. Dual Metal

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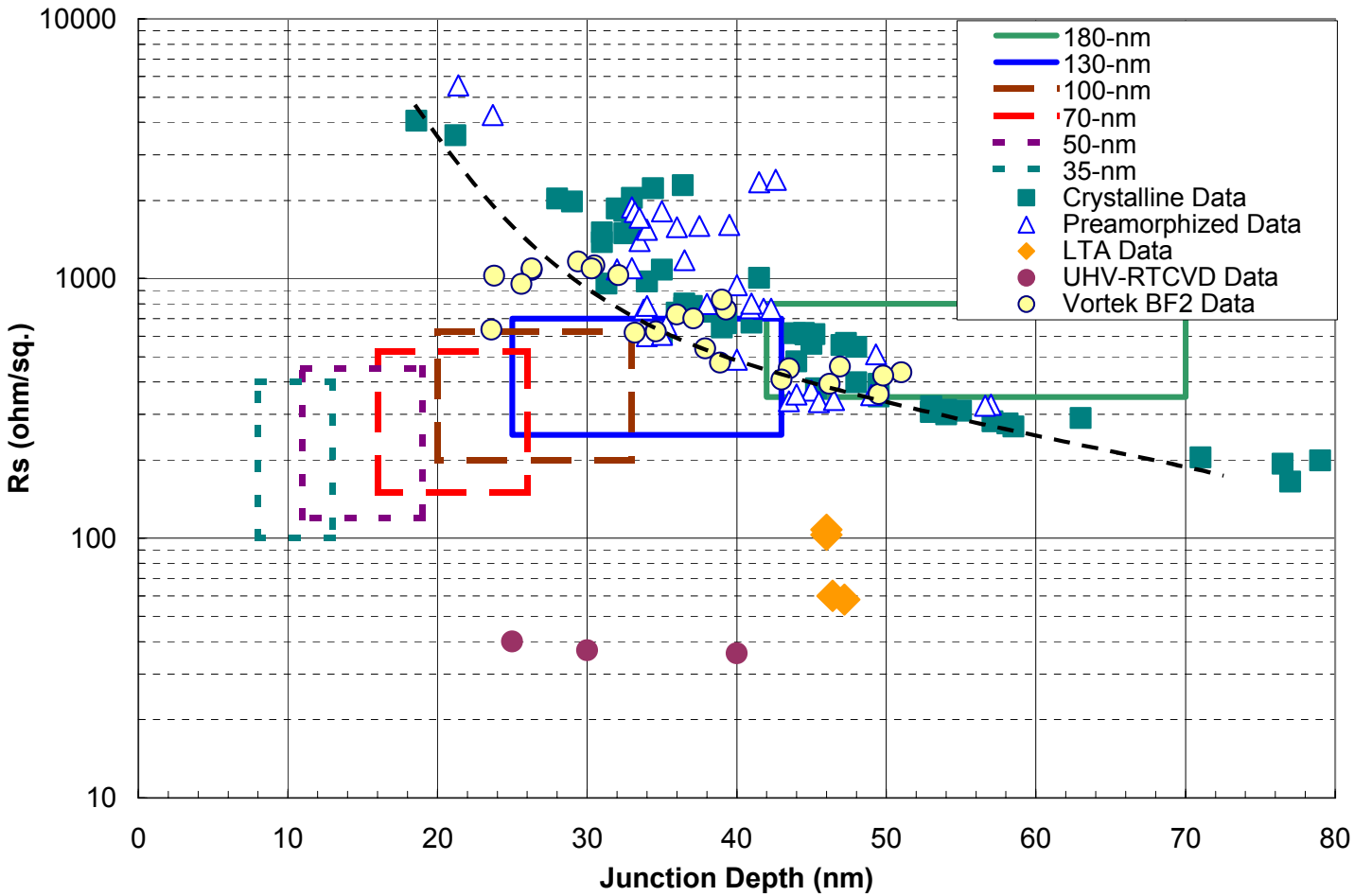
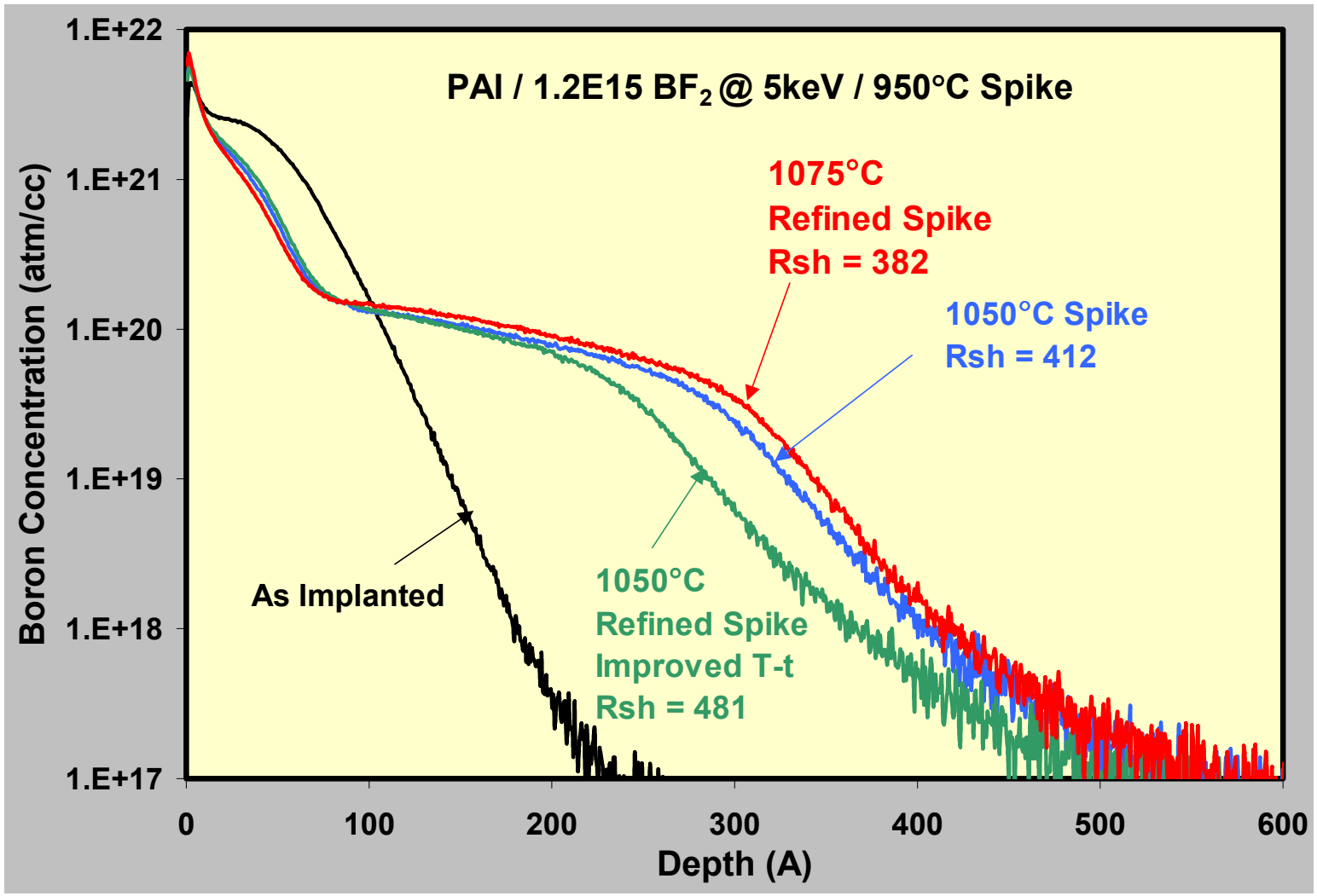
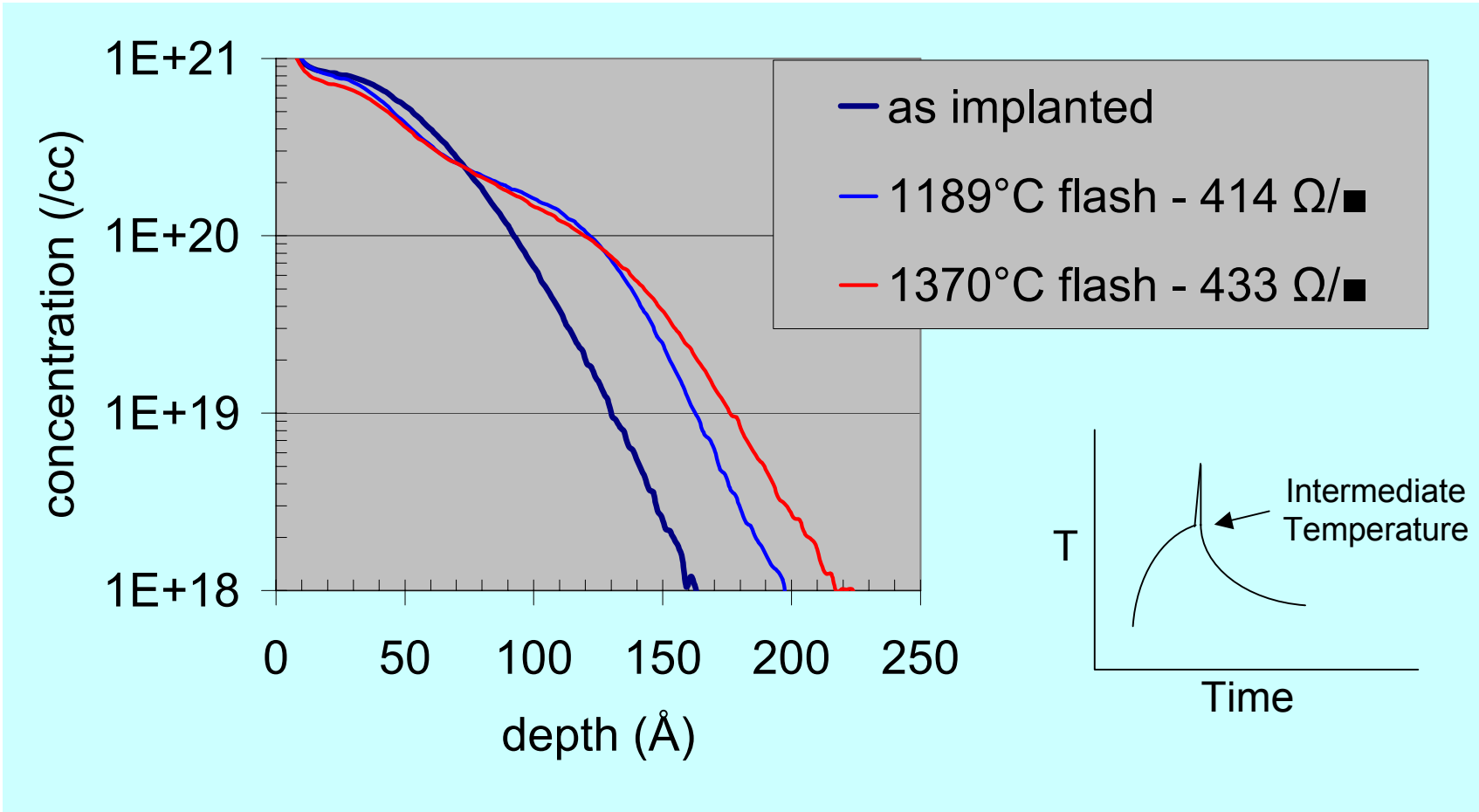
Ultra-Shallow Junctions - USJ



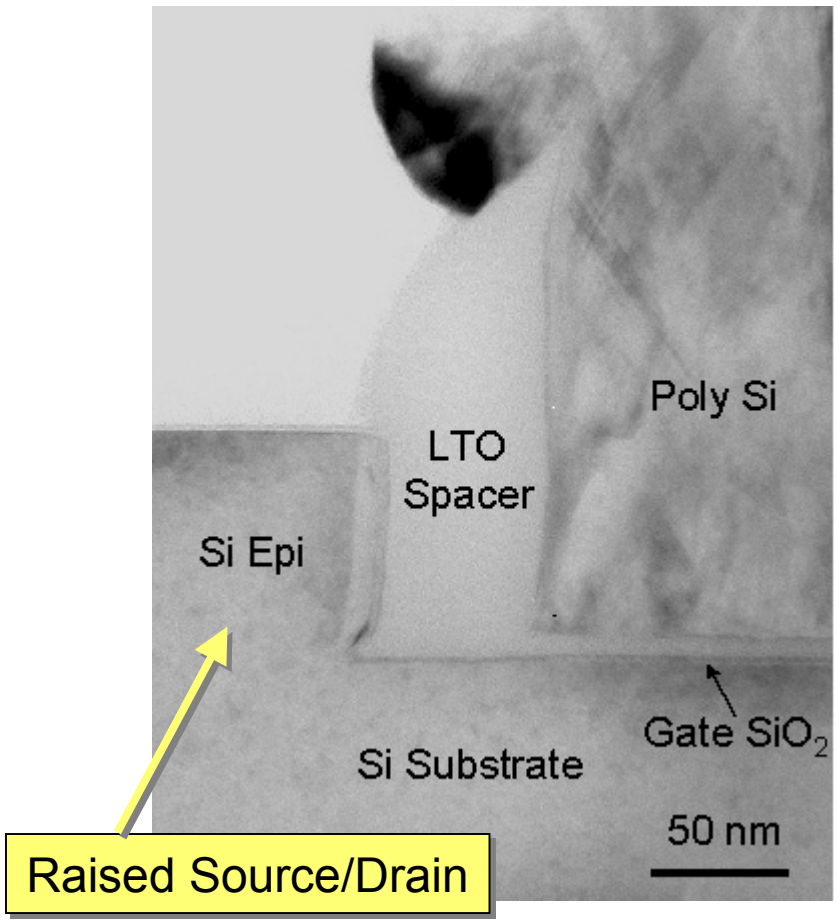
USJ – Advanced Spike RTA



Flash assisted Impulse Anneal, 800°C Intermediate Temperature



Raised Source/Drain



- **Advantages**
  - Improves drive current
  - Improves SCE
  - Essential for FD-SOI with ultra-thin-body
- **Needs**
  - Low Temp Selective EPI process <650 C
  - Facet control at sidewall edge
  - High doping (Ge, B, P)
  - Low defects
  - Good uniformity
  - Low CoO

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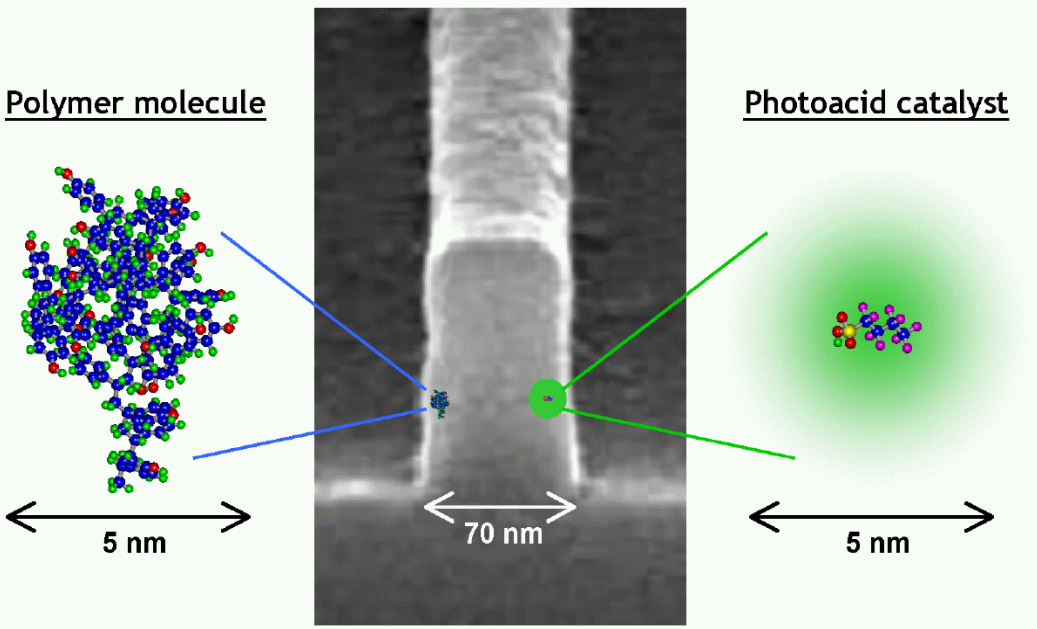
Gate Stack Etch

Line and sidewall edge roughness

The dimensions of resist features are now at a scale where the effects of individual molecules are important.



Issues:

LER of resist

- resist molecular scales (~ 5 nm)
- image contrast and flare
- mask roughness
- development effects

Etched gate edge roughness

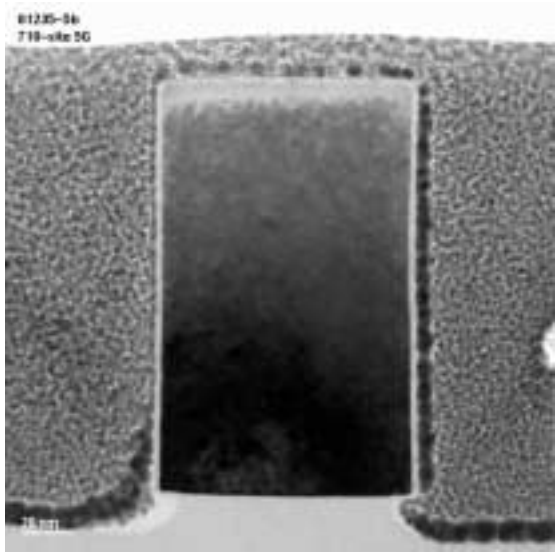
- transfer of LER from resist
- does not scale with etch bias
- granularity of film stack adds

Parameters involved in Line-edge roughness add in quadrature:

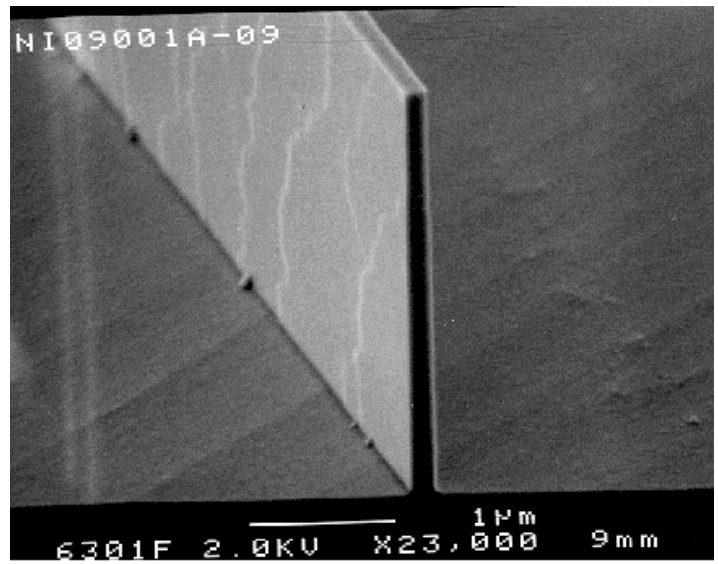
$$\sigma_{LER}^2 = \sigma_{SHOTNOISE}^2 + \sigma_{DIFFUSION}^2 + \sigma_{AERIAL\ IMAGE}^2 + \sigma_{DEVELOPMENT}^2 + \sigma_{ETCH}^2 + \sigma_{MASK}^2$$

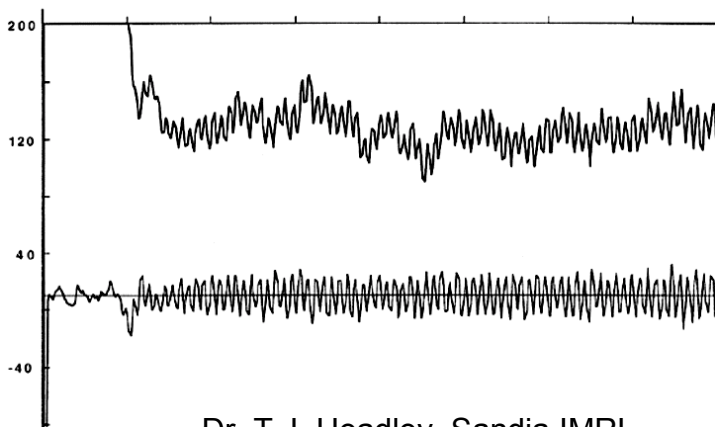
Gate Stack CD Control

Lateral Scaling



293 lattice planes = 91.9nm wide





Dr. T.J. Headley, Sandia IMRL

Atomistic Lateral Scaling of Gate Length

Gate Edge CD Control and Transistor Performance critical to etching and cleaning chemistries

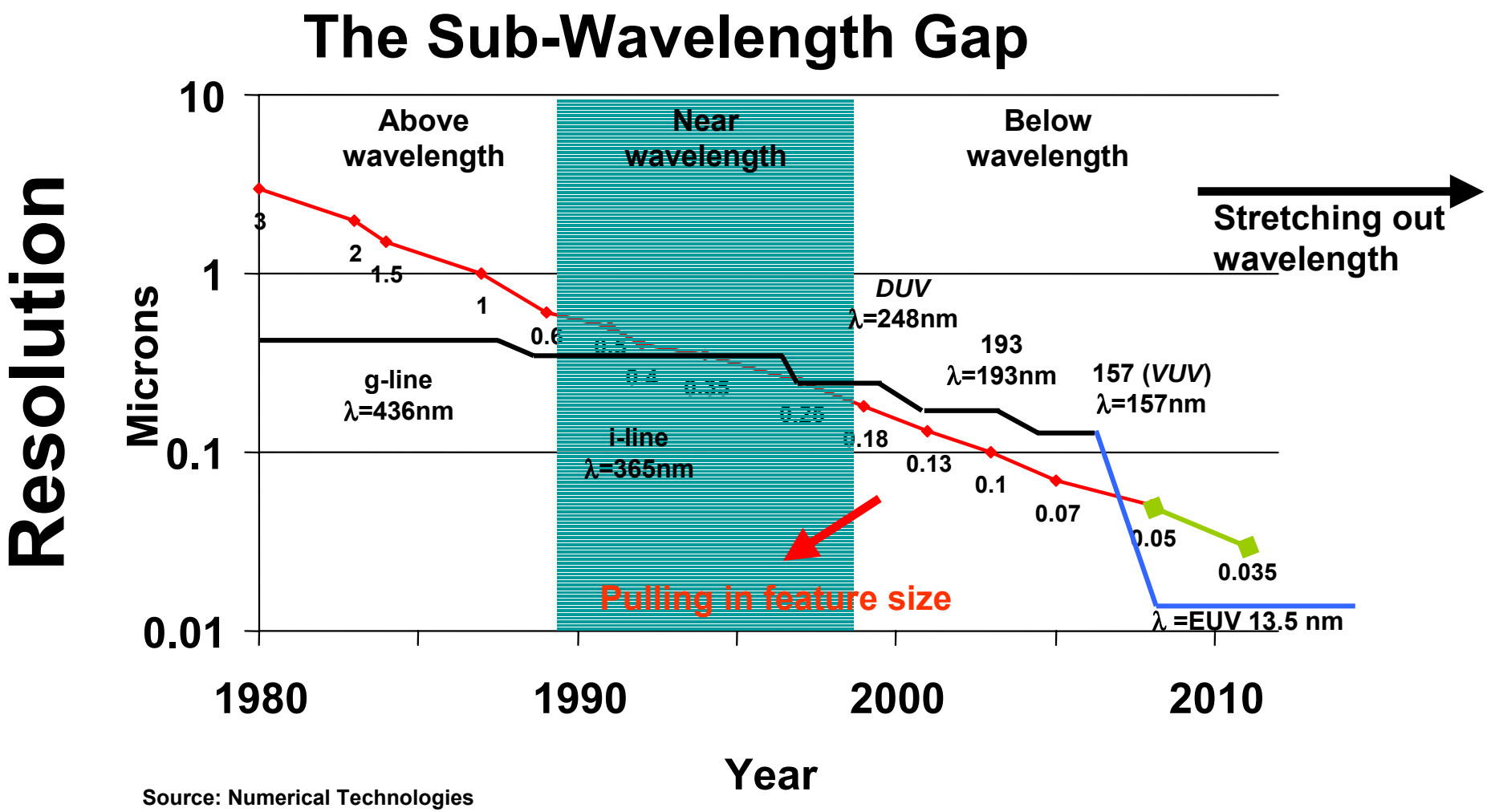
FEOL Clean Challenges

- **New Materials and Processes**
  - Cleaning and drying High Aspect Ratio (HAR) structures
  - Interface control for deposited high-k dielectrics
  - Post high-k gate stack etch cleans compatible with exposed materials and CD control
  - Interface control for epitaxial Si and Si-Ge
- **Scaling and Defect Levels**
  - Removal of small particles without affecting materials and structures
  - Control of contaminates (carbon, etc) for non-oxide gate dielectrics
- **ESH**
  - Chemical, DI water, energy reduction, and hazardous chemical elimination and avoidance

Topics

- Transistor Performance Trends
- Transistor Scaling Challenges
- New Device Architectures
  - Advanced CMOS
  - Non-Classical CMOS
  - Memories
- New Front End Materials & Modules
- Lithographic Trends
- Summary

Lithographic Front End Trends



Source: Numerical Technologies

Lithographic Front End Trends

iedm

In Keeping Pace with Moore's Law

Start mass production	2001	2003	2005	2007
Technology generation	130 nm	90 nm	65 nm	45 nm
Minimum half-pitch	160 nm	115 nm	80 nm	55 nm
k_1-factor	λ=248 nm, NA=0.7 0.45 λ=193 nm, NA=0.63 0.52	λ=193 nm, NA=0.63 0.38 λ=193 nm, NA=0.75 0.45	λ=193 nm, NA=0.85 0.35 λ=157 nm, NA=0.85 0.43	λ=157 nm, NA=0.95? 0.33 λ=157 nm, NA=1.25? 0.44
Respective DOF in micron	0.48 0.47	0.47 0.32	0.25 0.22	0.16 0.09
Layer-layer overlay	45 nm	32 nm	22 nm	15 nm

Liquid immersion lithography, assuming index = 1.4 and NA = 0.9 in liquid

Summary

- Front End Manufacturing Technology will undergo significant changes both in the near-term and long-term as new processes, materials, and structures are introduced to meet Roadmap scaling requirements.
- Material and process solutions potentially include high-k dielectrics, metal gate electrodes (mid-gap/dual), SOI (PD/FD), Strained Si, Spike and/or non-equilibrium annealing, Raised S/D, and others yet to be identified.
- Longer-term new non-classical CMOS structures such as Dual Gate, FinFET, PI/Tri-gate, may be required in combination with new materials to provide the ultimate End-of-Roadmap devices.

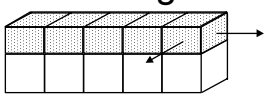
Acknowledgements

- Allen Bowling, Texas Instruments
- Olivier Faynot, LETI
- Judy Hoyt, MIT
- Majid Mansoori, Texas Instruments
- Shane Palmer, Texas Instruments
- Walt Trybula, International SEMATECH
- Rick Wise, Texas Instruments
- Peter Zeitzoff, International SEMATECH

Backup Charts

Effects of Biaxial Tensile Strain on Si Energy Bands and Mobility

Strained Si grown on Relaxed $Si_{1-x}Ge_x$

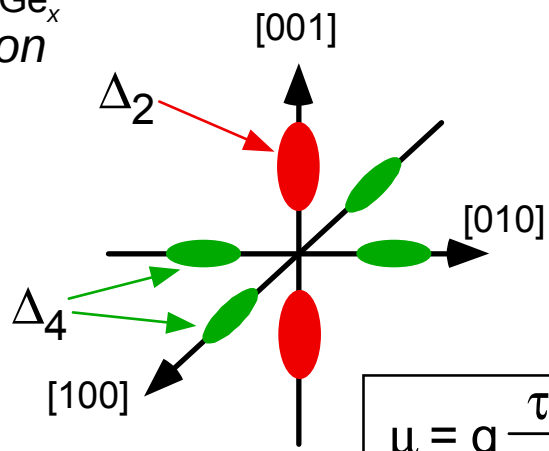


biaxial tension

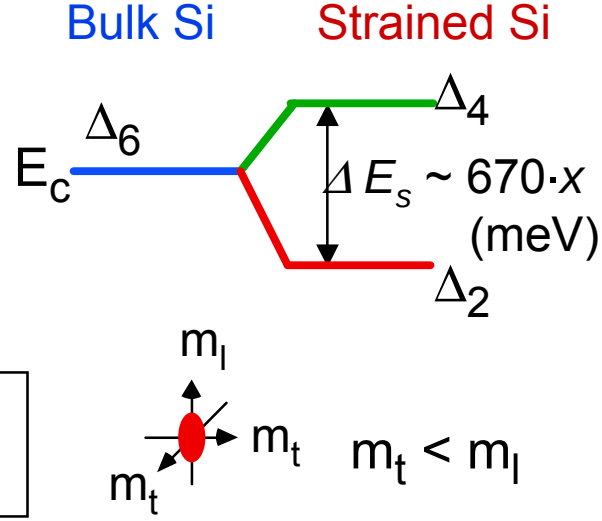
Conduction Band

Splitting between Δ_2 and Δ_4

- reduced intervalley scattering
- smaller in-plane effective transport mass



$$\mu = q\frac{\tau}{m_c^*}$$



Valence Band

HH/LH degeneracy lifted at Γ

- reduced interband scattering
- smaller in-plane transport mass due to band deformation