A Three-Transistor Threshold Voltage Model for Halo Processes

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Abstract

A closed-form expression for the threshold voltage, V_t, of MOSFETs fabricated with halo processes is described. The proposed approach accurately captures the length dependent V_t behavior under different drain and body bias conditions and temperature. In addition, the necessity of considering separate V_t expressions for current and capacitances is discussed. A doping transformation is employed to obtain equivalent channel dopings, necessary for charge-sheet models that do not rely on the threshold voltage concept.

1. Introduction

Current MOSFET technologies make use of halo or pocket implants [1-3] for improved scaling and control of short-channel effects. These processes result in non-uniform channel doping profiles along the device length, as illustrated in Fig. 1, which in turn gives rise to the well known reverse short-channel effect (RSCE). A closed-form V_t solution for non-uniform lateral doping profiles is not trivial. The few models that have appeared in the literature [4-6] are empirical and do not capture the physical RSCE behavior observed in strong halo processes. In addition, the different behaviors of I-V and C-V characteristics for halo processes have not yet been discussed in the literature.

The lack of a good RSCE model as a function of channel length is one of the leading causes for the need for multiple model parameter sets for circuit simulations, using the so-called parameter binning approach [6]. Parameter binning suffers from many drawbacks, including the time and effort to generate model parameters, lack of scalability, problems with smoothness, etc. This is illustrated in Fig. 2 by fitting V_t using BSIM4's binning approach.

Here, we propose a more physical RSCE model that enables accurate fits to the channel length dependency without the need for parameter binning.

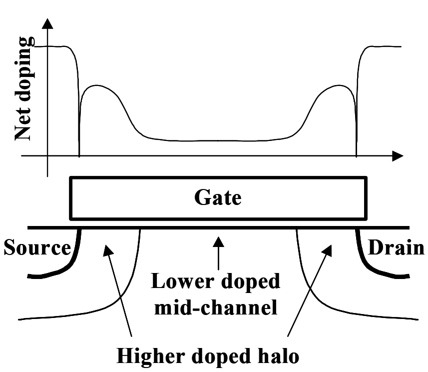

Fig.1: Illustration of non-uniform channel doping resulting from typical halo processes.

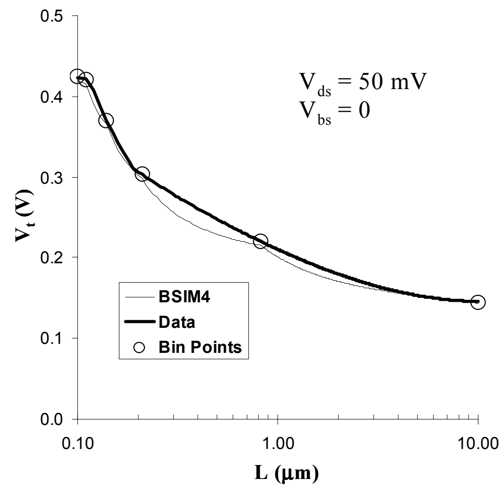

Fig. 2: V_t fits using the binning approach of BSIM4. The accuracy and smoothness of the fits are strongly dependent on the number and location of bin points.

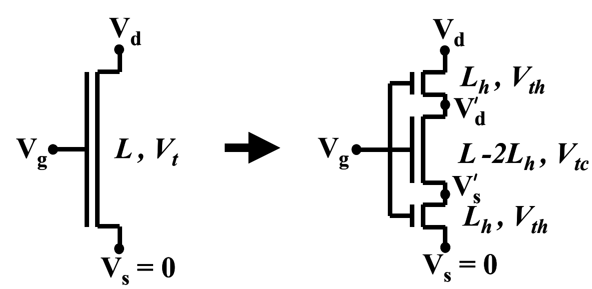

Fig. 3: Schematic representation of the device as formed by a center device with threshold V_{tc}, bounded by two edge devices of length L_h and threshold V_{th}.

2. Model description

The effect of the non-uniform lateral doping can be approximated by considering a composite device formed by three transistors in series, as illustrated in Fig. 3, with a center device with low threshold, V_{tc}, bounded by two edge devices with higher threshold, V_{th}. The series connection of the three transistors is considered for the channel current. To find the threshold voltage of the composite device for I-V, the sub-threshold currents are matched, resulting in a system of three independent equations with the unknowns V_t, V'_d and V'_s:

$$\frac{e^{-\beta V_t}}{L}\left(1-e^{-\beta V_d}\right)=\frac{e^{-\beta V_{th}}}{L_h}\left(1-e^{-\beta V_s'}\right) \tag{1}$$
$$=\frac{e^{-\beta V_{tc}}}{L-2L_h}\left(1-e^{-\beta (V_d'-V_s')}\right)=\frac{e^{-\beta V_{tc}}}{L_h}\left(1-e^{-\beta (V_d-V_d')}\right)$$

where β is the inverse of the thermal voltage $v_T = kT/q$.

Solving (1) for V_t leads to the following expression, valid for $L > 2L_h$:

$$V_{t_{(I-V)}} = V_{tc} + v_T \ln\left[1 + \frac{2L_h}{L}\left(e^{\beta(V_{th}-V_{tc})} - 1\right)\right] \qquad (2)$$

For the device quasi-static capacitance, we must consider the parallel connection of the devices in Fig. 3. Equating the sum of the sub-threshold inversion charges leads to:

$$V_{t_{(C-V)}} = V_{tc} - v_T \ln\left[1 + \frac{2L_h}{L}\left(e^{-\beta(V_{th}-V_{tc})} - 1\right)\right] \qquad (3)$$

For charge-sheet, surface potential based models, that do not use threshold voltage explicitly, we can find equivalent dopings for the composite device using the doping transformation:

$$N_a = \frac{(\varepsilon_{ox} V_t)^2}{4q\varepsilon_{Si} t_{ox}^2 \phi_f} \qquad (4)$$

obtained directly from the depletion charge contribution. Using (4), and ignoring the weak doping dependency of the band-bending ϕ_f, the equivalent dopings for any given channel length are given by:

$$N_a = \left\{\sqrt{N_c} + \frac{s v_T}{\delta}\ln\left[1 + \frac{2L_h}{L}\left(e^{s\delta\left(\sqrt{N_h/2+N_c}-\sqrt{N_c}\right)/v_T} - 1\right)\right]\right\}^2, L \geq 2L_h$$

$$N_a = \begin{cases} N_c + N_h \dfrac{L_h}{L}, & L_h < L < 2L_h \\ N_c + N_h\left(2 - \dfrac{L}{L_h}\right), & L \leq L_h \end{cases} \qquad (5)$$

$$\delta = 2\frac{t_{ox}\sqrt{q\varepsilon_{Si}\phi_f}}{\varepsilon_{ox}}$$

$$s = \begin{cases} 1 & \text{for I-V} \\ -1 & \text{for C-V} \end{cases}$$

where N_c and N_h are the average dopings of the center and halo regions, respectively. To arrive at the expressions valid for $L < 2L_h$, the additional assumption that the halo doping varies linearly within the length L_h has been used.

Within the assumptions of the three-transistor approximation, the model maintains the correct dependencies for the three physical parameters: background doping N_c, halo doping N_h, and halo characteristic length L_h. Most importantly, the model includes physical dependencies to gate oxide thickness, t_{ox}, and temperature, T, which are essential to preserve the model scalability.

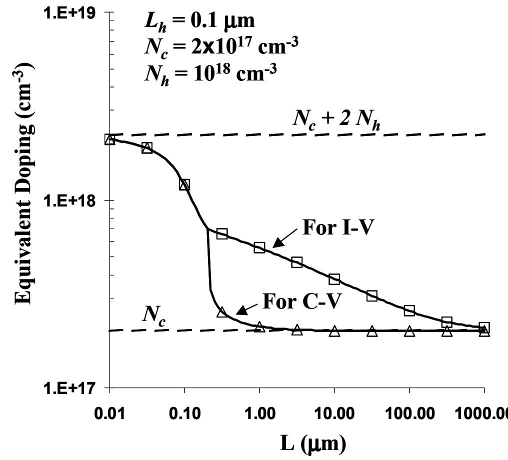

Fig. 4: Example of equivalent channel dopings for I-V and C-V, as given by the expressions (5).

3. Results

Fig. 4 illustrates the length dependency of the equivalent channel dopings for I-V and C-V. For channel lengths > $2L_h$ (when the low-doped center region becomes exposed) the threshold voltage and corresponding equivalent doping for C-V drops very quickly, accounting for the quasi-static buildup of inversion charge in the center device before there is significant lateral conduction.

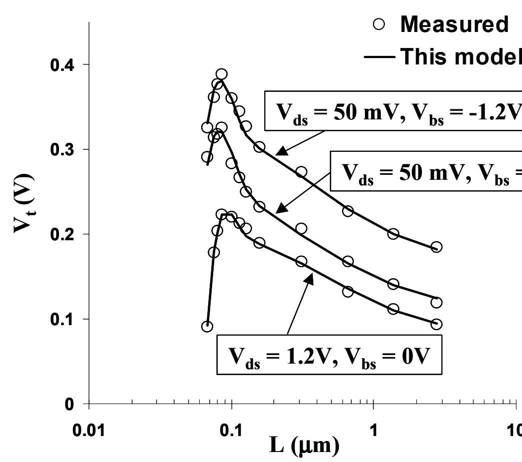

Fig. 5: Model fit to V_t data with a relatively large RSCE effect. The proposed approach captures the correct length dependencies for all bias conditions.

The proposed RSCE model was combined with a short-channel effect (SCE) model similar to the one described in [7] and implemented in Intel's in-house compact MOSFET model. The accuracy of the model is illustrated in Fig. 5 by fitting V_t data for the 130 nm technology node [8]. The proposed model shows excellent fits despite of the relatively large RSCE of these devices. As a benchmark, the industry standard model BSIM4 was also fitted to the same data using a single parameter set (no binning), as shown in Fig. 6. The empirical RSCE model of BSIM4 results in a parabolic shape in the log(L) plot and cannot capture the distinct behavior seen in the measured data. Note that this parabolic behavior is also observed between the bin points of Fig. 2, due to the 1/L dependencies of the binning equations.

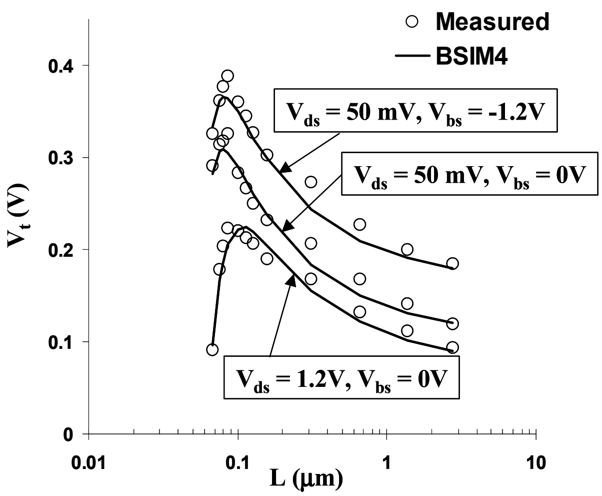

Fig. 6: BSIM4 fits to the same data of Fig. 5. The BSIM4 model does not capture the correct length dependent shape.

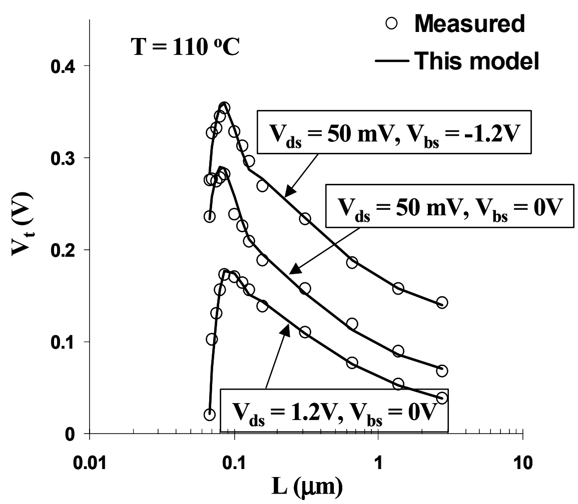

Fig 7: High temperature fit for the same devices of Fig. 5 with no additional temperature parameters for RSCE.

Fig. 7 illustrates the model's physical nature by fitting the high temperature V_t data for the same devices of Fig. 5 with no additional temperature parameters.

The need for different V_t models for I-V and C-V for intermediate size devices is illustrated in Fig. 8. The center device begins to form an inversion layer near V_{gs} = 0, indicated by the increase in gate capacitance, before there is significant current conduction along the channel. Using the same V_t model for I-V and C-V results in large errors in the C-V characteristics, as depicted by the solid lines in Fig. 8. Using the separate equivalent doping model for C-V given in expressions (5) results in excellent fits for the quasi-static C-V, as shown by the dashed lines in the figure.

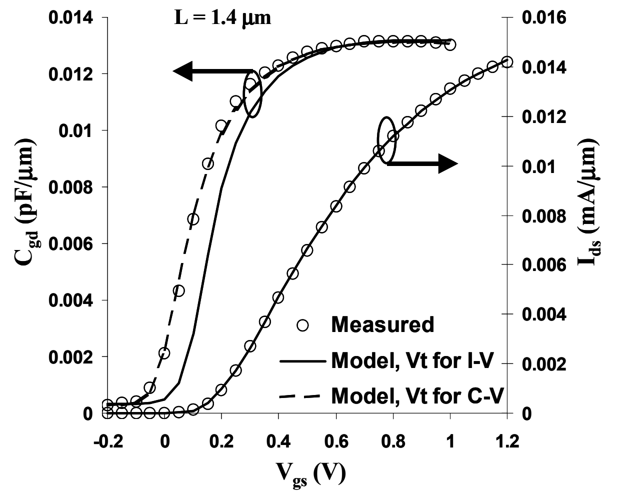

Fig. 8: Fits to linear region current I_{ds} and quasi-static split capacitance C_{gd} for an intermediate size device, illustrating the need for a separate V_t model for C-V.

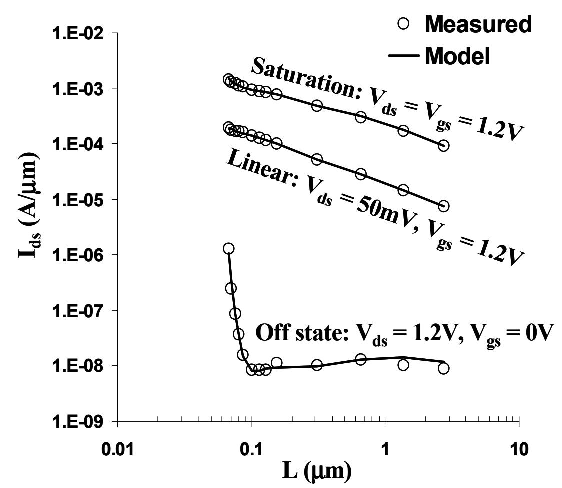

Fig. 9: Compact model fits to linear, saturation, and off-state leakage currents using a single parameter set.

When applied to a physical compact MOSFET model, the proposed approach enables excellent fits for all channel lengths with a single model parameter set. This is illustrated in Fig. 9 by the good fits to the saturation, linear, and off-state leakage currents for a wide range of channel lengths.

4. Beyond the Single V_t Model

The RSCE model discussed in section 2 describes an equivalent V_t (or equivalent channel doping) for halo devices that can be used in standard single V_t (or charge-sheet) compact models. However, just finding an equivalent V_t may not be sufficient to accurately describe the device behavior. Strong halo devices also have peculiar characteristics that present challenges for modeling and characterization. Some of these are discussed below.

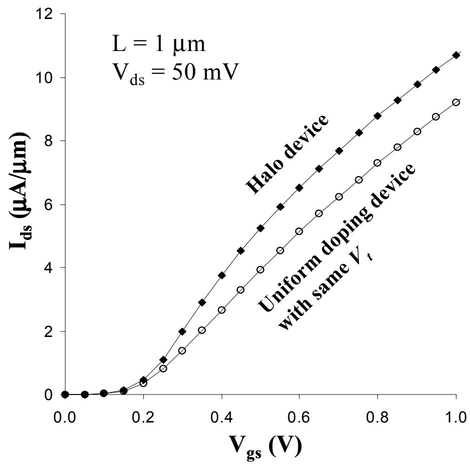

Fig. 10: Simulated linear region characteristics of two devices of same V_t with halo doping (dark symbols) and uniform channel doping (white symbols).

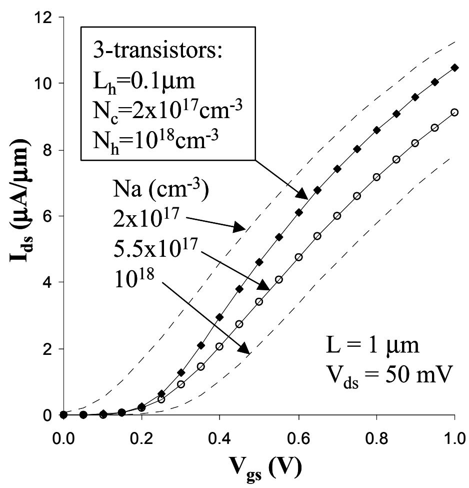

Fig. 11: 3-transistor equivalent used to reproduce and understand the halo effect on the linear current behavior.

A. Device Characteristics

Fig. 10 shows linear region characteristics of two devices with same length and matched V_t, obtained with 2-D device simulations. One device has a non-uniform halo profile while the other has a uniform channel doping. The halo device shows increased peak trans-conductance and higher strong inversion currents. This behavior difference is easily understood by using the 3-transistor equivalent model depicted in Fig. 3. The behavior of the equivalent 3-transistor model, obtained with a circuit simulator, is compared to that of a single device with same V_t. in Fig. 11. The dashed lines represent the two extremes of devices with uniform N_c and N_h dopings, which help clarify the halo effect on the device behavior. The heavily doped halo region impacts the weak inversion, since the device turn-on characteristics is limited by the available carriers in the higher V_t halo region. Once strong inversion sets in, the low doping, low V_t, center region begins to dominate resulting in larger currents than that of a uniformly doped device. The higher currents are simply due to increased gate drive, or reduced channel resistance, in the center region.

This analysis suggests that applying the standard single V_t models to analyze devices with strong halo dopings may lead to incorrect results. A more appropriate analytic model can be derived from the series resistance connection of the three channel regions, assuming strong-inversion condition and constant mobility:

$$I_{ds} = \frac{\mu \cdot C_{ox} \cdot W \cdot V_{ds}}{\dfrac{2 \cdot L_h}{V_{gs} - V_{th} - 0.5 \cdot V_{ds}} + \dfrac{L - 2 \cdot L_h}{V_{gs} - V_{tc} - 0.5 \cdot V_{ds}}}$$

This simple model shows how the higher gate drive $V_{gs} - V_{tc}$ of the center region should result in higher currents. Unfortunately, use of the above expression requires characterization of the parameters L_h, V_{th}, and V_{tc}.

B. Apparent Mobility Enhancement/Degradation

Another implication of Figs. 10 and 11 is that data analysis with standard single V_t models will lead to overestimated long-channel mobility values. On the other hand, the overestimated long-channel mobility will lead to apparent mobility degradation for short-channel devices. Furthermore, mobility extractions based on split C-V techniques become compromised by the different V_t of I-V and C-V (see Fig. 8).

C. Non Quasi-static (NQS) Behavior

Fig. 8 shows the quasi-static or low frequency C-V behavior, where enough time is given for the buildup of inversion charge. At high frequencies or fast gate voltage ramps, the higher V_t of the halo region will have the effect of further damping the formation of the inversion layer.

Conclusion

The simple three-transistor approximation results in a physical compact model for RSCE, enabling accurate V_t fits to all channel lengths with a single model parameter set. Distinct V_t expressions for I-V and C-V are proposed, essential for correct modeling of devices longer than twice the halo characteristic length. In addition, potential implications for the modeling and characterization of devices fabricated with strong halo processes have been discussed.

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