A 90-nm CMOS Device Technology with High-speed, General-purpose, and Low-leakage Transistors for System on Chip Applications

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Abstract

A leading edge 90nm bulk CMOS device technology is described in this paper. In this technology, multi Vt and multi gate oxide devices are offered to support low standby power (LP), general-purpose (G or ASIC), and high-speed (HS) system on chip (SoC) applications. High voltage I/O devices are supported using 70A, 50A, and 28A gate oxide for 3.3V, 2.5V, and 1.5-1.8V interfaces, respectively. The backend architecture is based on nine levels of Cu interconnect with hot black diamond (HBD) low-k dielectric (k<=3.0).

Key Technology Features

The device coverage in terms of off-state leakage, SRAM stand-by, and gate delay for this work is shown in Fig. 1. As can be seen, the ranges off-state leakage 0.003-100nA/μm, SRAM stand-by 0.003-50mA/Mb, and gate delay 7.9-26 ps properly cover the three principal application domains namely LP, G, and HS, respectively. The application domains are separated by at least one order of magnitude in circuit-level leakage. Multiple Vt devices are provided within each domain to added performance-leakage design flexibility. Table II summarizes the 90nm device options. The nominal poly gate length (Lg) and unload ring oscillator (RO) speed for std-Vt G, HS, and LP devices are 65, 45, 80nm respectively. Nominal gate delays of 8.4ps@1.2V, 7.9ps@1V, and 21ps@1.2V are demonstrated for G, HS, and LP device sets respectively. By optimizing STI depth, well implants, and S/D implants, aggressive N+/P+ isolation spacing of 0.16um with n/pMOS junction capacitance (Cjn/p) 0.8/0.95 fF/μm^2 was achieved. Nickel salicide has been evaluated for HS device to (1) ensure good poly resistance for line width down to ~40nm, (2) minimize interfacial S/D resistance, and (3) improve gate activation.

Critical layers use 193 nm photolithography combined with optical proximity correction (OPC), assist features, and phase-shift masks (PSMs) to improve resolution and process window. State-of-the-art patterning and module technology enabled aggressive DRs as shown in Table I. This technology can support various 6T-SRAM cells with size ranging from 0.999 to 1.65 μm^2. The backend employs 9 levels of Cu hierarchical interconnects and HBD low-k dielectric with effective k of <=3.0 [2]. Key design rules are shown in Table I.

CMOS devices were fabricated with super steep retrograde (SSR) indium and arsenic channels, aggressive poly Si gate control, multi-tilted pocket implants, shallow source/drain extensions, and deep source/drain with low junction leakage. Implants are followed by spike anneal process to minimize diffusion. Thermally grown nitrided gate-oxide is followed by un-doped poly-silicon deposition with N+ gate pre-doping and gate patterning. Next, shallow source/drain extensions for core and IO devices, low-thermal budget side-wall spacer, and deep source drains are formed. Modified source/drain implants were adopted to improve activation and junction capacitance while maintaining good SCE. Cobalt salicide is formed with Rsh <=10 Ω/sq for LP and G devices. Nickel salicide is evaluated for HS device with Rsh < 5 Ω/sq for poly-silicon lines as narrow as 40 nm.

Device Design and Performance

A. Isolation

Shallow trench isolation and well profiles are optimized to achieve aggressive inter-well isolation even with triple well process. There is a trade-off between isolation performance and junction capacitance (Cj). To improve N+/NW or P+/PW isolation spacing by 10 nm, Cj need to be increased about 5% due to higher well implant dose for constant STI depth as shown in Fig. 2. By optimizing STI depth, well implants, and S/D implants, 0.16um N+/P+ isolation spacing was achieved as shown in Fig. 3 with low junction capacitance of Cjn/p=0.85/0.95 fF/um^2.

B. Gate Dielectric

It is well known that gate leakage reduction can be attained by increasing levels of nitridation in the gate dielectric. As shown in Fig. 4, carrier mobility can be degraded more than 5%, especially for nMOS, for strong nitridation level. Light nitridation oxide was employed in LP/G devices without sacrificing carrier mobility. On the other hand, strong nitridized oxide is chosen to suppress gate leakage and B penetration in HS device. Aside from mobility degradation described above, strong nitrided oxide

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can also degrade nMOS SCE control due to the presence of nitrogen in the Si, which retards the B halo pile-up near the S/D extension. Therefore, halo implant optimization for the strongly nitrided oxide was needed to recover SCE control as shown in Fig. 5. Reliability is another concern for nitrogen incorporation. Figure 6 shows tha pMOS HCI lifetime can be significantly degraded especially for ultra thin gate dielectrics.

C. Spacer and S/D Engineering

Spacer thermal cycle was further optimized to reduce dopant transient enhanced diffusion (TED). Fig. 7 shows pMOS SCE improvement by the spacer optimization. Low S/D implant energy in modified implant scheme can get defect-free junction without degrading Idsat-Ioff performance. With optimized junction grading implants, low n/pCj was achieved without degrading SCE and n+/p+ isolation.

D. Salicide

Nickel salicide is evaluated for HS device to ensure good poly resistance for line width down to ~40nm. Nickel salicide also improves gate activation and series resistance resulting in I_{dsat}-I_{off} performance improvement (~5%) above $CoSi_X$.

E. Device Performance

A typical sub-nominal G-device crossection is shown in Fig. 8. Device competitiveness is asserted in terms of I_{off}-I_{dsat} and compared to literature data [3-7] as shown in Fig. 9. Short channel effect control for both G and LP devices is shown in Fig. 10. Good SCE control down to minimum L_g of 50 nm for G devices and 65nm for LP devices was demonstrated.

Device I_{dsat} depends on the active width (L_{OD}) along the current flow direction as shown in Fig. 11 due to STI induced stress. Clearly, n/pFET I_{dsat} has +5/-9 % difference from L_{OD}=0.6 to 10 µm. STI process and thermal cycle have to be carefully optimized to reduce the stress effect. In this paper, L_{OD} of 1.36 um is used as the standard test structure. Figures 12(a) and (b) show the output and sub-threshold characteristics for HS devices. Good sub-threshold slope and low drain induced barrier lowering (DIBL) were achieved. Figure 13 shows effect of drain-to-gate overlap capacitance (C_{OV}) reduction on the unloaded ring-oscillator delay at 1 and 1.2 V for G and HS devices.

Performance-leakage tradeoff benefits by substrate biasing have been reported elsewhere [8], Fig. 14 shows the substrate bias sensitivity for G & LP devices. For example, sub-threshold leakage can be reduced via substrate back-bias or block shutdowns. On the other hand, forward body bias can be effectively used to improve performance and reduce leakage power during burn-in and stand-by [8].

F. Reliability

Device hot-carrier reliability, bias temperature stability, and gate oxide time-dependent dielectric breakdown (TDDB) lifetime are verified to have enough margin to support nominal operation up to 1.2V. The G nMOS device DC and AC HCI lifetime is larger than 1 and 50 years for 1.2V operation as shown in Fig. 15. Fig. 16 shows the G/HS intrinsic gate-oxide TDDB at 125° C, which exceeding 10 years for 1.2 V operation.

Conclusion

This paper presented fully manufacturable SoC devices with 9 layers of Cu/HBD interconnects for 90nm CMOS technology applications. Versatile device offering includes high speed (HS), ASIC (G), and low standby power (LP) devices and three different I/O devices. Excellent device characteristics and reliability were obtained.

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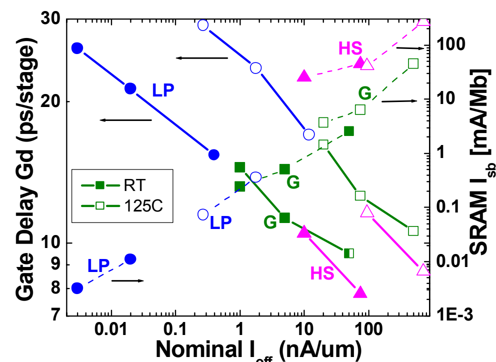

Fig. 1. Performance-leakage-standby space coverage by the LP @ 1.2V, G & HS @ 1V device sets. Dashed lines read on the right axis for SRAM stand-by leakage.

	CL013 (L/S)	CLN90 (L/S)
OD	0.14/0.21	0.11/0.14
PO with CO	0.13/0.38	0.1/0.28
PO without CO	0.13/0.18	0.1/0.14
CO	0.16/0.18	0.12/0.14
M_1	0.16/0.18	0.12/0.12
Inter-Via	0.19/0.22	0.13/0.15
M_{2-7}	0.2/0.21	0.14/0.14
Via_7	0.36/0.35	0.36/0.34
M_8	0.44/0.46	0.42/0.42
Via_8	NA	0.36/0.34
M_9	NA	0.42/0.42

Table I. Summary of key design rules.

TSMC Process	LP			G			HS		I/Os		
	Low-Vt	Std-Vt	High Vt	Low-Vt	Std-Vt	High Vt	Std-Vt	High-Vt			
V_{dd} (V)	1.2			1 (1.2)			1		1.8	2.5	3.3
T_{ox} (nm) [EOT]	22			16			<14		28	~53	~70
L_g (um)	80			65			45/50	50/55	145	265	365
I_{ds} (uA/um)	540/250	420/180	370/130	755/335 (995/460)	640/280 (865/400)	520/215 (750/320)	830/380	670/310	660/300	580/290	580/290
I_{off} (nA/um)	0.4	0.015	0.004	50 (75)	5 (7.5)	1 (1.5)	75	10	<300	<300	<300
J_g (A/um^2)	100p/30p			2.4n/1n (6n/2.4n)			0.3-1u		<5p	<1f	<<1f
C_j (fF/um^2)	1.3/1.2			0.85/0.95							
Inverter delay (ps)	15	21	26	9.5 (8.4)	11.3 (9.5)	14.5(11.6)	7.9	10.5	<23	<32	<42

Table II. Device options in 90nm technology.

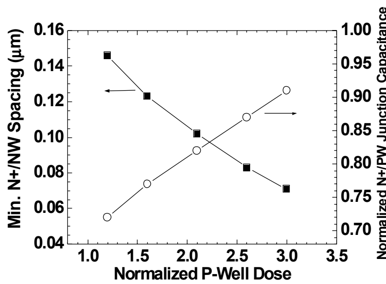

Fig. 2. Isolation and junction capacitance trade-off vs. well implant dose.

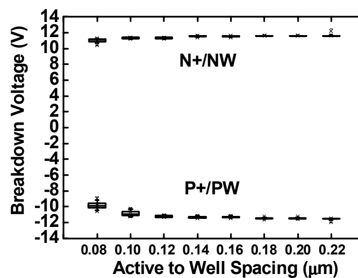

Fig. 3. N+ to NW and P+ to PW inter-well isolation characteristics. Isolation is still safe for spacing down to 80nm.

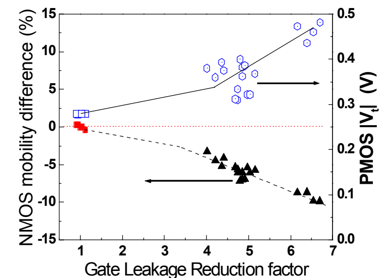

Fig. 4. High-field electron mobility degradation and pMOS Vt shift due to gate oxide with nitridation.

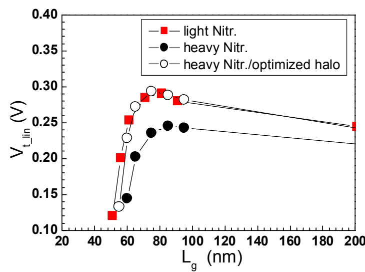

Fig. 5. NMOS SCE is degraded by heavily nitrided oxide. By halo optimization, the SCE control can be recovered.

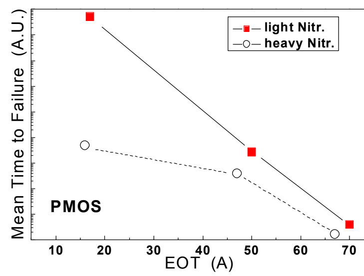

Fig. 6. HCI degradation in strongly nitrided gate dielectric. More severe as EOT scales down particularly for pFETs.

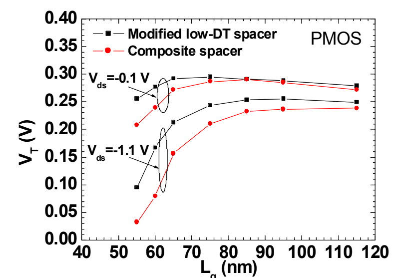

Fig. 7. PMOS SCE control improvement by optimizing spacer thermal cycle.

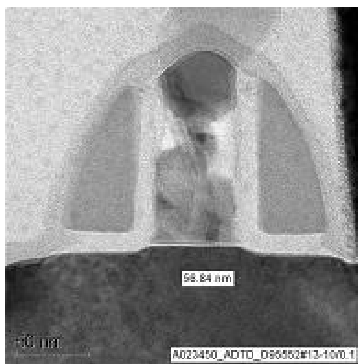

Fig. 8. Representative TEM cross-section of a sub-nominal G-type transistor.

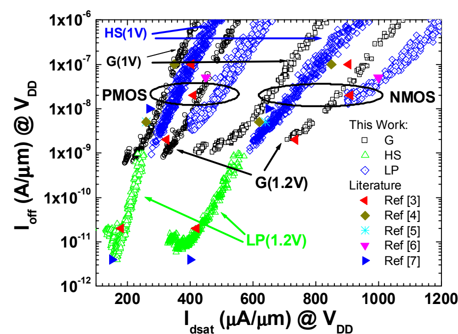

Fig. 9. Device DC performance as I_{off} versus I_{dsat} for G, HS, and LP devices.

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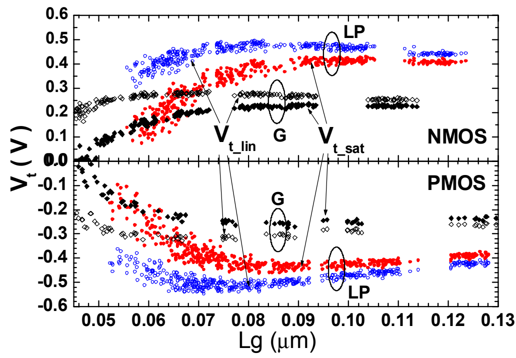

Fig. 10. SCE characteristics for G and LP device sets.

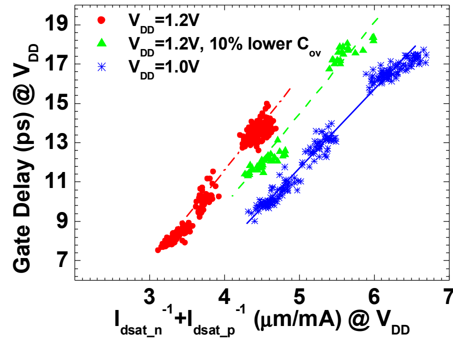

Fig. 13. Unloaded ring-oscillator gate delay of G devices. Overlap capacitance improvement enhances speed significantly.

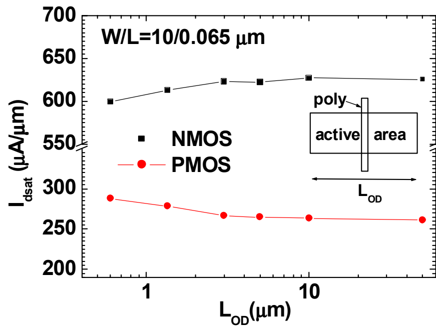

Fig. 11. STI mechanical stress effect on I_{dsat} can be minimized by process optimization.

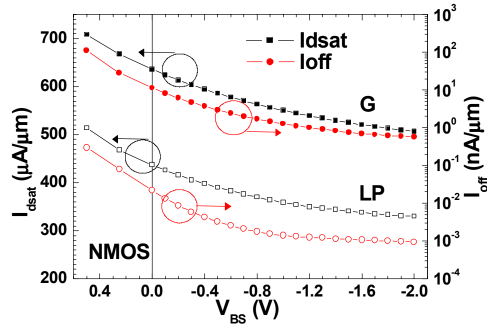

Fig. 14. Back bias effect on I_{dsat} an I_{off}.

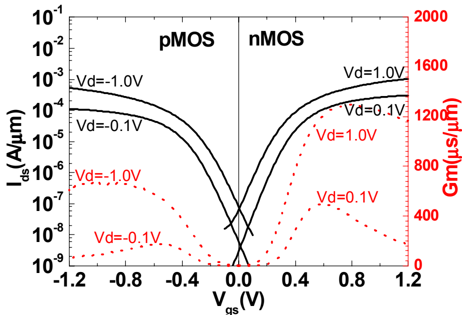

Fig. 12(a). Sub-threshold behavior for 45nm devices

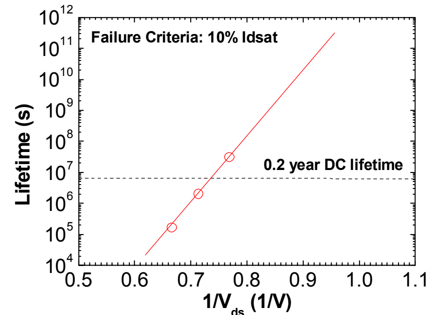

Fig. 15. Hot carrier lifetime for 16 Å G nMOS.

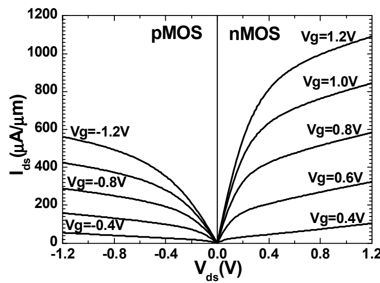

Fig. 12(b). Output characteristic for 45nm devices.

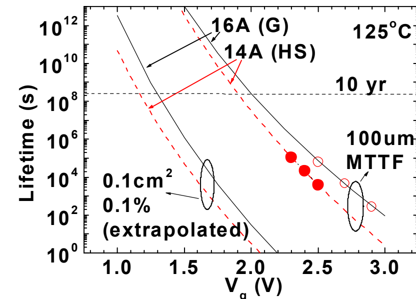

Fig. 16. TDDB lifetime supports 1.2V operation for G devices.

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