Lateral Ion Implant Straggle and Mask Proximity Effect

Terence B. Hook, J. Brown, Peter Cottrell, *Fellow, IEEE*, Eric Adler, Dennis Hoyniak, Jim Johnson, and Randy Mann

***Abstract*—Lateral scattering of retrograde well implants is shown to have an effect on the threshold voltage of nearby devices. The threshold voltage of both NMOSFETs and PMOSFETs increases in magnitude for conventional retrograde wells, but for triple-well isolated NMOSFETs the threshold voltage decreases for narrow devices near the edge of the well. Electrical data, SIMS, and SUPREM4 simulations are shown that elucidate the phenomenon.**

***Index Terms*—CMOS, high energy implanters, lateral ion implant, lateral scattering, NMOSFETs, nwell, parasitic bipolar gain, PMOSFETs, pwell, retrograde well implants, SIMS, SUPREM4 simulations.**

I. INTRODUCTION

RETROGRADE well profiles have several key advantages for highly scaled bulk complementary metal oxide semiconductor (CMOS) technology [1]. With the advent of high-energy implanters and reduced thermal cycle processing, it has become possible to provide a relatively heavily doped deep nwell and pwell without affecting the critical device-related doping at the surface. The deep well implants provide a low resistance path and suppress parasitic bipolar gain for latchup protection, and can also improve soft error rate and noise isolation. A deep buried layer is also key to forming triple-well structures for isolated-well NMOSFETs. However, deep buried layers can affect devices located near the mask edge. Some of the ions scattered out of the edge of the photoresist are implanted in the silicon surface near the mask edge, altering the threshold voltage of those devices. In this paper, we show data of a deep boron retrograde pwell, a deep phosphorus retrograde nwell, and also a triple-well implementation with a deep phosphorus isolation layer below the pwell. Threshold voltage shifts of up to 100 mV can be observed over a lateral distance on the order of a micrometer. TSUPREM4 [2] was also used to illuminate some of the details of the effect.

The phenomenon is shown schematically in Fig. 1. Ions scattered laterally just inside the photoresist edge will be able to emerge from the resist [3]. These may be implanted into the silicon within the area that will become a transistor active-region later in the process. The depth and concentration of the implanted ions will depend on the angle and energy of the scattered ions. The details of the lateral scattering depend on the mass of the incoming ions and the mass of the species in the photoresist from which they are scattered. Whether or not there is a significant effect on the threshold voltage depends on the overall width of the device, the location of the device relative to the mask edge, the lateral range of the effect, and the density and depth of the scattered ions relative to those intentionally implanted in that region. The simulations and data described in the following sections show that a quantitatively significant effect can be observed for dimensions and implants which may be found in typical processes.

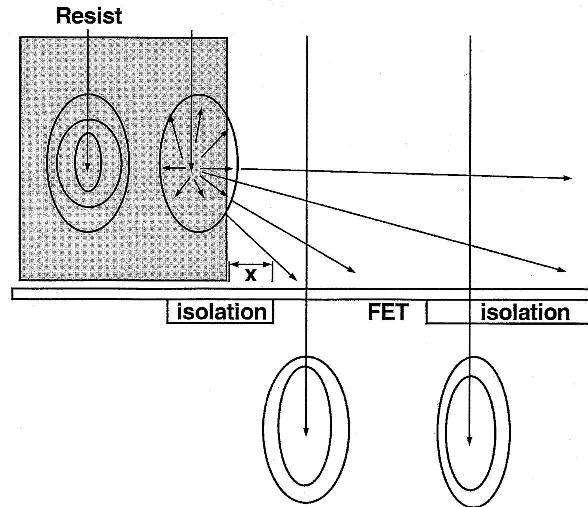

Fig. 1. Schematic representation of mask edge proximity effect.

II. SIMULATION RESULTS

The Monte Carlo implant models available in TSUPREM4 are capable of modeling this effect, and some results of this modeling are shown in Figs. 2–4. Fig. 2 pictures a process with a deep boron implant. The 2.3 μm-thick pwell mask is shown on the left; the region to the right is where NMOSFETs are to be built later in the process. A deep boron retrograde implant implanted normal to the surface at 600 KeV has been performed (see region A in Fig. 2). For this simulation, default implant conditions were used with 500 000 implant trajectories. Minimal heat was applied just to activate the dopant; this was not intended to be a simulation of the full technology parameters. The dopants in region B are scattered out of the photoresist and are implanted into the silicon. Had there been no mask edge, the entire profile would have been as in Region A. It is apparent that this is a long-range effect: for a distance on the order of one micrometer from the mask edge there is excess boron doping near the surface. That dopant near the surface (within the depletion region of the FET) will affect the threshold voltage. As the

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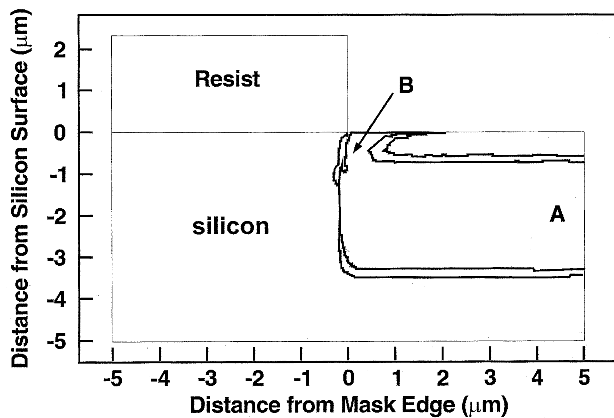

Fig. 2. Contour plot of simulated doping near resist mask edge. Only boron implantation was performed in this simulation. In Region A only the normal deep well profile appears. Excess surface dopant near the resist edge is evident in Region B.

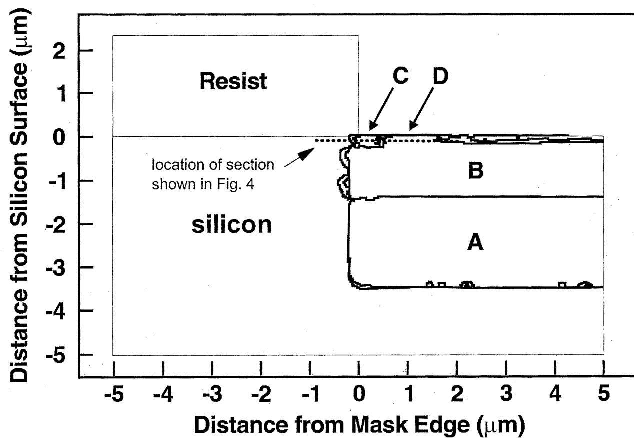

Fig. 3. Contour plot of simulated doping near resist mask edge. Both boron (intermediate and near-surface) and phosphorus (deep) implantations were simulated. Region A is the deep phosphorus implant region. Region B is the isolated pwell area. In Region C there is a small pocket of scattered phosphorus.

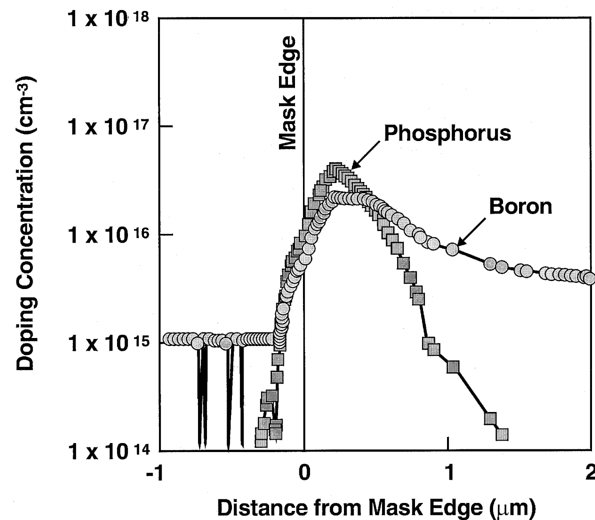

Fig. 4. Simulated lateral doping profiles of B and P immediately below the silicon surface for the implants whose two-dimensional (2-D) contour plot is shown in Fig. 3.

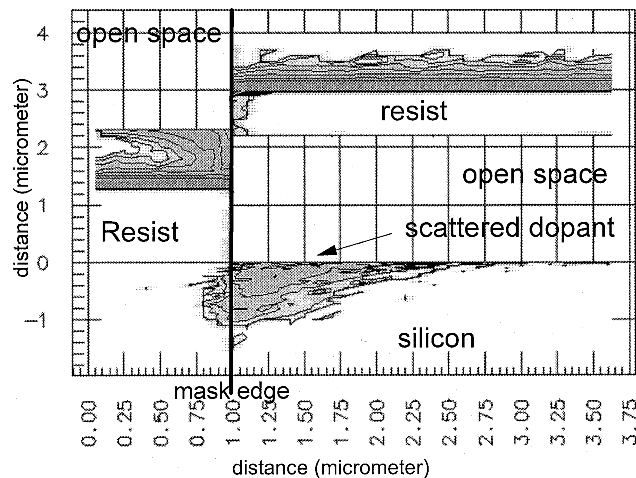

Fig. 5. Simulated dopant profiles of scattered ions using a novel stopping film to eliminate the directly implanted ions from the silicon surface.

typical spacing of NMOSFETs from the mask edge is certainly 0.5 μm or less, the extra implant can cause a substantial increase in the threshold voltage of those devices, particularly when they are one micrometer wide or less.

Fig. 3 illustrates the effect when a deep phosphorus implant is used to form a pwell region isolated from the substrate. In this case, Region A is the buried n-type layer and Region B is the pwell. (In the actual process sequence an additional n-type implant would be performed subsequently to complete the lateral isolation of the pwell region.) Region D is an area where the pwell implant has been scattered out of the resist edge; this increases the threshold voltage in this area. Region C is where the deep phosphorus has been scattered out of the resist, and has inverted the net doping at the surface; the net result is n-type doping in this area. If this were to intrude in the FET channel region, that portion of the channel would have a lower threshold voltage. Fig. 4 shows the lateral concentration profile of both boron and phosphorus near the silicon surface. At 0.5 μm and beyond, the net doping is p-type; but, closer than 0.3 μm to the mask edge, the doping is n-type. The lateral doping profile of the boron is as would be observed in the process of Fig. 2; in this case the phophorus profile is superimposed on the scattered boron, and even inverts the sense of the doping at the surface near the mask edge.

The process by which the implanted ions are stopped in the resist has two phases. When the energy is high, the scattering is largely electronic, and the angle of incidence is changed little. Ions scattered out of the resist by this mechanism retain relatively high energy, and a relatively steep implant angle. If the ions are implanted deeply enough then the threshold voltage will not be affected. As the ions are slowed, nuclear scattering begins to be of greater importance, and the scattered angle is larger. These ions will emerge at a shallower angle and traverse a larger lateral distance and be implanted at a shallower depth. They will have a more significant effect on the threshold voltage. A special simulation was done with the directly implanted ions blocked by a thick layer suspended over the device region, leaving only the scattered ions to be implanted into the silicon. A representative two-dimensional profile is shown in Fig. 5, where the steeply scattered, high-energy ions can be seen closer to the mask edge and the widely scattered, shallow ions extending laterally away from the edge.

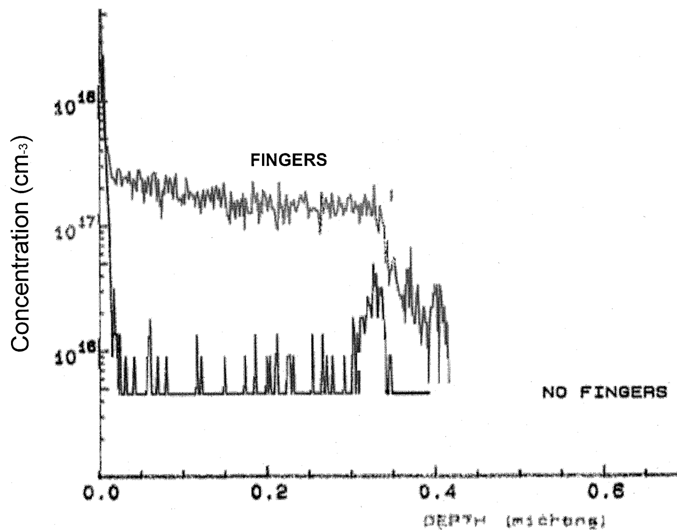

Fig. 6. SIMS profiles of boron concentration in a partially masked region ("fingers") and an unmasked region ("no fingers").

III. Experimental Results

Data from secondary ion mass spectroscopy (SIMS) profiling confirmed the resist-edge proximity effect. In that experiment, wafers were processed with the deep boron well implant at 600 KeV; the photoresist was stripped and the wafers profiled in two different places on the wafer. One location was distant from any pwell mask edge. The other location was in a region of uniform stripes of masking (width two micrometers with one micrometer space). If there were no effect of the mask edges on the doping, then the concentration found in the partially masked second structure would differ from that in the wide open first structure by only a constant factor of one-third. In fact, the boron concentration in the second structure exceeded that in the first structure by at least a factor of ten, to a depth of at least 0.30 μm. The SIMS results are pictured in Fig. 6, which show significant boron concentration near the surface only for the fingered region. For a 600 KeV boron implant energy, the doping at the surface could have come only from the straggle phenomenon described herein.

Transistor test structures were built in a 0.18-μm CMOS technology [4] to demonstrate the scattering effect on threshold. Experimental implant conditions were specifically devised to emphasize the effect. Devices of identical design were placed between mask edges spaced at various distances, from 10 μm down to 0.42 μm. Several lengths and widths of both NMOSFETs and PMOSFETs were employed. The arrangement is shown schematically in the inset in Fig. 7. The variable "X" is the same dimension as pictured in Fig. 1; L and W are the transistor width and length, respectively. Note that in order to eliminate variations in isolation-induced mechanical stress variations, the active area dimensions and proximity to the oxide isolation edges are the same for each of the devices—only the distance from gate edge to well mask was modified. For each of the devices the threshold voltage was measured and compared to the device with the mask edges located at a large distance from the device. Fig. 7 shows the NMOSFET threshold voltage offset for various well-to-device spacing for

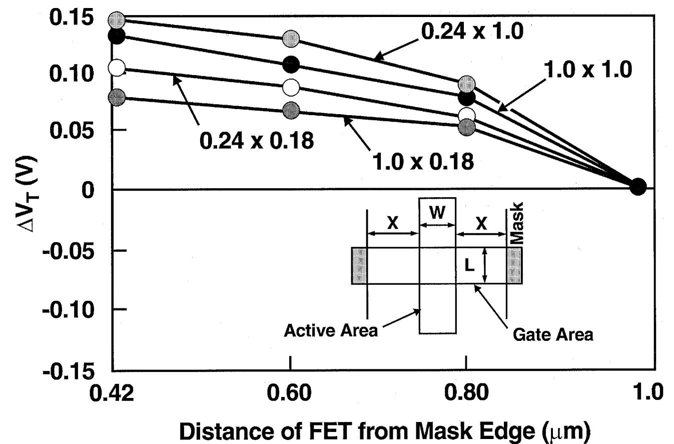

Fig. 7. Difference in threshold voltage between an NMOSFET device located 10 μm from an NW mask edge and devices at various distances. Data from four device sizes are plotted.

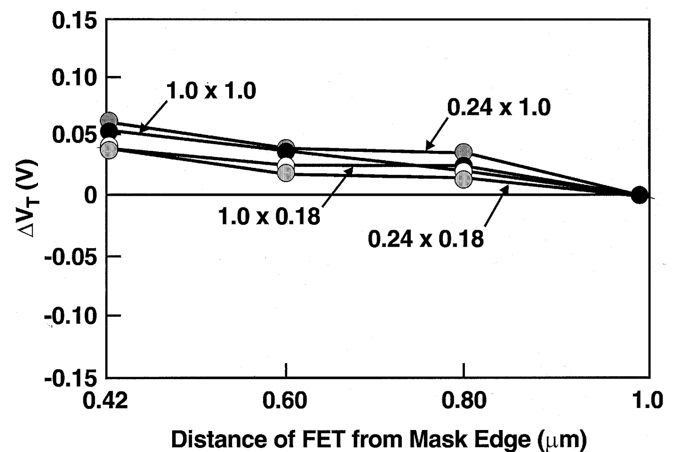

Fig. 8. Difference in threshold voltage between a PMOSFET device located 10 μm from an NW mask edge and devices at various distances. Data from four device sizes are plotted.

four device sizes. The effect is more apparent on narrower and longer devices. The reason for a larger impact on narrow devices is self-evident, but the channel length dependency may be less apparent. The threshold voltage of shorter devices is affected by the halo dose and channel length as well as the well doping. For a minimum length device, the relative contribution of the well doping to the threshold voltage is smaller than for a longer device.

Fig. 8 shows similar data for PMOSFET devices with a deep phosphorus dose. The same trend with width and length is noted here, but the overall magnitude is smaller than for the NMOSFETs.

The effect of the energy of the deep boron implant is shown in Fig. 9. Data for the most sensitive long/narrow device is shown for wafers with different depths but similar total dose. Wafers indicated as A in the figure had a single implant at 360 KeV; those in curve B had two implants; one at 400 KeV and one at 600 KeV, for a total dose nearly the same as in A. The wafers with the shallower implant show a larger proximity effect. This is consistent with simulated results. Two implants of the same dose and different energies were simulated for the same thickness of photoresist. A lateral doping profile immediately below

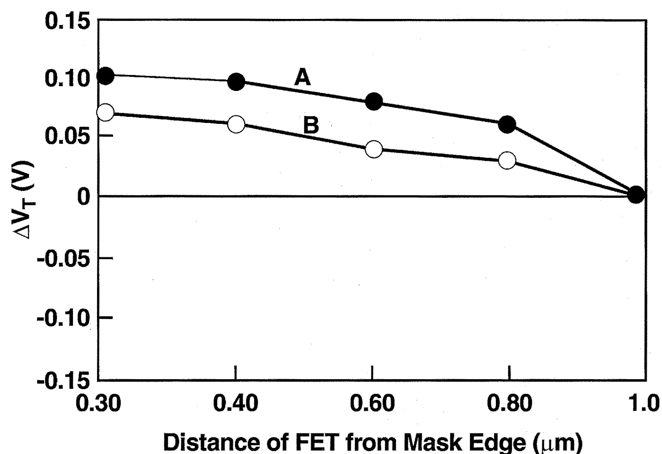

Fig. 9. Difference in threshold voltage between an NMOSFET device located 10 μm from an NW mask edge and devices at various distances. Data from wafers with different implant depths are plotted.

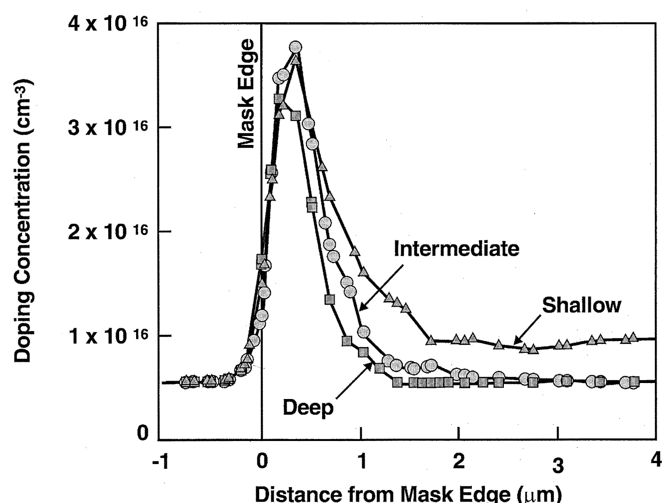

Fig. 10. Simulated lateral doping profiles of B immediately below the silicon surface for implants of three different energies and the same dose.

the silicon surface is shown in Fig. 10. The deeper implant peaks more closely to the mask edge and has less lateral extent. (For the shallowest simulated implant, a portion of the implant appears near the surface, thus altering the baseline doping.)

In some wafers the deep boron implant was completely omitted and a deep phosphorus implant substituted. (When combined with a ring of n-type junction isolation, this structure allows the pwell to be independent of the wafer bulk.) Fig. 11 shows the NMOSFET proximity effect observed in that experiment. The medium-energy boron for the pwell implant causes the threshold to be larger for devices located 0.60 μm or more from the well edge, but for devices at 0.42 μm from the well edge the deep phosphorus begins to compensate the pwell and reduces the threshold voltage, although it does not become smaller than zero. This result agrees with simulation. Referring to the simulated lateral profile in Fig. 4 absolute compensation (i.e., formation of an n-type channel at the device edge) is not anticipated until the well-to-device spacing is less than 0.30 μm for these implant conditions.

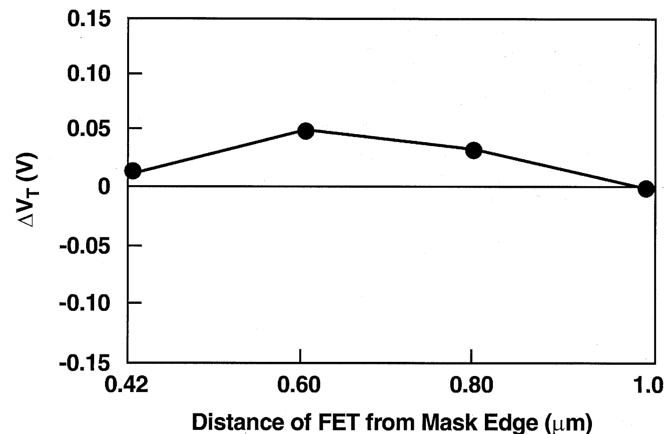

Fig. 11. Difference in threshold voltage between an NMOSFET device located 10 μm from an NW mask edge, and devices at various distances. Data from wafers with a triple-well deep phosphorus implant are plotted.

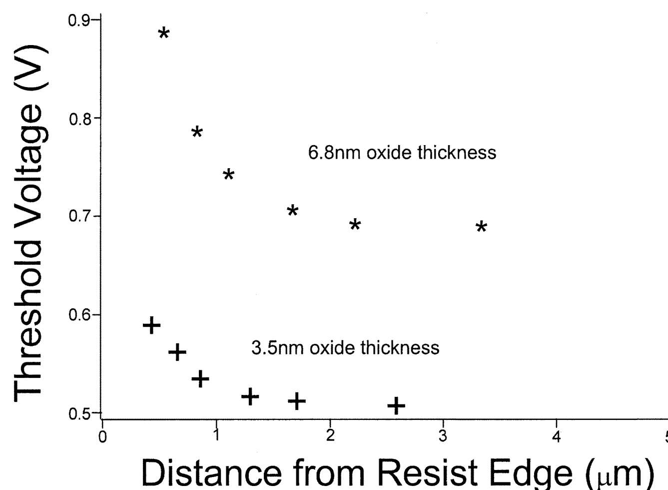

Fig. 12. Threshold voltage for thin (3.5 nm) and thick (7.0 nm) oxide devices as a function of distance from a nearby well mask edge.

The threshold voltage of devices with thicker gate oxide is more affected than thinner oxide devices by the same scattered dopant. The two curves in Fig. 12 compare the threshold voltage shift as a function of well edge distance on thick (6.8 nm) and thin (3.5 nm) oxide devices on the same wafers, with the same well implants. The change in threshold voltage in this particular example is nearly 100 mV for the thinner oxide device, and twice that for the thicker oxide device.

IV. Potential Impact in Designs

In static RAMs and low-power designs with narrow devices, many of the transistors on the chip are close to the well mask edge, and these effects may be important if care is not exercised in setting the transistor sizes. In analog designs, threshold differences that are insignificant to digital circuit functionality and performance may be important.

In static RAMs the scattering effect may be naturally beneficial, reducing the leakage current in SRAM cells where performance is not of paramount importance. An unintended result may be the disruption of the intended relationship of the currents among the different devices in the cell. Often the pulldown

NMOSFETs are placed in closer proximity to the well mask edge than the wordline transfer gate, and the lateral dopant scattering will affect these two devices differently. The ratio of their currents is typically referred to as the "beta" of the cell, and is a critical design parameter affecting cell stability. The scattering effect described here must be taken into account to determine the actual cell beta. For dual-well technology, the cell beta will be lower than might otherwise have been expected as the threshold voltage of the pulldown device will be increased by the scattered dopant to a greater degree than the more distant transfer device. This has an adverse effect on the stability and performance of the cell, and must be taken into account when establishing the device sizes.

Logic gates that drive light loads and those intended for low-power usage are generally quite narrow, often being at the minimum allowable design width, and certainly at less than 0.5 μm in 0.13-μm designs. An unusually high threshold voltage may be the result in these structures, resulting in reduced performance.

Analog circuits often require precise matching of the threshold voltage of two or more transistors. Layout techniques such as common-centroid designs are often used, and it is commonplace to presume that the local density of critical images such as the gate conductor must be identical to obtain the optimal matching. To mitigate the effects described here, it is also necessary to design such that the same proximity effect occurs in devices that one wishes to match most precisely.

For triple-well structures in the dimensions found in 0.13-μm and 0.10-μm technologies, compensation of the well may take place at the device edge. This essentially exacerbates the inverse narrow-channel effect. In contrast to LOCOS-isolated technologies, shallow-trench isolated technologies generally experience a reduction (in magnitude) of threshold voltage for narrow devices. As shown in Figs. 3 and 11 the deep n-type implant compensates the NMOSFET surface doping, and for spacing typical of the 0.10-μm generation may even invert the sense of the doping at the surface.

V. CONCLUSION

We have shown that the implanted ions scattered out of the edge of a photoresist mask can have an important effect on devices as far away as a micrometer. The experimental results are in qualitative agreement with the expectations from SUPREM4 simulation. For a given mask thickness medium-energy implants have a large lateral range on the order of one micrometer; deeper implants show less lateral dispersion. In the case of simple dual-well structures, the threshold voltage of narrow devices near mask edges is larger in magnitude than those remote from the mask, but for triple-well structures the effect may be opposite. The magnitude of the threshold voltage perturbation is directly proportional to the gate oxide thickness.

The data and simulation presented here discuss the influence on the threshold voltage of deep retrograde well implants, but the same phenomenon in principle exists for any sort of retrograde implant; that is, an implant wherein the surface concentration is intended to be less than the concentration at a depth below the surface.

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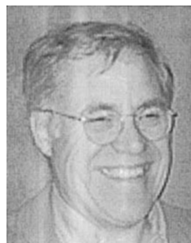

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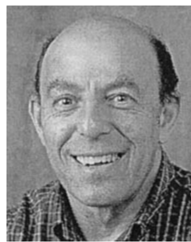

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