IEEE WMED 2010 Technical Program

Friday, April 16th, 2010 8:00AM-7:00PM

8:00AM	Check In and Door Registration *Continental Breakfast in Jordan-D*
8:30AM	Welcome to WMED2010 *Jordan-D Ballroom*
8:45AM	Invited Talk: "CeNSE: The Central Nervous System for the Earth" *Dr. Peter Hartwell, Hewlett-Packard Labs, Palo Alto* *Jordan-D Ballroom*
9:45AM	Break & Poster Setup
10:00AM	Invited Talk: " Challenges and Innovations in Nano-CMOS Transistor Scaling" *Dr. Ghani Tahir, IEEE Fellow, Intel Corporation* *Jordan-D Ballroom*
11:00AM	Invited Talk: "Challenges and Opportunities Moving from 2D to 3D Chips" *Dr. James Lu, RPI* *Jordan-D Ballroom*
NOON	Buffet Luncheon *Provided by the Workshop* *Jordan-AB*
1:00PM	Invited Talk: "Hydrogenated Silicon (Si:H) Thin Film Solar Cells" *Dr. C.R. Wronski, Penn State University.* *Jordan-D Ballroom*
2:00PM	Invited Tutorials Tutorial A: "The title of this tutorial here", Jordan-D *Dr. Banerjee Kaustav* Tutorial B: "Practical Semiconductor Reliability": Jordan-C *Dr. Todd Marquart, Micron Technologies* *(Tutorials are two hours and simultaneous)*
4:00PM	Break
4:15PM	Paper Sessions Process and Devices: Jordan-D Solid State Circuits: Jordan-C *(Sessions are simultaneous)*
5:45PM	Poster Presentation and Reception *Jordan-D Ballroom*

This workshop is receiving technical co-sponsorship support from the IEEE Electron Device Society

Contributed Talks: Parallel Sessions (4:15PM-5:45PM)

Process and Devices Session

4:15p. . . . . Modified Floating Gate and IPD Profile for Better Cell Performance of Sub-50nm NAND Flash Memory
Jennifer Lequn Liu, Fernando, and Y. Jeff Hu, Micron Technology, Inc., Jixin Yu, Charan Srinivasan, Ervin Hill, Intel Corporation

4:30p. . . . . Study of Carrier Mobility of Low-Energy, High-Dose Ion Implantations using Continuous Anodic Oxidation Technique/Differential Hall Effect (CAOT/DHE) Measurements
Shu Quin, Y. Jeff Hu, Allen Mcteer, Si Prussin, Jason Reyes, Micron Technology, Inc.

4:45p. . . . . Discrete Test Structure Device Degradation Analysis and Correlation to NAND Flash Circuit Operation.
Jasper Gibbons, Puneet Sharma, Steve Porter, Jim Fulford, Praveen Vaidyanathan, Sheryll De Guzman, Pratap Murali, Micron Technology, Inc.

5:00p. . . . . A Comprehensive Study on Nanomechanical Properties of Various SiO_2-based Dielectric Films.
Guohua Wei, Song Varghese, Kevin Beaman, Irina Vasilyeva, Tom Mendiola, Andrew Carswell, David Fillmore, and Shifeng Lu, Micron Technology, Inc.

5 :15p. . . . . A Novel Depletion Mode High Voltage Isoloation Device
Vladimir Mikhalev, Michael Smith, Micron Technology, Inc.

5:30p. . . . . Atomistic Study of Ultra-scaled Electron and Hole SiGe Nanowire FETs
Abhijeet Paul, Saumitra Mehrotra, Methieu Luisier, Gerhard Klimeck, Purdue University

Circuits Session

4:15p. . . . . Continuous-Time/Discrete-Time (CT/DT) Cascaded Sigma-Delta Modulator for High Resolution and Wideband Applications
Ali Mesgarani, Suat U. Ay, University of Idaho, Khosrow H. Sadeghi, Sharif University of Technology.

4:30p. . . . . All digital Multiplying DLL Using Precision Digital Delay Line as DCO
Seong-Hoon Lee, Micron Technology, Inc.

4:45p. . . . . Main Memory with Proximity Communication, A Wide I/O DRAM Architecture
Qawi Harvard, R. Jacob Baker, Boise State University, Robert Drost, Sun Microsystems Laboratory

5:00p. . . . . A Low Noise Low Power DC Coupled Sensor Amplifier with Offset Cancellation
Hari Krishnan Krishnamurthy, Dirk Robinson, Dave M. Rector, Geroge S. La Rue, Washington State University.

5:15p. . . . . Integration of a New Column-Parallel ADC Technology on CMOS Image Sensor
Fan Z. Nelson, Suet U. Ay. University of Idaho

5:30p. . . . . Gain Error Correction for CMOS Image Sensor using Delta-Sigma Modulation
Kuangming Yap, R. Jacob Baker, Boise State University

Poster Session

5:45p. . . . . Enhanced Optical Transmission in Hexagonal Plasmonic Crystals
A. English, L. Lowe, and W. Kuang, Boise State University

A Compact Delay-Locked Loop for Multi-Phase Non-Overlapping Clock Generation
Chris Gagliano and R. Jacob Baker, Boise State University

A 16-bit 500KSps Low Power SAR ADC
Kun Yang and George S. La Rue, Washington State University

Design of an On-Chip Quasi-Resonant Fixed Frequency Buck DC-DC Power Converter
Lucas A Wells, University of Idaho

Method of determination pattern placement errors (PPE) due to scanner lens aberration by using product circuit pattern with double patterning technology
Maiko Uemura and Masato Shinohara, Micron Japan, Nishiwaki City, Hyogo, Japan

Using Gate Voltage Sensitivity to Analyze Bvdss in NAND Periphery RESURF Devices
Michael A. Smith, Micron Technology Inc

Damage Engineering of Boron-Based Low Energy Ion Implantations on USJ Fabrications

Shu Qin, Y. Jeff Hu, and Allen McTeer, Micron Technology Inc.