IEEE Components, Packaging and Manufacturing Technology Society
Phoenix Chapter

Tuesday, September 19th, 2006 Tutorial Meeting

Failure Analyses for Electronic Packaging

Dr. Jonathan Harris, President, CMC Interconnect Technologies, Tempe, Arizona
Mr. Ken Tylor, Manager, Sonoscan, Inc., Scottsdale, Arizona
Dr. Dev Gupta, CTO, APSTL, Scottsdale, Arizona
Dr. Rajen Dias, Principal Engineer, Intel Corporation, Chandler, Arizona

Tutorial Scope

Introduce basic methods, tools and techniques of failure analyses practiced in microelectronic packaging. Present applications in Flip Chip Interconnect, Pb-free solders, High Performance Processor Packaging, and Ceramic & Plastic Packaging. Discuss failure modes, mechanisms and resolutions in these application areas. Look beyond the limitations of current day's tools and techniques to address the needs of next generation interconnect and package technologies.

Tutorial Agenda

12:00 – 12:50 PM	Registration
12:50 PM – 1:00 PM	Welcome Address by Dr. Mali Mahalingam and Dr. Daniel Lu
1:00 PM – 2:00 PM	How Interfacial Structure Can Play a Major Role in Packaging Reliability *Dr. Jon Harris, CMC Interconnect Technologies*
2:00 PM – 3:00 PM	Introduction to Acoustic Micro Imaging and Its Applications *Mr. Ken Tylor,* Sonoscan, Inc.
3:00 PM – 3:30 PM	Refreshment Break
3:30 PM – 4:30 PM	Failure Analyses for Flip Chip Packages *Dr. Dev Gupta, APSTL*
4:30 PM – 5:30 PM	Next Generation Analytical Tools for Package Failure Analysis *Dr. Rajen Dias, Intel Corporation*
5:30 PM – 5:45 PM	Tutorial Wrap-Up

Tutorial Abstracts

How Interfacial Structure Can Play a Major Role in Package Reliability?
Dr. Jon Harris, CMC Interconnect Technologies

This talk will investigate the general role of interfacial microstructure on the reliability of package construction. Specifically, the talk will focus on the role of intermetallic compound morphology in determining failure modes when mechanical stress is applied to the package. Methods for delineating interfacial structures will be discussed, including cross-sectional SEM and optical microscopy. Examples of the controlling effect of interfacial microstructure will be given from ceramic and plastic packaging technologies. The role of Pb-free solders on intermetallic compound formation will also be described.

Introduction to Acoustic Micro Imaging and Its Applications
Mr. Ken Tylor, Sonoscan, Inc.

Ultrasound is a form of mechanical energy and is, therefore, sensitive to the elastic properties of the materials it travels through. It is particularly sensitive to locating air gaps (cracks, delaminations and voids). Acoustic Micro

Imaging (AMI) uses high frequency ultrasound (5 – 300MHz) to image internal features and characterize physical defects that occur during the manufacturing process or environmental stress. This presentation will provide an overview of the basics of ultrasound, how it is used for Acoustic Imaging, and explores a variety of applications (including: plastic encapsulated ICs, power devices, flipchips, MLCCs, etc.). It will also cover the role of AMI in industry standards, current developments, and future advancements.

Failure Analyses for Flip Chip Packages
Dr. Dev Gupta, APSTL

Flip chip packaging is now pervasive for high performance processors and is spreading into the less critical but yet larger volume Portable Electronics applications. As this once robust high end technology has to adjust to changes in materials sets (low – k, Pb – free,..) and undergoes cost cutting in order to expand its applications, reliability issues and failure analyses need to be revisited. Failure and Root Cause Analyses during Package Qualification as well as Field Failures play a crucial role in building confidence for outsourced manufacturing. Failure Analyses can be more effective when the Analyst understands typical vulnerabilities of a technology. This presentation covers both fundamentals of Flip Chip packaging as well as successful approaches to Failure Analyses.

Next Generation Analytical Tools for Package Failure Analysis
Dr. Rajen Dias, Intel Corporation

Advanced packaging solutions for high performance microprocessors involve use of multi-level interconnections, shrinking geometries and improved thermal solutions. These trends together with the introduction of low k dielectrics and Cu metallization in next generation Si technologies and new package substrate materials has resulted in severe die/package thermal - mechanical mismatch concerns. Packaging solutions for non CPU applications such as memory, chip sets, networking and communication chips are driven by miniaturization, stacked die for increase in functionality and Pb free applications.

Understanding the defect and intrinsic failure mechanisms during the development and certification of these new package technologies is becoming extremely difficult and time consuming using traditional approaches to failure analysis. Non destructive methods to detect the onset of these mechanisms are critical to time to information in the current era of rapidly shrinking development cycles. This talk will discuss the unique challenges faced by the failure analyst and will focus on advancements in three nondestructive tools – Scanning SQUID microscopy for detecting shorts, 3D x-ray radiography/tomography for imaging various levels of interconnections and scanning acoustic microscopy for detecting interfacial delamination and defects. In addition, novel analytical tools such as Laser Spallation for understanding interfacial adhesion and Laser milling for package delayering and microsurgery will be introduced.

Speaker Biographies

Dr. Jonathan Harris has played a leadership role in the advanced ceramic materials and electronic packaging industry over the past 20 years. Dr. Harris is currently the President of *CMC* Interconnect *Technologies*, a materials analysis and consulting firm which focuses on the electronic interconnect industry. CMC provides a range of technology services including materials characterization, failure analysis, device/package deprocessing, and technical market analysis. CMC's clients include Fortune 100 device manufacturers and advanced materials companies. Prior to founding *CMC Interconnect Technologies* in 2003, Dr. Harris was President of *CMC Wireless Components*, a high thermal performance ceramic packaging company which served the telecommunications, optics, and medical industries. Dr. Harris received his doctorate in Solid State Physics from Brown University (Providence, RI) in 1983. He is the author of over 50 publications and book chapters and has 20 US Patents.

Dr. Jonathan Harris, President, CMC Interconnect Technologies
7755 S. Research Drive, Suite 115, Tempe, AZ 85284
Tel: (480) 496-5120 Email: jharris@cmcinterconnect.com

Mr. Ken Tylor holds a Bachelor of Science degree in Physics from Wheaton College in Wheaton, Illinois. He started with Sonoscan in 1989. During his nine years at the corporate office in the Chicago area, he was involved in various aspects of the laboratory and instrument quality assurance. He was also part of the team opening Sonoscan's first off-site laboratory in San Jose, California. In 1998 Ken moved to Phoenix, Arizona, to start up and manage Sonoscan's second branch laboratory, supporting customers in the southwest region of the country.

Ken Tylor, Analytical Testing Laboratory Manager, Sonoscan, Inc.
7585 E. Redfield Road, Suite 106, Scottsdale, AZ 85260
Tel: (480) 342 – 9400 Email: SSW@Sonoscan.com

Dr. Dev Gupta is an industry recognized expert in Advanced Packaging who regularly teaches Professional Development Courses at IEEE organized international conferences and contributes to industry publications. As a Material Scientist Dr. Gupta has been deeply involved in applying modern failure analyses techniques to the package technologies he has worked on. Since the late '80s Dev has been involved in pioneering the development of key Flip Chip packaging technologies at Motorola. Later at Intel he solved key technological bottlenecks to volume production of organic substrates and managed the design & start up of the original factories for same in Japan. At APSTL, a company engaged in developing and licensing flip chip and wafer level packaging technologies for low cost applications like mobile phones, Dr. Gupta has developed technologies for electroless nickel and column bump flip chip processes and managed turnkey engineering of same at customer fabs in both the US and Far East.

Dr. Dev Gupta, Chief Technology Officer, APSTL, Scottsdale, Arizona
Phone: (480) 540-3232 Email: apstl@az.rmci.net

Dr. Rajen Dias graduated with a Bachelor of Science degree in Metallurgy and Material Science from Indian Institute of Technology, Madras, India, and an MS and Ph.D. in Material Science at Lehigh University. He worked at Intel Corporation for 21 years in the assembly technology development Quality & Reliability department. His areas of focus have been understanding failure modes and mechanisms in new packages, training failure analysts corporate wide and responsible for developing the next generation analytical tools and techniques for package failure analysis.

Dr. Rajen Dias, Principal Engineer, Intel Corporation, Tempe, Arizona
5000 W. Chandler Blvd., Mail Stop: CH5-263, Chandler, Arizona - 85226
Phone: (480) 554-5202 Email: rajen.c.dias@intel.com

Date:	Tuesday, September 19th, 2006
Location:	Amphitheater (Located in Third Floor) Hilton Phoenix Airport, 2435 South 47th Street, Phoenix, Arizona - 85034 Tel: (480) 894-1600; Website: www.phoenixairport.hilton
Time:	12:00 PM – 12:50 PM Registration 12:50 PM – 5:45 PM Program 3:00 PM – 3:30 PM Refreshment Break
Cost:	$15 for IEEE members / $25 for Non-IEEE Members (Includes Tutorial Material and Refreshments)
Registration:	www.ieee.org/phoenix
Audience:	IEEE members and non-members all are welcome to attend.

For more information please call any of the following officers:

Mali Mahalingam (480) 413-5368
Vivek Gupta (480) 554-2195
Vladimir Noveski (480) 554-2375
Vasu Atluri (480) 554-0360
Debendra Mallik (480) 554-5328
Rao Bonda (480) 413-6121
Daniel Lu (480) 552-2909
Victor Prokofiev (480) 552-0228
Jim Drye (480) 413-3604

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Tutorial Registation at www.ieee.org/phoenix

TUTORIAL LOCATION DETAILS

Hilton
Phoenix Airport

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is located at
2435 South 47th Street
Phoenix, Arizona 85034

West of 143 Freeway and North of University Drive

For Further Assistance Call
(480) 894-1600