Session 15 – Design Foundations for Advanced Technologies

Analog/Mixed-Signal Design Challenges in 7-nm CMOS and Beyond

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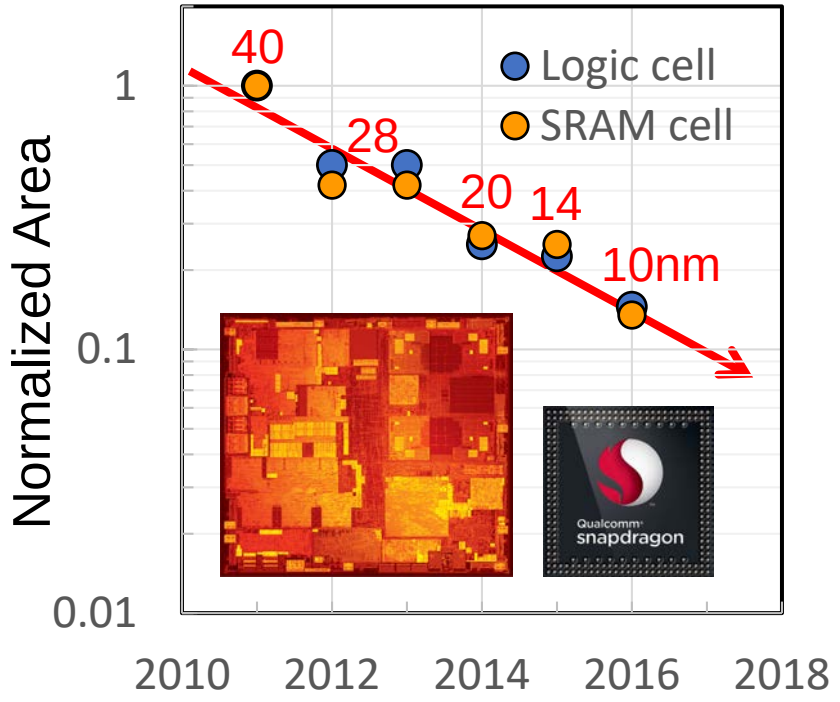
Mobile SoC – Main Driver for CMOS Scaling

- 7nm smartphone products imminent
- SoC technology driven by economics of logic & SRAM scaling
- New node feasible with enough PPAC (Power/Performance/Area/Cost) benefit
  - Incremental feature size reduction
  - Extensive logic & SRAM DTCO
- AMS (Analog/Mixed-Signal) ubiquitous
  - PLLs, wireline I/Os, ESD, regulators, data converters, bandgap references
  - AMS device palette slaved to logic



Outline

- Introduction
- Technology Scaling Enablers
- AMS Device Palette
- AMS Design Impact
- Concurrent Technology/Design Development
- Conclusion

Outline

- Introduction
- **Technology Scaling Enablers**
  - **FinFET**
  - **Lithography & Self-Aligned Patterning**
  - **High-*K* Gate Dielectric & Metal Gate (HKMG)**
  - **Mechanical Stressors**
  - **Middle-End-Of-Line (MEOL)**
- AMS Device Palette
- AMS Design Impact
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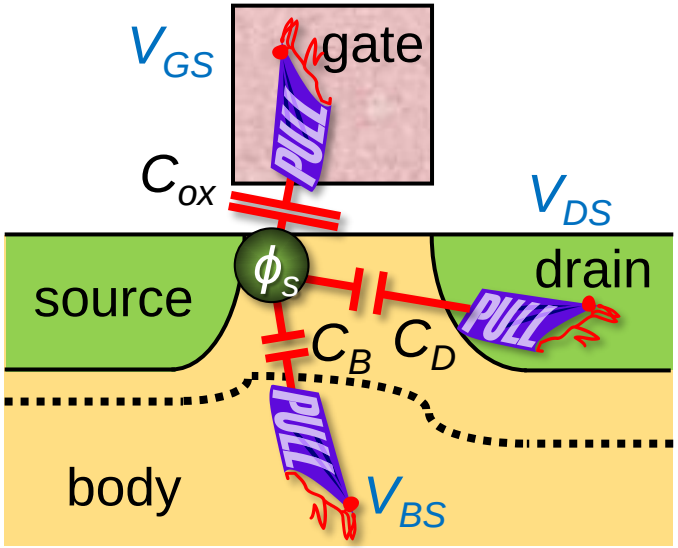
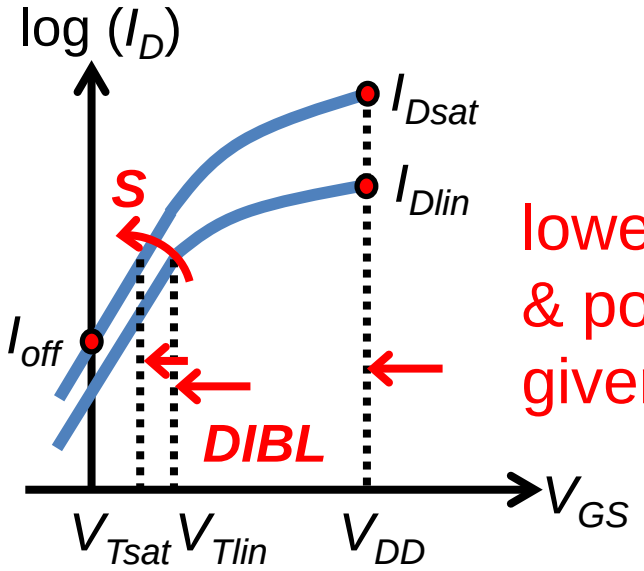
Stronger Short-Channel Gate Control

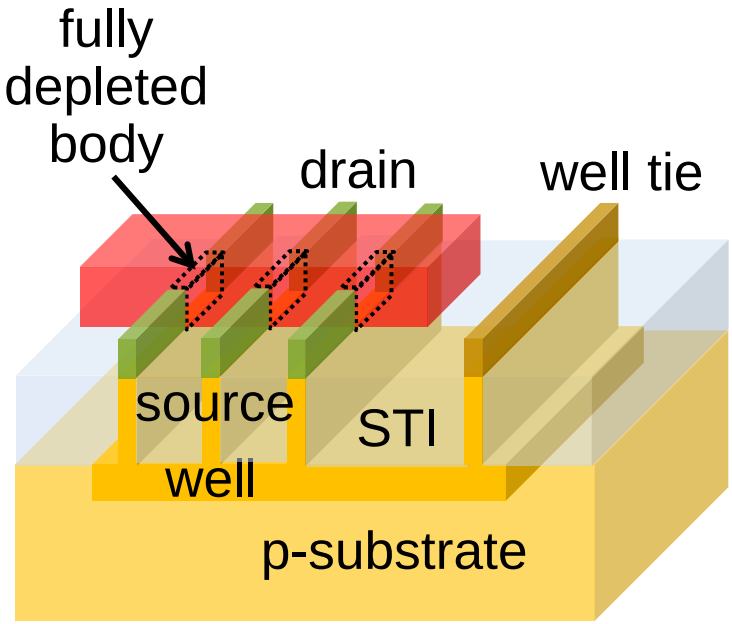




lower supply & power for given I_{on} & I_{off}

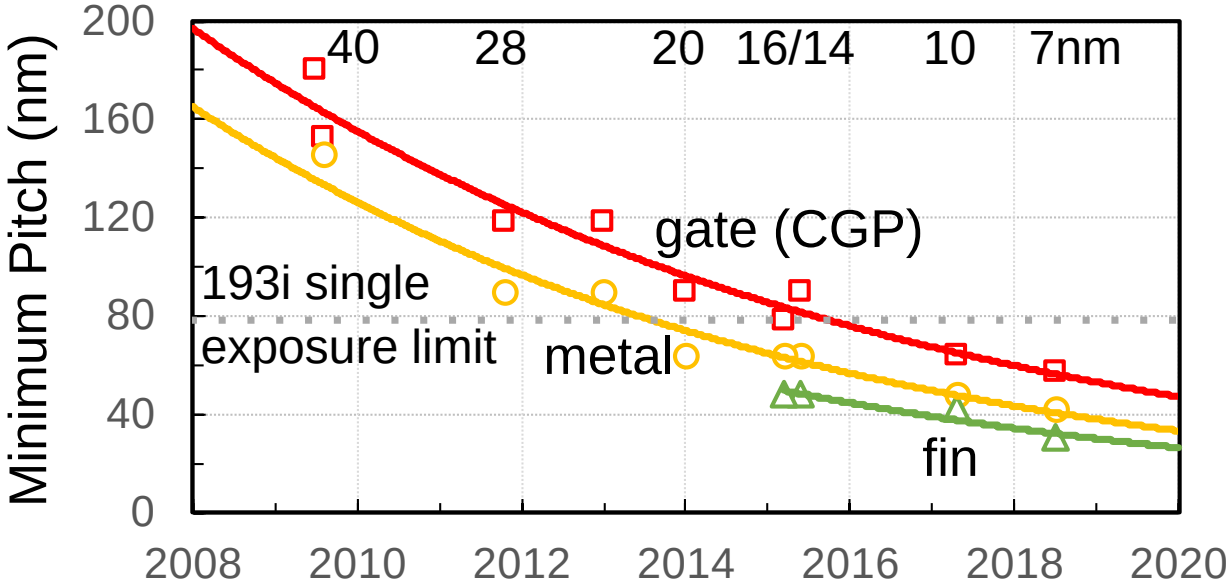
- Subthreshold controlled by C_{ox} vs. (C_B+C_D)
- Fully-depleted finFET weakens C_B & C_D → less *S*, *DIBL* & body effect

Fully Depleted Tri-Gate FinFET



- More I_{on} & g_m per area
- Quantized channel width
- Less DIBL → higher r_{out}, 3× intrinsic gain
- Negligible body effect ($\Delta V_T < 10mV$)
- Less RDF mismatch
- Parasitics
  - High S/D resistance → big deal
  - High S/D coupling to gate
  - Fin width << fin pitch → low C_j, high R_{well}

Foundry Pitch Scaling

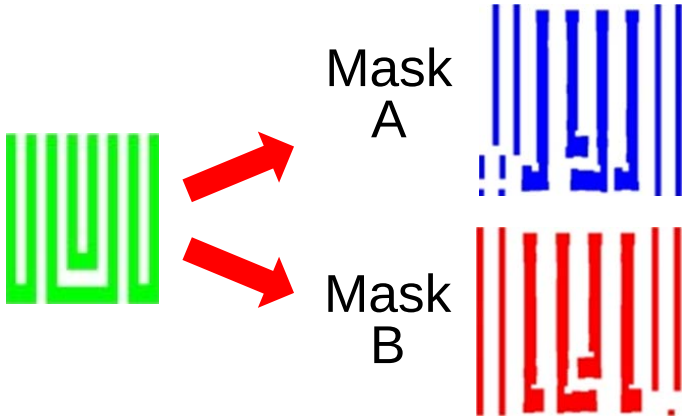


- Scaling rate slower than 0.7x per node → node name = PPAC marketing
- EUV late, only started at 7nm → process complexity for sub-80nm pitch

Lithography Innovations

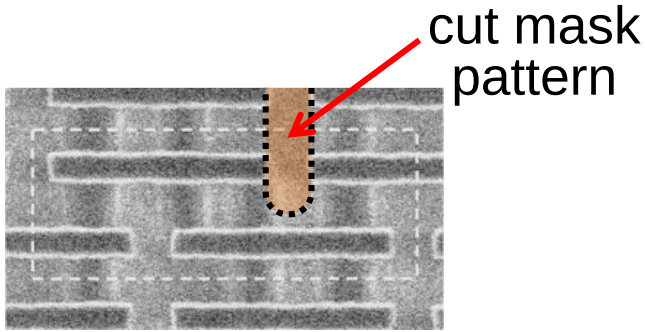
Pitch splitting (LELE)

- Interleave single exposures
- Mask color decomposition & balance
- Extendible to LELELE
- Limited by overlay between masks



Orthogonal cutting

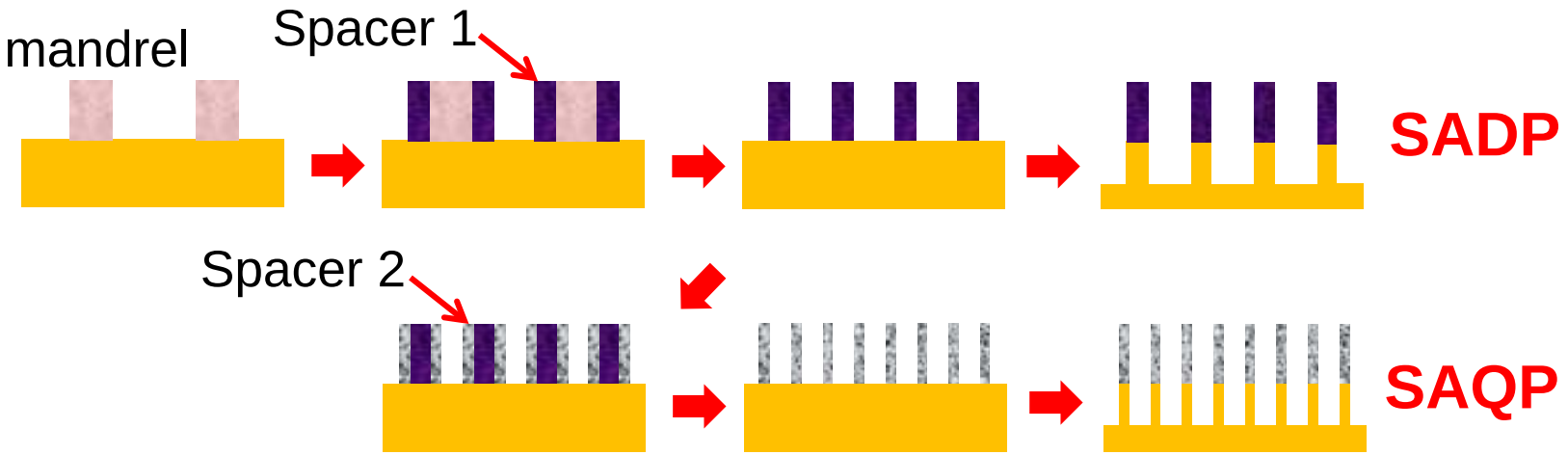
- Extra mask(s) to break line patterns
- Reduced end-to-end spacing
- Limited by overlay in very tight pitch



Arnold *et al.*, ASML [11]
Auth *et al.*, Intel [12]

Spacer-Based Patterning

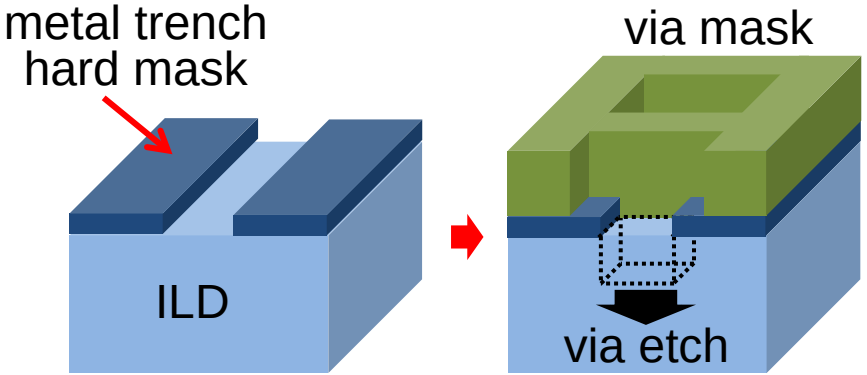
- Pattern fins; now common for gate, MEOL & lower BEOL
- Conformal spacer → correlated LER → less width variation
- Mandrel & spacer width control critical to minimize pitch walking
- Only one feature width, but can be trimmed with extra mask



Self-Aligned Metal Patterning

Self-aligned via

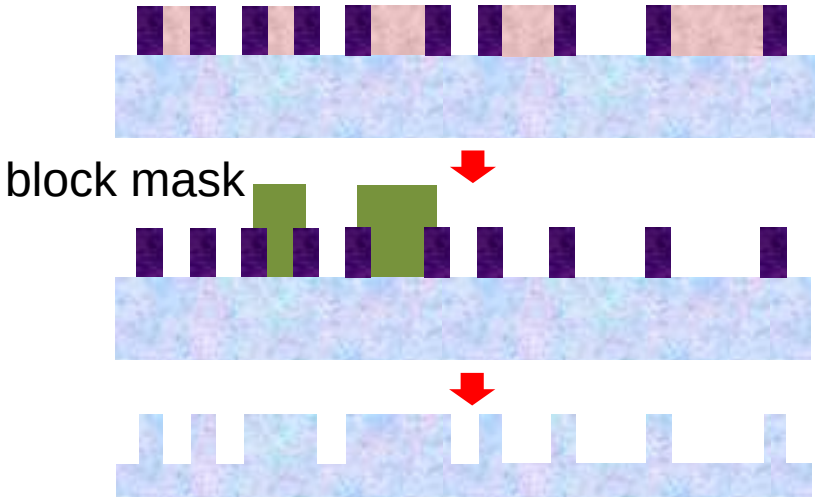
- Dual-damascene metal integration
- Conceptually similar to cuts
- Via etch only at intersection of trench & via masks



Brain *et al.*, Intel [16]

SADP/SAQP + block mask

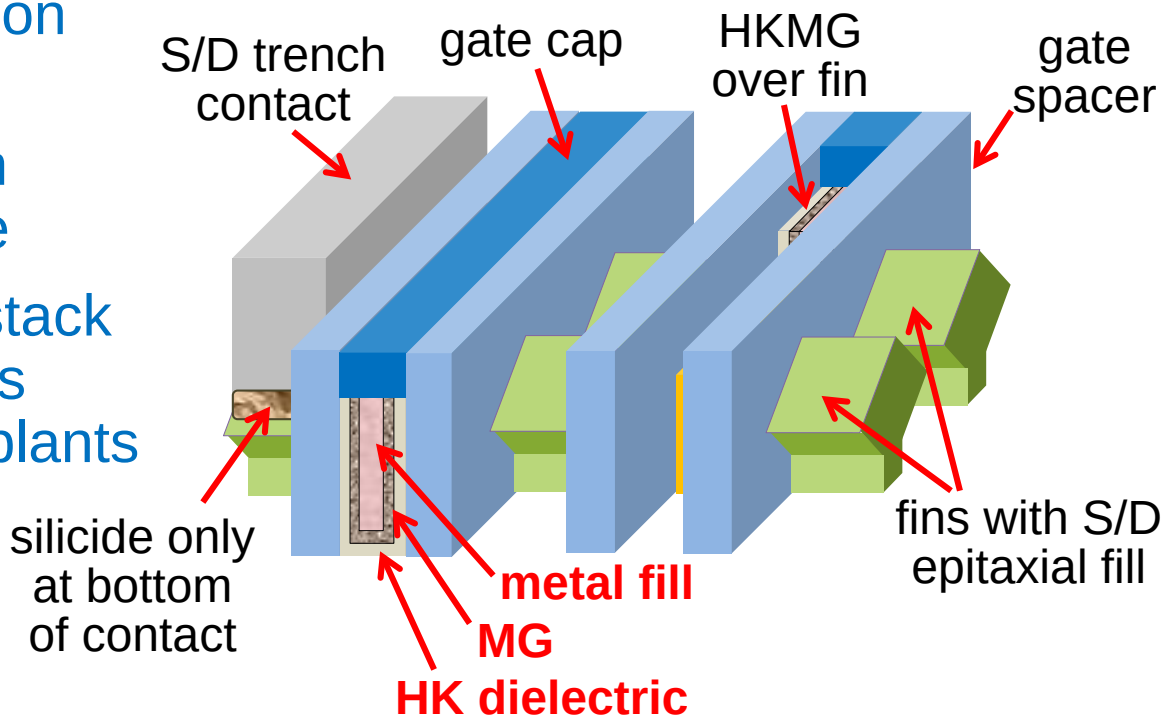
- Block mask to bridge several spacers
- Adjust mandrel width/space for more flexible metal width/space



Woo *et al.*, Globalfoundries [15]

High-*K* + Metal-Gate (HKMG) → Higher C_{ox}

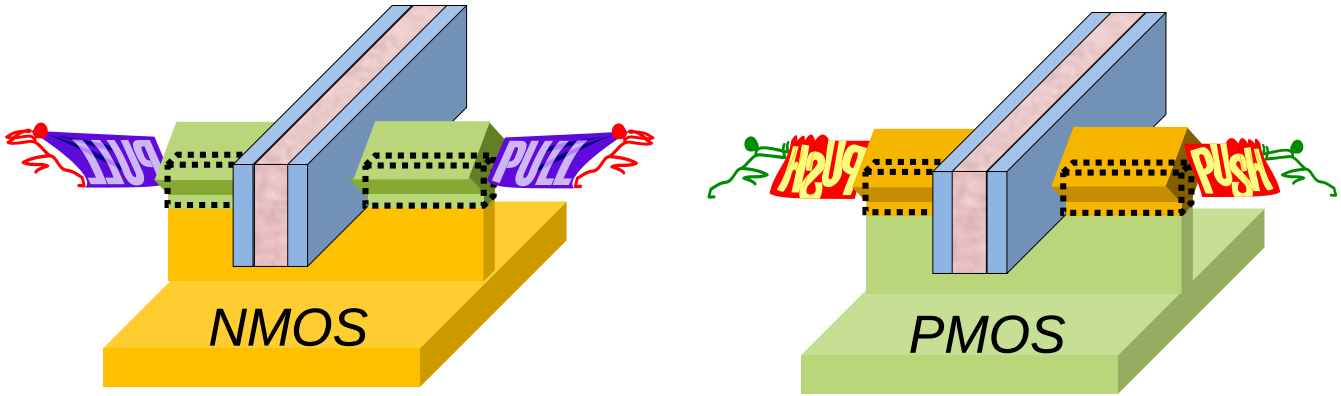
- Less I_{gate}, no poly depletion
- Replacement metal gate (RMG) for stable V_T with delicate HK/MG interface
- V_T tuning with ALD MG stack composition & HK dipoles → less variation than implants
- High gate resistance
- High S/D resistance with silicide last



Hou, TSMC [9]
Auth *et al.*, Intel [14]

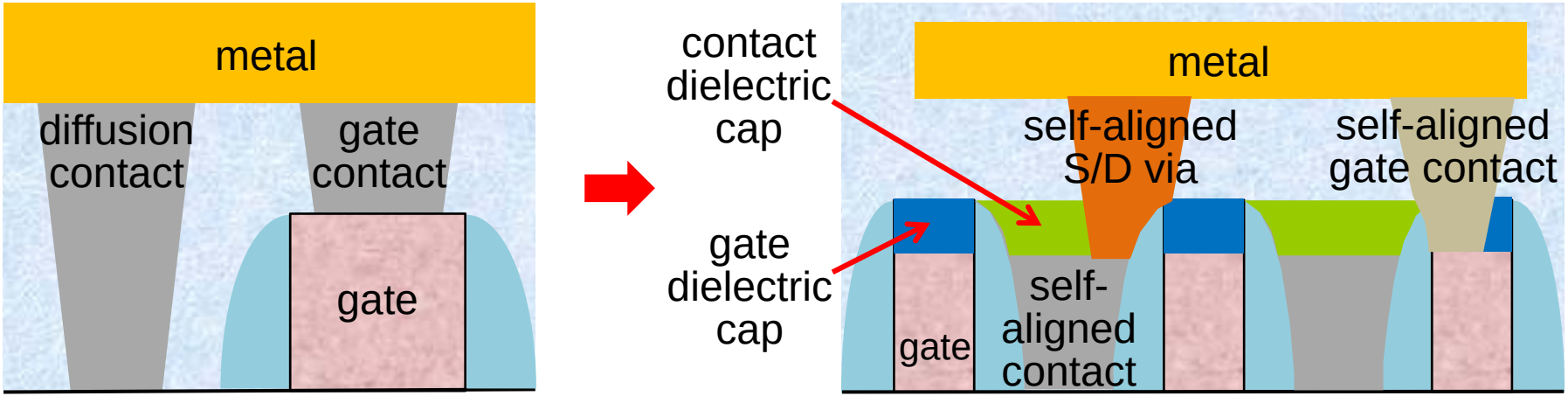
Mechanical Stressors → Mobility Boost

- Induce channel strain along *L* with surrounding stressors
  - Tensile for NMOS, compressive for PMOS (but reality very complicated)
  - Techniques: S/D fin recess & epitaxy, gate stress
- More effective for PMOS, *β* ratio → 1, not scaling well with CGP
- Less effective for longer *L*



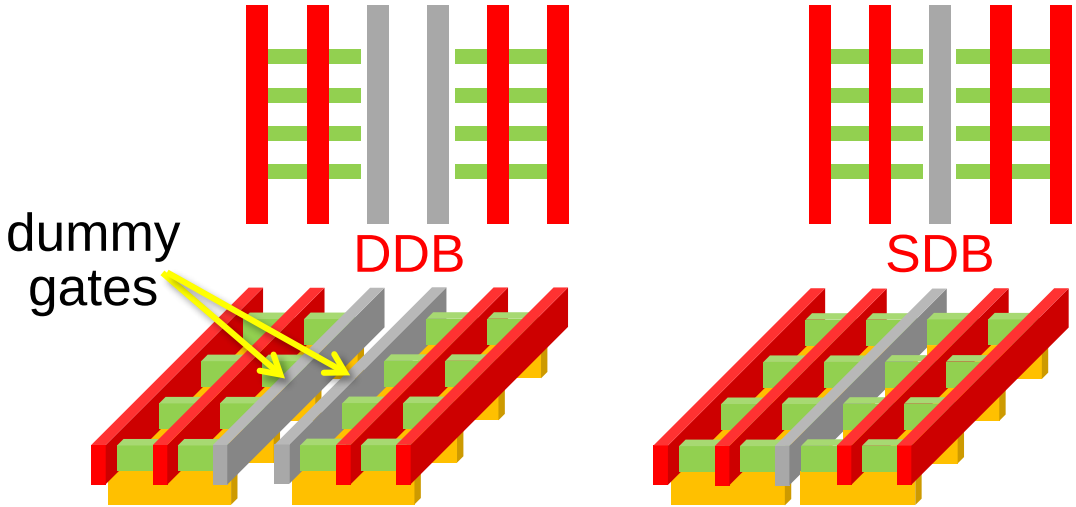
Complex MEOL & Self-Aligned Contacts

- Tight CGP → tough to land diffusion & gate contacts without shorts
- Dielectric caps protect gate & contact against etch
- Self-aligned gate contacts over fins, not restricted to gate overhang
- More interfaces → high S/D, MEOL & lower BEOL resistance



Single vs. Double Diffusion Break

- Dummy gates terminate OD to constrain S/D epitaxy
- SDB eliminates dummy gate waste → saves 10–20% logic area
- Aggressive tensile dielectric isolation for SDB → stress LDE



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  - **Passives**
  - **Diodes**
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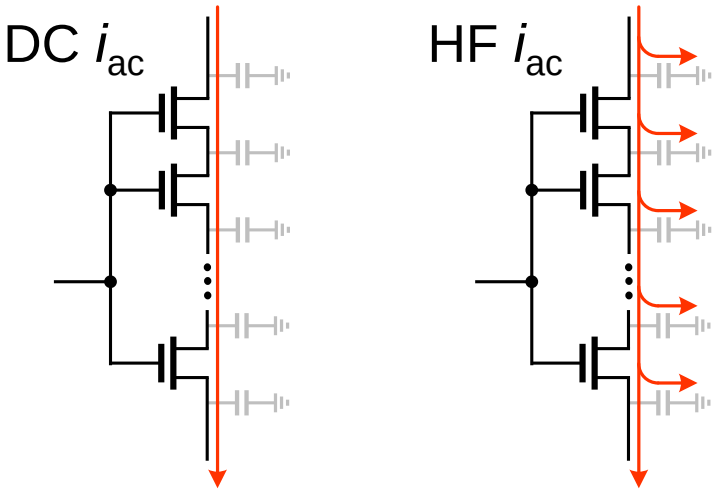
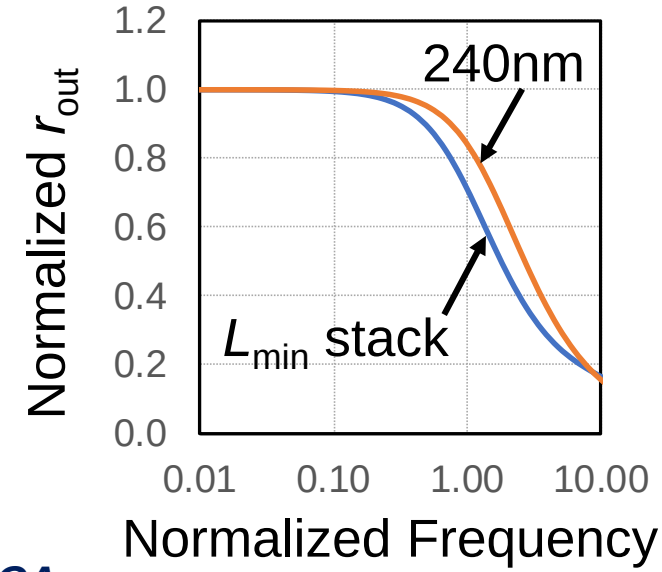
Stacked FET for Higher r_{out}

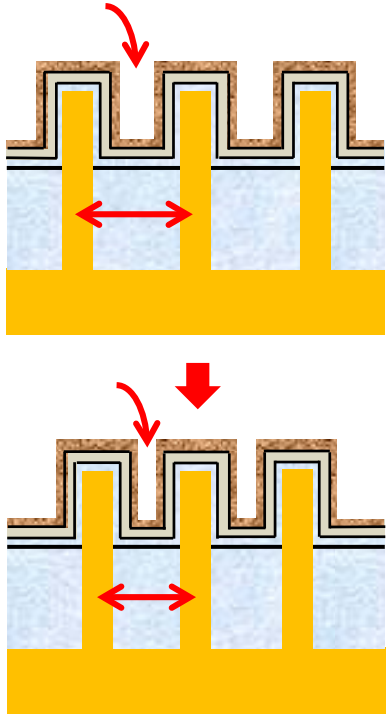
- L_{max} limited by gate litho/etch loading & HKMG CMP
- Short L has most μ boost → potentially less area
- Intermediate diffusions degrade HF r_{out} (gain, CMRR, …)





Thick-Oxide I/O FET

- GPIOs still use 1.8V swing despite reduced core V_{DD}
  - Talk to peripheral ICs made in lower cost nodes
- Challenging to keep 1.8V I/O devices
  - Tighter fin pitch → tough ALD gate fill
  - Complex level shifters to handle larger ΔV_{DD}
  - Many links stopped supporting legacy modes to enable higher data rate & lower power
  - Improve power & area with thinner I/O oxide, e.g., 1.2V

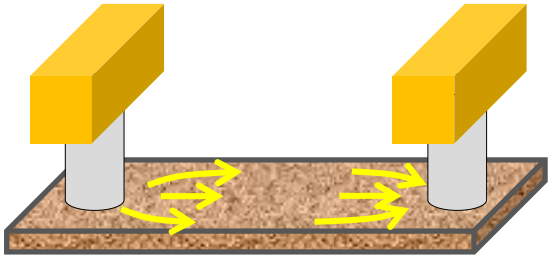


tighter fin pitch

Passives (*RCL*)

Resistors

- MEOL thin film resistor
  - HKMG → poly resistor obsolete
  - Variation limits area scaling
- Gate resistor – unusable, high variation

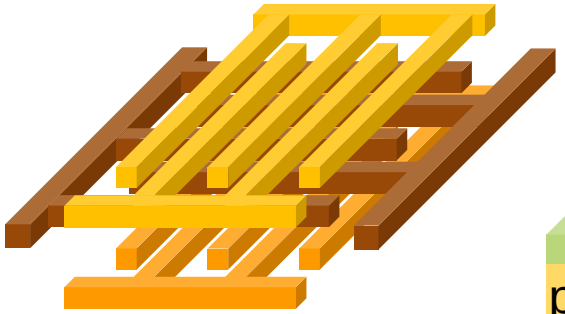


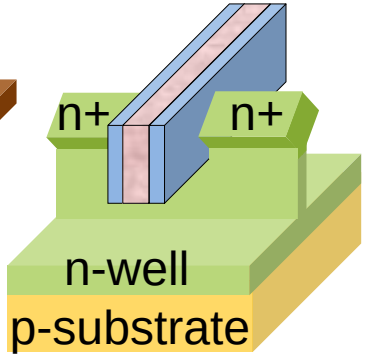
Inductors

- Upper BEOL layers
- Small impact from scaling, but more fill

Capacitors

- BEOL MOM (Metal-Oxide-Metal)
  - High density with metal pitch scaling
  - Reduced AC coupling efficiency
- Accumulation-mode varactor
  - Steeper *C-V* transition
- Upper-BEOL MIM – uncommon in mobile

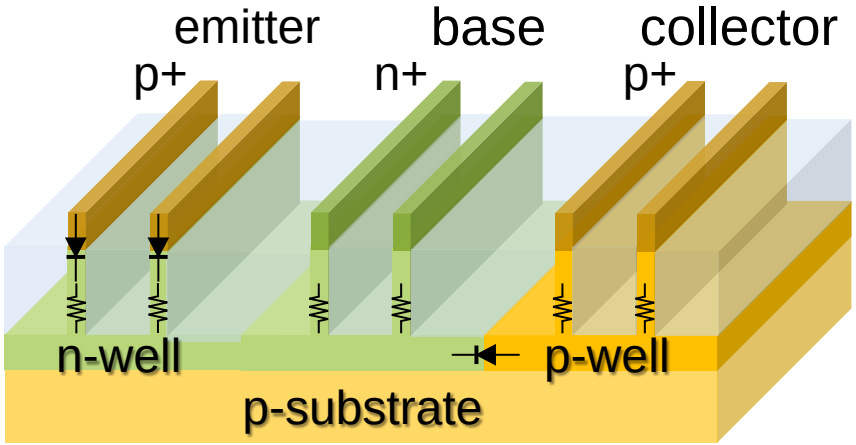




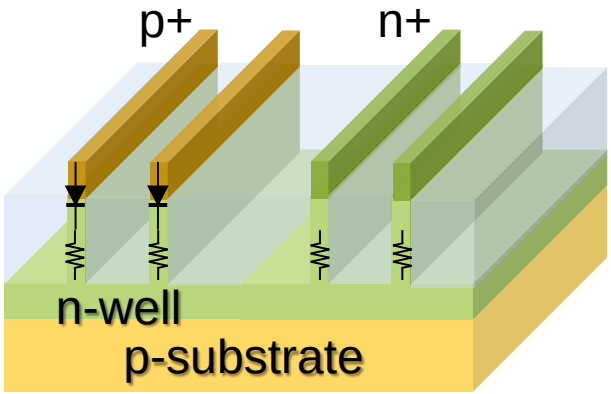
Diodes

- High R_{well} → stricter well tie, guard ring & latch-up rules
- ESD & latch-up guidelines immature during technology development

PNP-BJT (Analog Diode)



STI ESD Diode



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  - Parasitics
  - Layout-Dependent Effects (LDEs)
  - Layout Considerations
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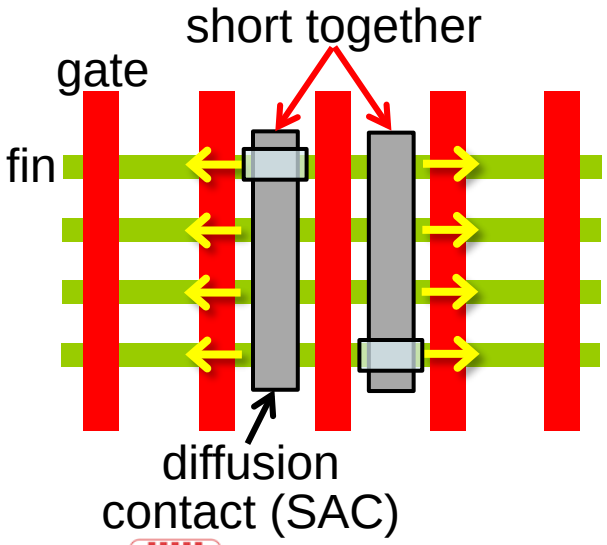
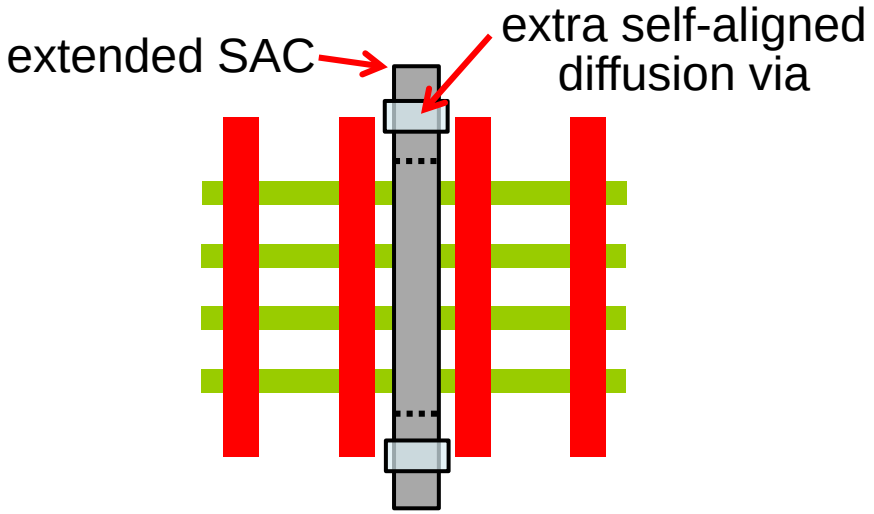
Diffusion & MEOL Resistance

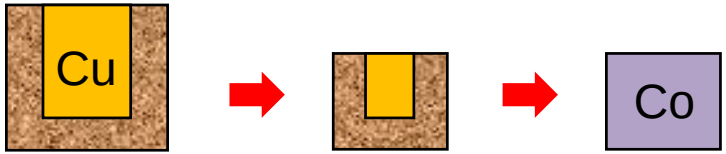
- Challenging for high-current circuits, e.g., I/O drivers, clock buffers
- Double-source layout halves S/D $R_{contact}$ (despite higher C)
- Extend SAC to land extra diffusion via



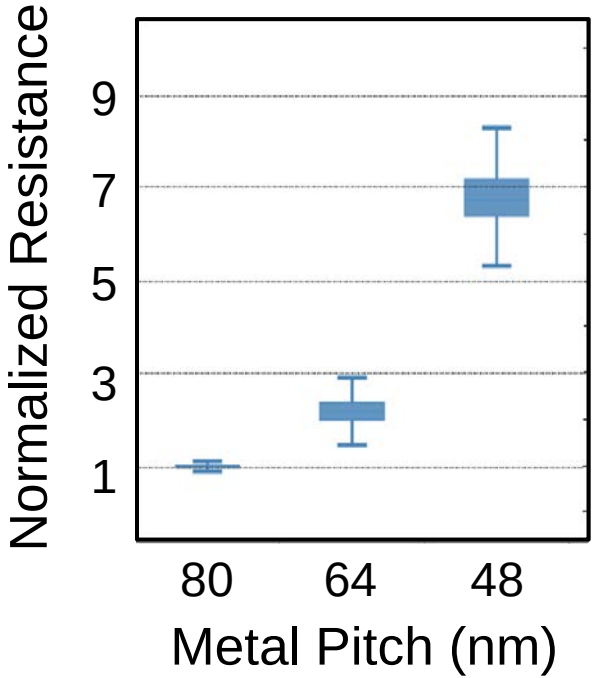


BEOL Resistance

- Aggressive M1-M3 pitch scaling for dense logic routing → less die area & cost
- Meticulous pitch optimization for PPAC
- High-ρ TaN barrier cladding Cu wire not scaling with metal pitch

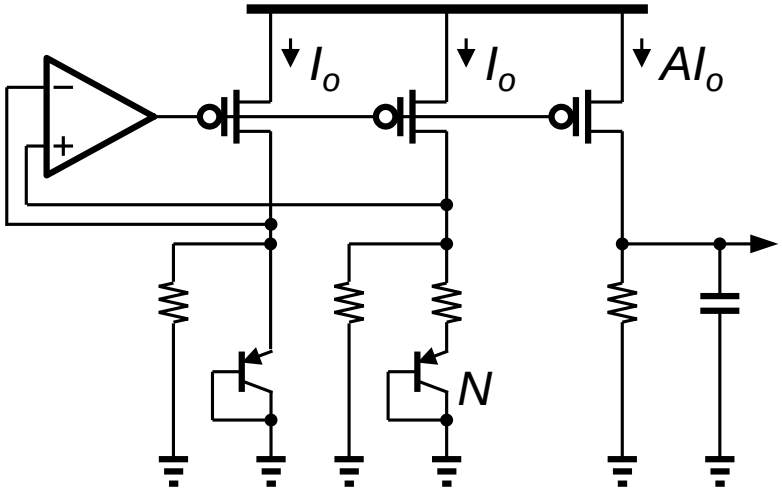


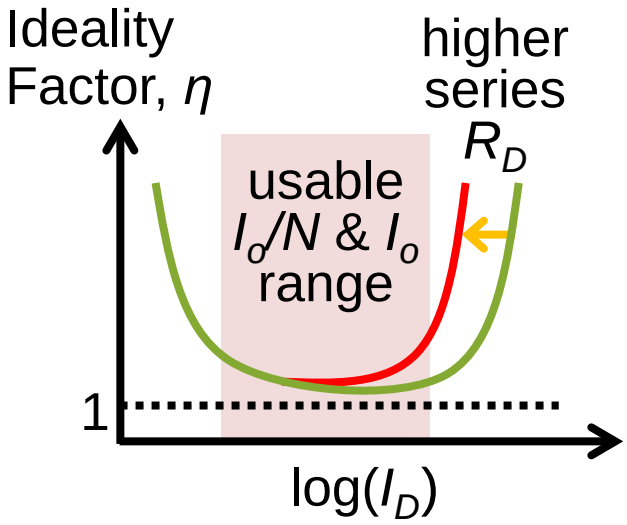
- Barrier-less cobalt & ruthenium with higher ρ are promising material enablers



Auth *et al.*, Intel [14]
Yang *et al.*, Qualcomm [22]

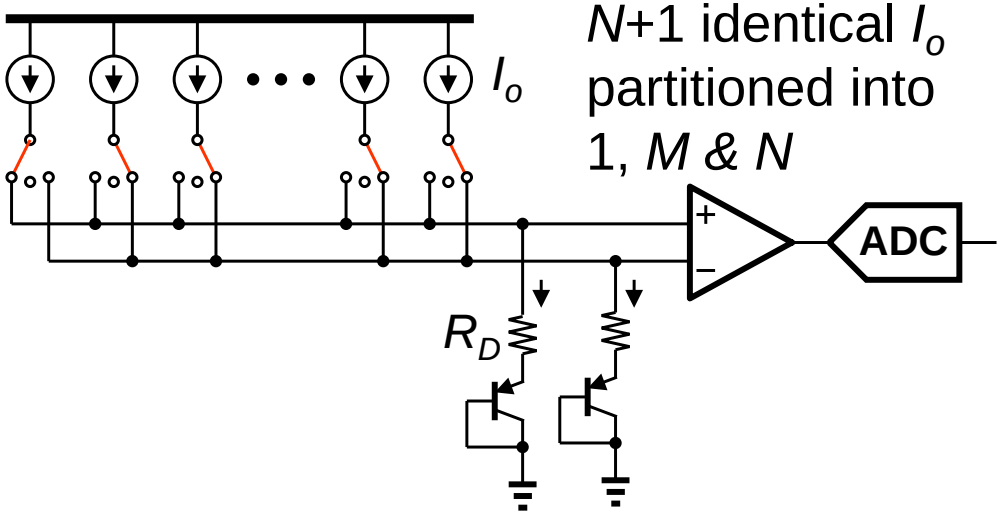
Low-Voltage Bandgap Reference





- Higher R_D → smaller N → variation sensitivity
- Higher V_D from high well doping → higher V_{DD} (e.g., 1.2V) for headroom
- Variation dominated by PMOS mirror mismatch → trimming

Thermal Sensor with R_D Cancellation



$$\Delta V_{BE,M} = \frac{\eta kT}{q} \ln M + (M\text{-}1)\, I_o R_D$$

$$\Delta V_{BE,N} = \frac{\eta kT}{q} \ln N + (N\text{-}1)\, I_o R_D$$

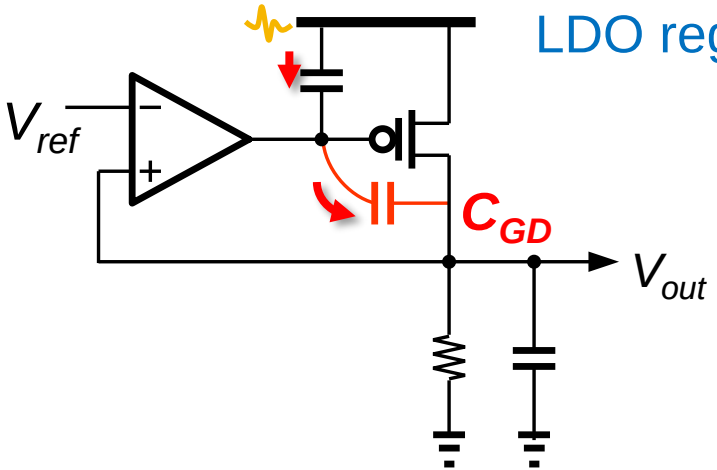
$$\frac{\eta kT}{q} = \frac{(N\text{-}1)\Delta V_{BE,M} - (M\text{-}1)\Delta V_{BE,N}}{(N\text{-}1)\ln M - (M\text{-}1)\ln N}$$

- Measure ΔV_{BE} at M:1 & N:1 → cancel R_D
- DEM → cancel I_o mismatch
- Swap amp inputs → cancel diode mismatch

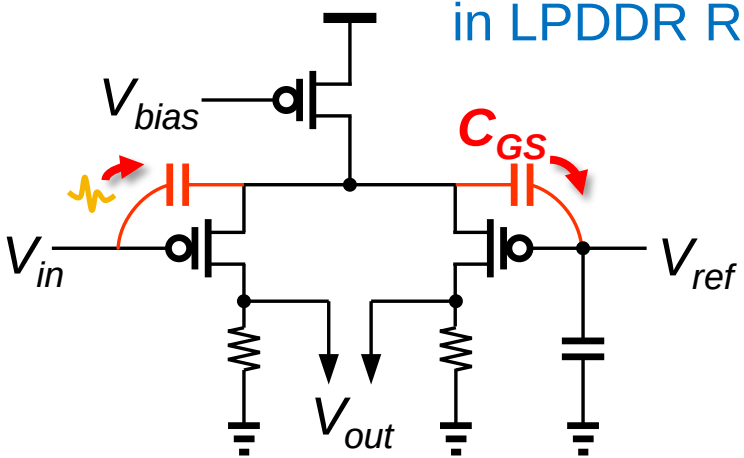
Parasitic Capacitance Impact on Analog

- S/D trench contacts & gate form vertical plate capacitors
- Adding capacitance increases area & wake-up time (burst-mode)

Worse PSRR in LDO regulator

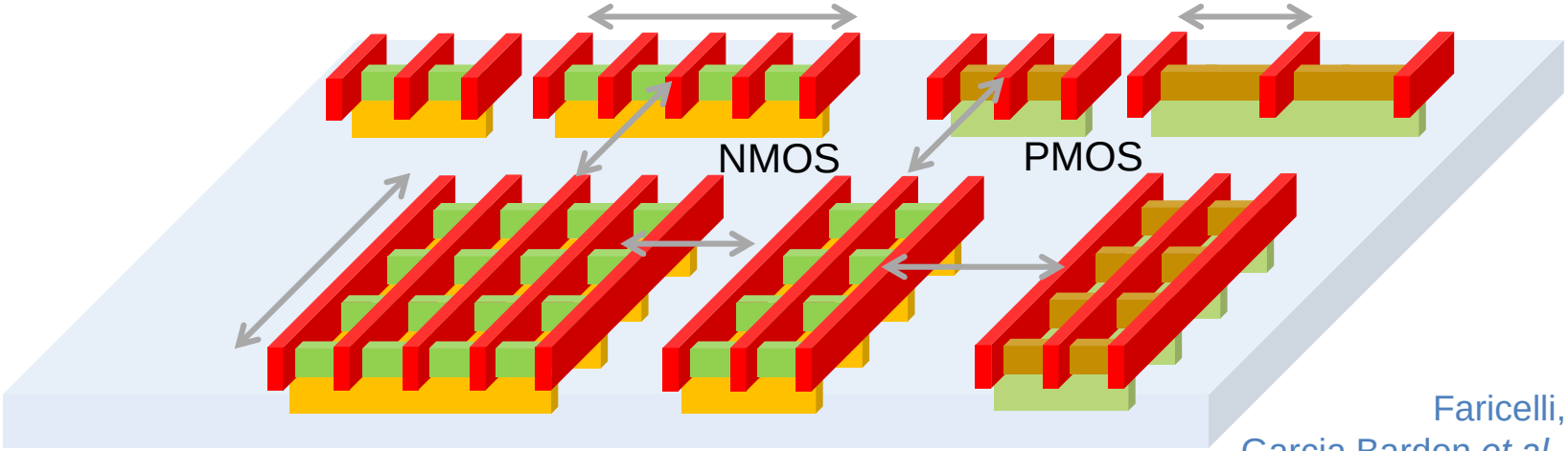


Kickback noise in LPDDR RX



Stress LDEs

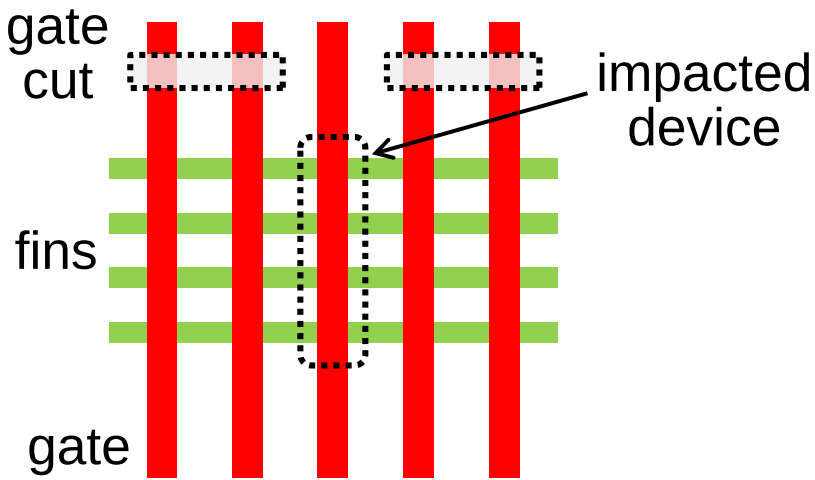
- Stronger stressors & layout effects → schematic/layout Δ
- Stress build-up in longer OD, I_D per fin not constant vs. # fins
- Interaction with surrounding tensile STI & ILD stress
- NMOS/PMOS stress mutually weaken each other

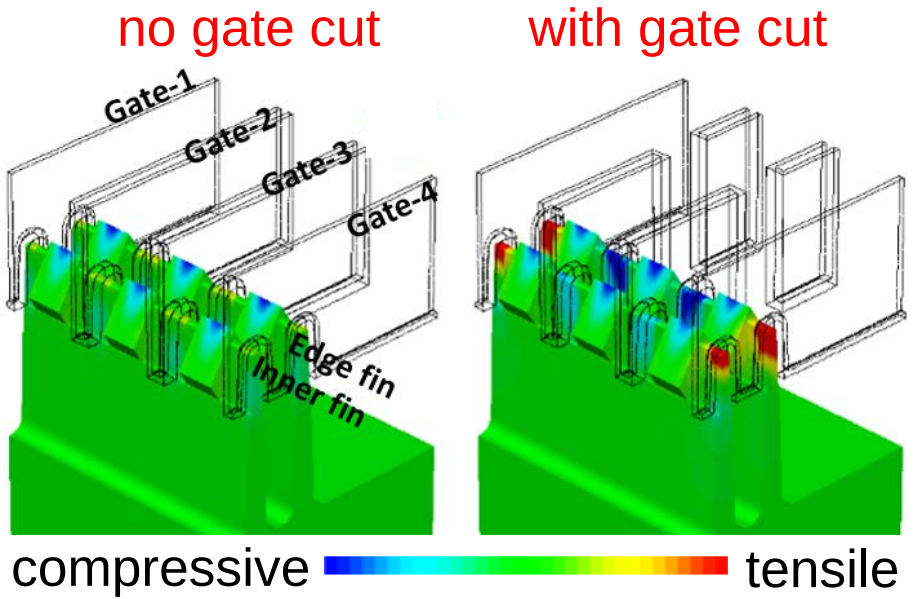


Faricelli, AMD [29]
Garcia Bardon *et al.*, imec [30]
Bianchi *et al.*, STMicroelectronics [31]

Gate Cut Stress LDE

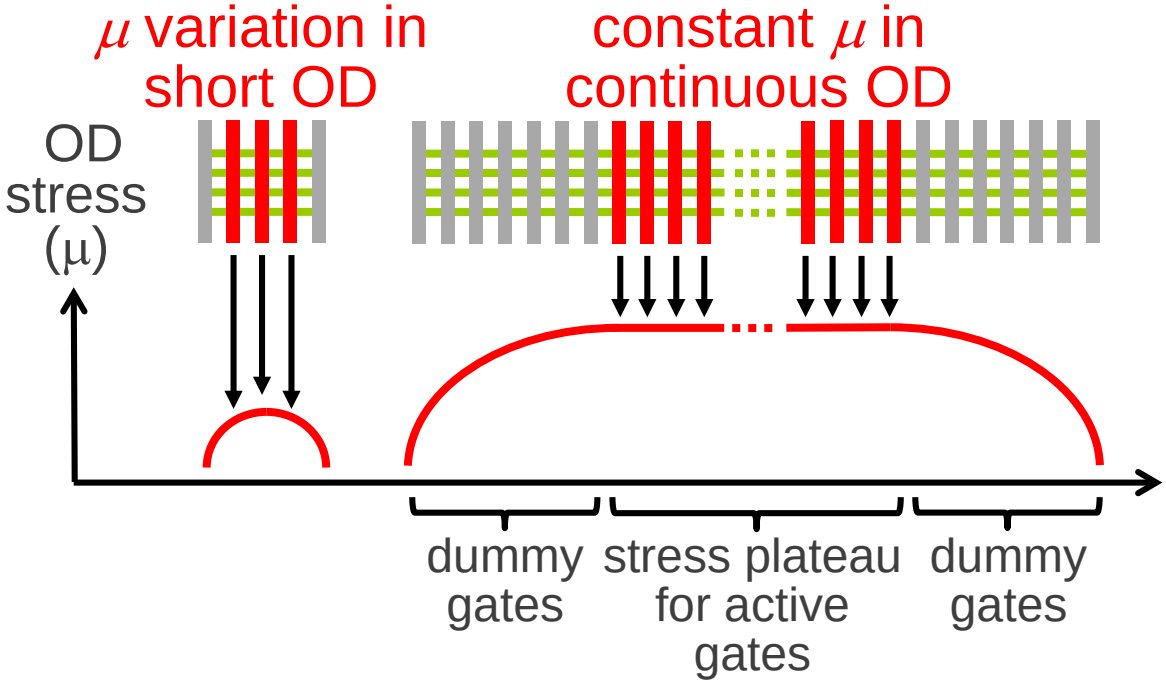
- Gate cut disrupts mechanical support of continuous gate
- Modulate stress near cut → $\Delta\mu$ & ΔV_T, modeled in post-layout netlist





Continuous OD for Performance & Matching

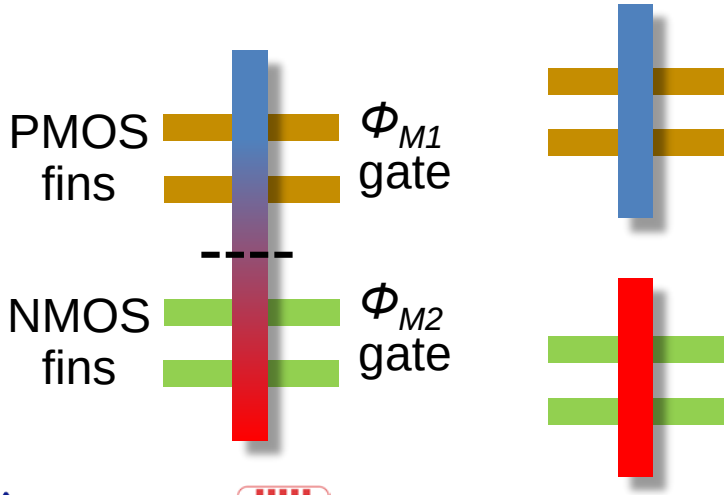
- Build up stress plateau for higher μ
- Desensitize FET from μ variation in short OD
- Most critical for short *L* with strongest LDE
- Matched FETs also need matched spacing to surrounding devices



HKMG LDEs

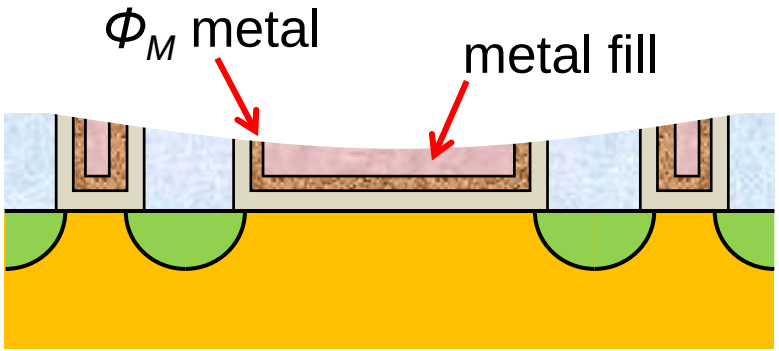
Metal Boundary Effect

- ΔV_T near border of different Φ_M
- Interdiffusion of Φ_M
- Modeled in post-layout netlist



Gate Density Induced Mismatch

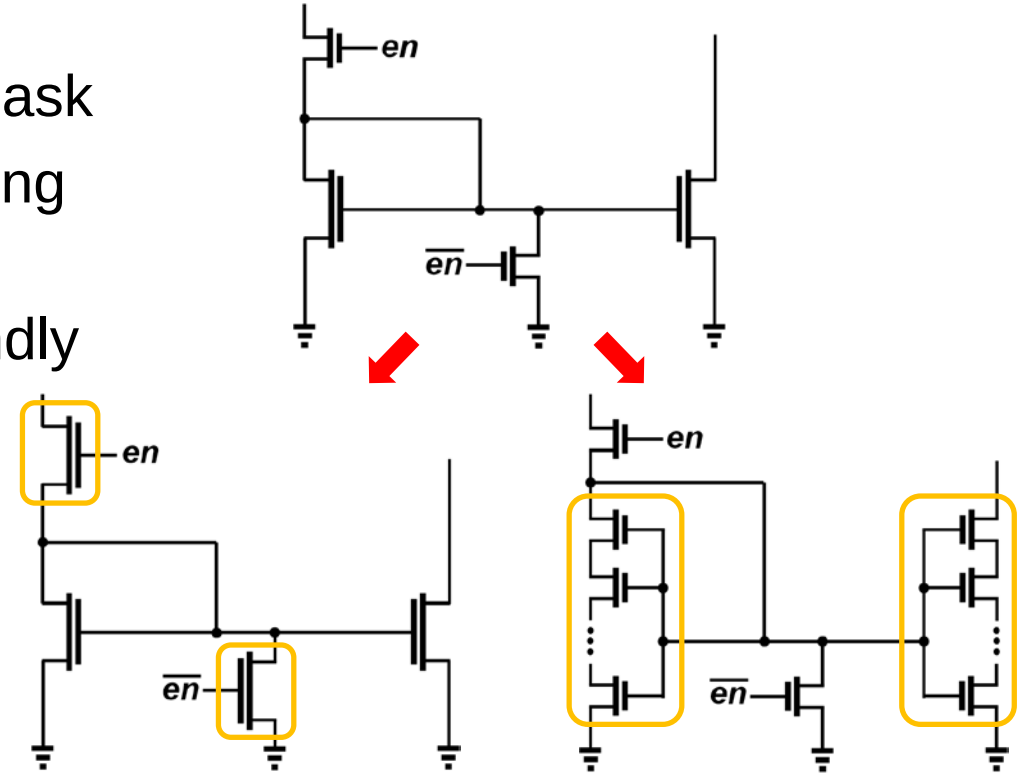
- ΔV_T from RMG CMP dishing
- Φ_M influenced by metal fill & sidewall MG
- Not modeled, contained with DRC



Yang et al, Qualcomm [24]
Hamaguchi *et al*., Toshiba [33]

Current Mirror with Enable Devices

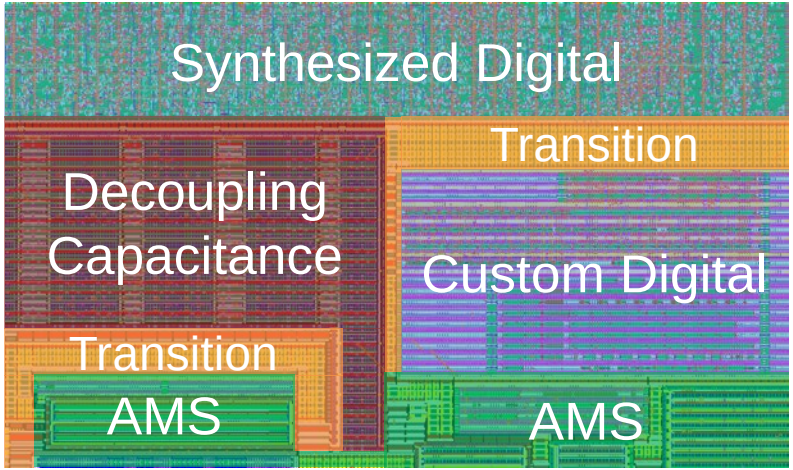
- Short *L* patterned by SADP; long *L* with conventional 2nd mask
- SADP prone to litho/etch loading effects
- Consistent *L* more SADP-friendly
- Avoid mixing short- & long-channel FETs



Layout Density & Floorplan Considerations

- Tougher DRCs → AMS layout resemble logic arrays
- Density checks to reduce long-range pattern variation
  → iterative rework of smaller cells
  - Contacts, vias, cuts, tight-pitch metal
  - Area, perimeter, gradient
  - Larger checking windows
  - Density union of multiple metal levels
- Floorplanning more tedious & bloated
  - More dummy gates, well taps, guard rings
  - Transitions between different device types & pattern densities

ADPLL partial floorplan



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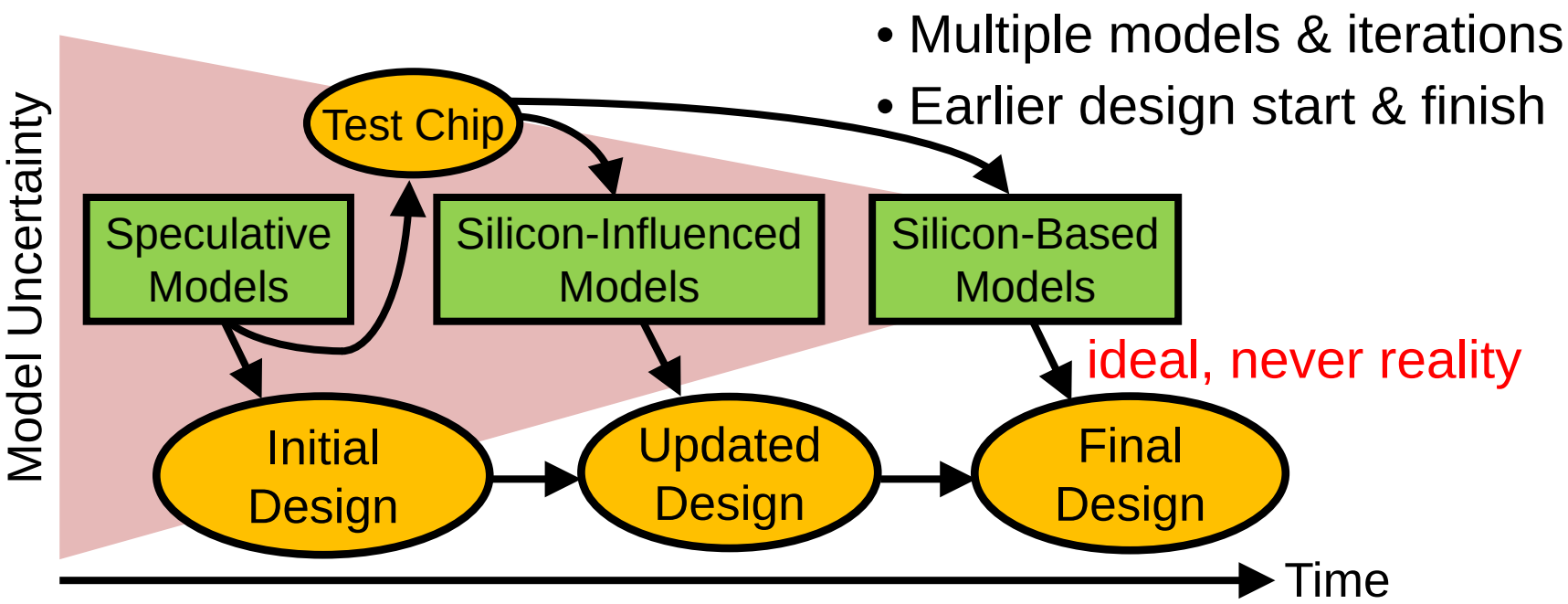
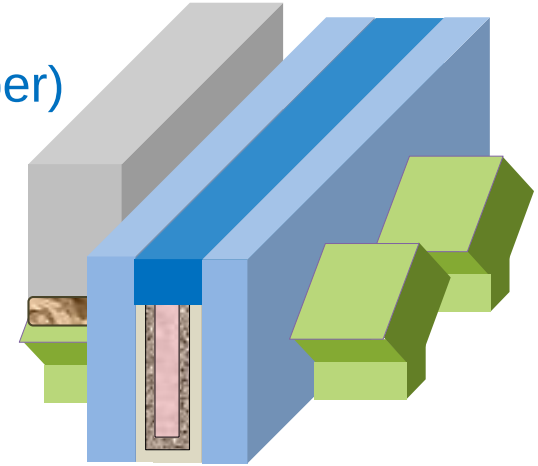
Bleeding-Edge Product Development

- Design while technology being developed to shorten time-to-market



Dealing with Target-Based Model Uncertainty

- Process at tapeout more immature in each new node
  - More masks & longer fab cycle time → fewer cycles of silicon learning
- Process development areas, even after tapeout
  - HKMG stack & RMG optimization to tune multiple V_T
  - S/D epitaxy, MEOL modules (contacts, vias & metal)
  - Logic & SRAM area-saving constructs (SDB, S/D jumper)
- Most vulnerable (unstable) model parameters
  - FET V_T, μ, LDEs
  - Long *L* & I/O FETs usually impacted, not priority #1
  - *RC* parasitics in S/D & MEOL
- Trade incremental AMS area for reduced exposure



Overcoming Process/Model Immaturity

Layout Guideline	Reduced Exposure
Use continuous OD stress plateau	Stress LDEs (S/D epitaxy, STI)
Attach dummy FETs to OD ends	
Avoid single-diffusion break	
Use only one Φ_M in each gate	Metal boundary LDE
Avoid using gate as interconnect	Gate cut LDE
Contact gate on both sides	Gate resistance, Φ_M tuning to adjust V_T
Use groups of fewer fins	
Use double-source layout for high-*I* nets	S/D contact resistance & epitaxy
Extend S/D contact to land extra via	MEOL & S/D resistance
Do not push DRCs to limit	DRC updates

Conclusion

- AMS design in remaining CMOS nodes is tedious & about managing technology-imposed non-idealities
- AMS area scaling 0.8-0.9x per node vs. 0.5x for logic/SRAM
- Parasitics & LDEs only get worse, will ultimately limit scaling
- Digital-friendly AMS design inspires new performance, power & integration levels
- Implementation just requires a lot more perspiration

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